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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 150K Logic Modules
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	536-LFBGA, CSPBGA
Supplier Device Package	536-CSPBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s150t-fcsg536i

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- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for T_J symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

where

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the package edge)
- T_C = Case temperature
- P = Total power dissipated by the device

Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices

Device	Still Air	1.0 m/s	2.5 m/s	θ_{JB}	θ_{JC}	Unit
	θ_{JA}					
005						
FG484	19.36	15.81	14.63	9.74	5.27	°C/W
VF256	41.30	38.16	35.30	28.41	3.94	°C/W
VF400	20.19	16.94	15.41	8.86	4.95	°C/W
TQ144	42.80	36.80	34.50	37.20	10.80	°C/W
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
VF256	37.36	34.26	31.45	24.84	7.89	°C/W
VF400	19.40	15.75	14.22	8.11	4.22	°C/W
TQ144	38.60	32.60	30.30	31.80	8.60	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
VF256	33.85	30.59	27.85	21.63	6.13	°C/W
VF400	18.36	14.89	13.36	7.12	3.41	°C/W
FCS325	29.17	24.87	23.12	14.44	2.31	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
FG896	14.70	12.50	10.90	7.20	4.90	°C/W
VF400	17.53	14.17	12.63	6.32	2.81	°C/W
FCS325	27.38	23.18	21.41	12.47	1.59	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
FG676	15.49	12.21	11.06	7.07	3.87	°C/W
VF400	17.45	14.01	12.47	6.22	2.69	°C/W
FCS325	27.03	22.91	21.25	12.33	1.54	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
FG676	14.52	11.19	10.37	6.17	3.24	°C/W
FCS325	26.63	22.26	20.13	14.24	2.50	°C/W

Table 48 • LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.8 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 49 • LVCMOS 1.8 V DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
LVCMOS 1.8 V DC Recommended Operating Conditions					
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 50 • LVCMOS 1.8 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	V_{IL} (DC)	-0.3	$0.35 \times V_{DDI}$	V
Input current high ¹	I_{IH} (DC)			-
Input current low ¹	I_{IL} (DC)			-

1. See Table 24, page 22.

Table 51 • LVCMOS 1.8 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	$V_{DDI} - 0.45$		V
DC output logic low	V_{OL}		0.45	V

Table 52 • LVCMOS 1.8 V Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank) ¹	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	295	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank) ¹	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DDI}	1.425	1.5	1.575	V

Table 61 • LVCMOS 1.5 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high for (MSIOD and DDRIO I/O banks)	V _{IH} (DC)	0.65 × V _{DDI}	1.575	V
DC input logic high (for MSIO I/O bank)	V _{IH} (DC)	0.65 × V _{DDI}	3.45	V
DC input logic low	V _{IL} (DC)	-0.3	0.35 × V _{DDI}	V
Input current high ¹	I _{IH} (DC)			-
Input current low ¹	I _{IL} (DC)			-

1. See Table 24, page 22.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

Table 67 • LVCMOS 1.5 V Receiver Characteristics for DDRIO I/O Bank with Fixed Codes (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.051	2.413	2.086	2.455	ns

Table 68 • LVCMOS 1.5 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	3.311	3.896	3.285	3.865	ns
50	3.654	4.299	3.623	4.263	ns
75	3.533	4.156	3.501	4.119	ns
150	3.415	4.018	3.388	3.986	ns

Table 69 • LVCMOS 1.5 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.959	3.481	2.93	3.447	ns
50	3.298	3.88	3.268	3.845	ns
75	3.162	3.719	3.128	3.68	ns
150	3.053	3.592	3.021	3.554	ns

Table 70 • LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns

Table 144 • LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	$0.6 \times V_{DDI}$		V
AC differential cross point voltage	V_x	$0.4 \times V_{DDI}$	$0.6 \times V_{DDI}$	V

Table 145 • LPDDR AC Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 146 • LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance	R_{REF}	20, 42	Ω	Reference resistor = 150 Ω
Effective impedance value (ODT)	R_{TT}	50, 70, 150	Ω	Reference resistor = 150 Ω

Table 147 • LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for LPDDR (T_{DP})	R_{TT_TEST}	50	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	Ω

AC Switching Characteristics

Worst-case commercial conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, worst-case V_{DDI} .

Table 148 • LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes

	On-Die Termination (ODT)	T_{PY}		Unit
		-1	-Std	
Pseudo differential	None	1.568	1.845	ns
True differential	None	1.588	1.869	ns

Table 149 • LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns

Table 156 • LPDDR-LVCMOS 1.8 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.9	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 157 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification for DDRIO Bank

Output Drive Selection	V_{OH} (V) Min	V_{OL} (V) Max	I_{OH} (at V_{OH}) mA	I_{OL} (at V_{OL}) mA
2 mA	$V_{DDI} - 0.45$	0.45	2	2
4 mA	$V_{DDI} - 0.45$	0.45	4	4
6 mA	$V_{DDI} - 0.45$	0.45	6	6
8 mA	$V_{DDI} - 0.45$	0.45	8	8
10 mA	$V_{DDI} - 0.45$	0.45	10	10
12 mA	$V_{DDI} - 0.45$	0.45	12	12
16 mA ¹	$V_{DDI} - 0.45$	0.45	16	16

1. 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

Table 158 • LPDDR-LVCMOS 1.8V AC Switching Characteristics for Receiver (for DDRIO I/O Bank with Fixed Code - Input Buffers)

ODT (On Die Termination)	-1	-Std	-1	-Std	Unit
None	1.968	2.315	2.099	2.47	ns

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ} ¹		T_{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	medium_fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	medium_fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	medium_fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns

Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.554	3.004	ns
100	2.549	2.999	ns

Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics
Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$.

Table 180 • B-LVDS AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

Table 181 • B-LVDS AC Switching Characteristics for Receiver for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 182 • B-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

2.3.7.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 183 • M-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage ¹	V_{DDI}	2.375	2.5	2.625	V

1. Only M-LVDS TYPE I is supported.

Table 184 • M-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high ¹	I_{IH} (DC)			
Input current low ²	I_{IL} (DC)			

1. See Table 24, page 22.

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	0.3	2.1	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

The following table lists the input data register propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 219 • Input Data Register Propagation Delays

Parameter	Symbol	Measuring Nodes (from, to) ¹	-1		Unit
			-1	-Std	
Bypass delay of the input register	T_{IBYP}	F, G	0.353	0.415	ns
Clock-to-Q of the input register	T_{ICLKQ}	E, G	0.16	0.188	ns
Data setup time for the input register	T_{ISUD}	A, E	0.357	0.421	ns
Data hold time for the input register	T_{IHD}	A, E	0	0	ns
Enable setup time for the input register	T_{ISUE}	B, E	0.46	0.542	ns
Enable hold time for the input register	T_{IHE}	B, E	0	0	ns
Synchronous load setup time for the input register	T_{ISUSL}	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	T_{IHSL}	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	T_{IALN2Q}	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	T_{IWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 234 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.32	0.377	ns
Read access time without pipeline register	T_{CLK2Q}			2.272	2.673	ns
Access time with feed-through write timing				1.511	1.778	ns
Address setup time	T_{ADDRSU}	0.612		0.72		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.33		0.388		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}			1.511	1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.529		0.622		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}			1.528	1.797	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.488		0.574		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}			400	340	MHz

Table 259 • 2 Step IAP Programming (Fabric Only)

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	302672	4	39	6	Sec	
010	568784	7	45	12	Sec	
025	1223504	14	55	23	Sec	
050	2424832	29	74	40	Sec	
060	2418896	39	83	50	Sec	
090	3645968	60	106	73	Sec	
150	6139184	100	154	120	Sec	

Table 260 • 2 Step IAP Programming (eNVM Only)

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	137536	2	59	5	Sec	
010	274816	4	98	11	Sec	
025	274816	4	100	10	Sec	
050	2,78,528	3	107	9	Sec	
060	268480	5	98	22	Sec	
090	544496	10	174	43	Sec	
150	544496	10	175	44	Sec	

Table 261 • 2 Step IAP Programming (Fabric and eNVM)

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	439296	6	78	11	Sec	
010	842688	11	122	21	Sec	
025	1497408	19	135	32	Sec	
050	2695168	32	158	48	Sec	
060	2686464	43	159	70	Sec	
090	4190208	68	258	115	Sec	
150	6682768	109	308	162	Sec	

Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

Table 265 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	69	49	50	Sec
010	99	57	57	Sec
025	150	64	63	Sec
050	55 ¹	Not Supported	Not Supported	Sec
060	313	105	104	Sec
090	449	131	130	Sec
150	730	179	183	Sec

1. Auto programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

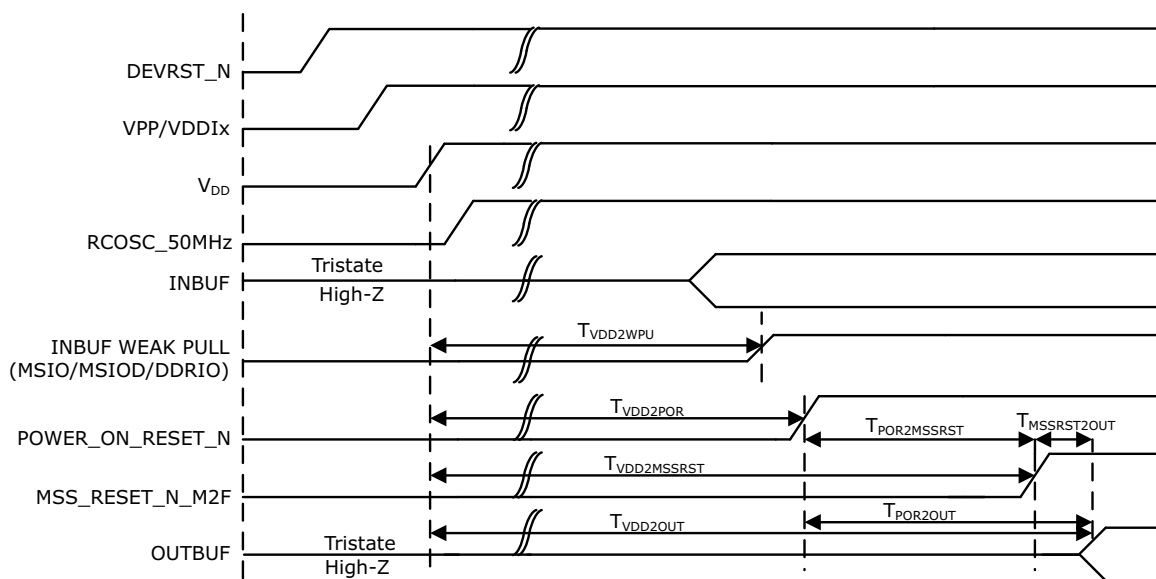
Table 266 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	63	70	71	Sec
010	108	109	109	Sec
025	109	107	108	Sec
050	107	Not Supported	Not Supported	Sec
060	100	108	108	Sec
090	176	184	184	Sec
150	183	183	183	Sec

Table 267 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)

M2S/M2GL Device	Auto Programming			Unit
	100 kHz	25 MHz	12.5 MHz	
005	109	89	88	Sec
010	183	135	135	Sec
025	251	142	143	Sec
050	134	Not Supported	Not Supported	Sec
060	390	183	180	Sec
090	604	283	282	Sec
150	889	331	332	Sec

Figure 17 • Power-up to Functional Timing Diagram for SmartFusion2



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 289 • Power-up to Functional Times for IGLOO2

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 292 • DEVRST_N to Functional Times for IGLOO2

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	116	113	113	115	115	114
$T_{DEVRST2OUT}$	DEVRST_N	Output available at I/O	V_{DD} at its minimum threshold level to output	314	353	314	307	343	341	341
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	200	238	201	195	230	229	227
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

Table 310 • SPI Characteristics for All Devices (continued)

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	15			ns	
sp9m	SPI_[0 1]_DI hold time ²	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time ²	3			ns	
sp9s	SPI_[0 1]_DI hold time ²	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 23 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

