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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I ² C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 150K Logic Modules |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s150ts-1fc1152 |



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2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 38 • LVCMOS 2.5 V DC Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-----------|-------|-----|-------|------|
| Supply voltage | V_{DDI} | 2.375 | 2.5 | 2.625 | V |

Table 39 • LVCMOS 2.5 V DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---------------|------|-------|------|
| DC input logic high (for MSIOD and DDRIO I/O banks) | V_{IH} (DC) | 1.7 | 2.625 | V |
| DC input logic high (for MSIO I/O bank) | V_{IH} (DC) | 1.7 | 3.45 | V |
| DC input logic low | V_{IL} (DC) | -0.3 | 0.7 | V |
| Input current high ¹ | I_{IH} (DC) | | | |
| Input current low ¹ | I_{IL} (DC) | | | |

1. See [Table 24](#), page 22.

Table 40 • LVCMOS 2.5 V DC Output Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|----------------------|-----------------------|-----------------|-----|------|
| DC output logic high | V_{OH} ¹ | $V_{DDI} - 0.4$ | - | V |
| DC output logic low | V_{OL} ² | | 0.4 | V |

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

Table 41 • LVCMOS 2.5 V AC Minimum and Maximum Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|--|-----------|-----|------|--|
| Maximum data rate (for DDRIO I/O bank) | D_{MAX} | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | D_{MAX} | 410 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | D_{MAX} | 420 | Mbps | AC loading: 17 pF load, maximum drive/slew |

Table 42 • LVCMOS 2.5 V AC Calibrated Impedance Option

| Parameter | Symbol | Typ | Unit |
|---|----------|------------------------|----------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)
(continued)

| Output Drive Selection | Slew Control | T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ}^1 | | T_{LZ}^1 | | Unit |
|------------------------|--------------|----------|-------|----------|-------|----------|-------|------------|-------|------------|-------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 4 mA | Slow | 3.095 | 3.641 | 2.705 | 3.182 | 3.088 | 3.633 | 4.738 | 5.575 | 4.348 | 5.116 | ns |
| | Medium | 2.825 | 3.324 | 2.488 | 2.927 | 2.823 | 3.321 | 4.492 | 5.285 | 4.063 | 4.781 | ns |
| | Medium fast | 2.701 | 3.178 | 2.384 | 2.804 | 2.698 | 3.173 | 4.364 | 5.135 | 3.945 | 4.642 | ns |
| | Fast | 2.69 | 3.165 | 2.377 | 2.796 | 2.687 | 3.161 | 4.359 | 5.129 | 3.94 | 4.636 | ns |
| 6 mA | Slow | 2.919 | 3.434 | 2.491 | 2.93 | 2.902 | 3.414 | 5.085 | 5.983 | 4.674 | 5.5 | ns |
| | Medium | 2.65 | 3.118 | 2.279 | 2.681 | 2.642 | 3.108 | 4.845 | 5.701 | 4.375 | 5.148 | ns |
| | Medium fast | 2.529 | 2.975 | 2.176 | 2.56 | 2.521 | 2.965 | 4.724 | 5.558 | 4.259 | 5.011 | ns |
| | Fast | 2.516 | 2.96 | 2.168 | 2.551 | 2.508 | 2.95 | 4.717 | 5.55 | 4.251 | 5.002 | ns |
| 8 mA | Slow | 2.863 | 3.368 | 2.427 | 2.855 | 2.844 | 3.346 | 5.196 | 6.114 | 4.769 | 5.612 | ns |
| | Medium | 2.599 | 3.058 | 2.217 | 2.608 | 2.59 | 3.047 | 4.952 | 5.827 | 4.471 | 5.261 | ns |
| | Medium fast | 2.483 | 2.921 | 2.114 | 2.487 | 2.473 | 2.91 | 4.832 | 5.685 | 4.364 | 5.134 | ns |
| | Fast | 2.467 | 2.902 | 2.106 | 2.478 | 2.457 | 2.89 | 4.826 | 5.678 | 4.348 | 5.116 | ns |
| 12 mA | Slow | 2.747 | 3.232 | 2.296 | 2.701 | 2.724 | 3.204 | 5.39 | 6.342 | 4.938 | 5.81 | ns |
| | Medium | 2.493 | 2.934 | 2.102 | 2.473 | 2.483 | 2.921 | 5.166 | 6.078 | 4.65 | 5.471 | ns |
| | Medium fast | 2.382 | 2.803 | 2.006 | 2.36 | 2.371 | 2.789 | 5.067 | 5.962 | 4.546 | 5.349 | ns |
| | Fast | 2.369 | 2.787 | 1.999 | 2.352 | 2.357 | 2.773 | 5.063 | 5.958 | 4.538 | 5.339 | ns |
| 16 mA | Slow | 2.677 | 3.149 | 2.213 | 2.604 | 2.649 | 3.116 | 5.575 | 6.56 | 5.08 | 5.977 | ns |
| | Medium | 2.432 | 2.862 | 2.028 | 2.386 | 2.421 | 2.848 | 5.372 | 6.32 | 4.801 | 5.649 | ns |
| | Medium fast | 2.324 | 2.734 | 1.937 | 2.278 | 2.311 | 2.718 | 5.297 | 6.233 | 4.7 | 5.531 | ns |
| | Fast | 2.313 | 2.721 | 1.929 | 2.269 | 2.3 | 2.706 | 5.296 | 6.231 | 4.699 | 5.529 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 47 • LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)

| Output Drive Selection | Slew Control | T_{DP} | | T_{ZL} | | T_{ZH} | | T_{HZ}^1 | | T_{LZ}^1 | | Unit |
|------------------------|--------------|----------|-------|----------|-------|----------|-------|------------|-------|------------|-------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| 2 mA | Slow | 3.48 | 4.095 | 3.855 | 4.534 | 3.785 | 4.453 | 2.12 | 2.494 | 3.45 | 4.059 | ns |
| 4 mA | Slow | 2.583 | 3.039 | 3.042 | 3.579 | 3.138 | 3.691 | 4.143 | 4.874 | 4.687 | 5.513 | ns |
| 6 mA | Slow | 2.392 | 2.815 | 2.669 | 3.139 | 2.82 | 3.317 | 4.909 | 5.775 | 5.083 | 5.98 | ns |
| 8 mA | Slow | 2.309 | 2.717 | 2.565 | 3.017 | 2.74 | 3.223 | 5.812 | 6.837 | 5.523 | 6.497 | ns |
| 12 mA | Slow | 2.333 | 2.745 | 2.437 | 2.867 | 2.626 | 3.089 | 6.131 | 7.213 | 5.712 | 6.72 | ns |
| 16 mA | Slow | 2.412 | 2.838 | 2.335 | 2.747 | 2.533 | 2.979 | 6.54 | 7.694 | 6.007 | 7.067 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 77 • LVCMOS 1.2 V AC Calibrated Impedance Option

| Parameter | Symbol | Typ | Unit |
|---|----------|----------------|------|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 40 | Ω |

Table 78 • LVCMOS 1.2 V AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|---|-------------------|-----|------|
| Measuring/trip point | V _{TRIP} | 0.6 | V |
| Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ}) | R _{ENT} | 2K | Ω |
| Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ}) | C _{ENT} | 5 | pF |
| Capacitive loading for data path (T _{DP}) | C _{LOAD} | 5 | pF |

Table 79 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

| Output Drive Selection | | | V _{OH} (V) | V _{OL} (V) | IOH (at V _{OH}) | IOL (at V _{OL}) |
|------------------------|----------------|----------------|-------------------------|-------------------------|---------------------------|---------------------------|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | V _{DDI} × 0.75 | V _{DDI} × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | V _{DDI} × 0.75 | V _{DDI} × 0.25 | 4 | 4 |
| | | 6 mA | V _{DDI} × 0.75 | V _{DDI} × 0.25 | 6 | 6 |

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.14 V

Table 80 • LVCMOS 1.2 V Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)

| On-Die Termination (ODT) | T _{PY} | | T _{PYS} | | Unit |
|--------------------------|-----------------|------|------------------|-------|------|
| | -1 | -Std | -1 | -Std | |
| None | 2.448 | 2.88 | 2.466 | 2.901 | ns |

Table 81 • LVCMOS 1.2 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

| On-Die Termination ODT) | T _{PY} | | T _{PYS} | | Unit |
|-------------------------|-----------------|-------|------------------|-------|------|
| | -1 | -Std | -1 | -Std | |
| None | 4.714 | 5.545 | 4.675 | 5.5 | ns |
| 50 | 6.668 | 7.845 | 6.579 | 7.74 | ns |
| 75 | 5.832 | 6.862 | 5.76 | 6.777 | ns |
| 150 | 5.162 | 6.073 | 5.111 | 6.014 | ns |

2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 173 • B-LVDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-----------|-------|-----|-------|------|
| Supply voltage | V_{DDI} | 2.375 | 2.5 | 2.625 | V |

Table 174 • B-LVDS DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---------------------------------|---------------|-----|-------|------|
| DC input voltage | V_I | 0 | 2.925 | V |
| Input current high ¹ | I_{IH} (DC) | | | |
| Input current low ¹ | I_{IL} (DC) | | | |

1. See Table 24, page 22.

Table 175 • B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------------|----------|------|-------|------|------|
| DC output logic high | V_{OH} | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | V_{OL} | 0.9 | 1.075 | 1.25 | V |

Table 176 • B-LVDS DC Differential Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|------|-----------|------|
| Differential output voltage swing (for MSIO I/O bank only) | V_{OD} | 65 | 460 | mV |
| Output common mode voltage (for MSIO I/O bank only) | V_{OCM} | 1.1 | 1.5 | V |
| Input common mode voltage | V_{ICM} | 0.05 | 2.4 | V |
| Input differential voltage | V_{ID} | 0.1 | V_{DDI} | V |

Table 177 • B-LVDS Minimum and Maximum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|---------------------------------------|-----------|-----|------|---|
| Maximum data rate (for MSIO I/O bank) | D_{MAX} | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

Table 178 • B-LVDS AC Impedance Specifications

| Parameter | Symbol | Typ | Unit |
|------------------------|--------|-----|----------|
| Termination resistance | R_T | 27 | Ω |

Table 179 • B-LVDS AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|--|------------|-------------|----------|
| Measuring/trip point for data path | V_{TRIP} | Cross point | V |
| Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | R_{ENT} | 2K | Ω |
| Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | C_{ENT} | 5 | pF |

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------------|----------|------|-------|------|------|
| DC output logic high | V_{OH} | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | V_{OL} | 0.9 | 1.075 | 1.25 | V |

Table 186 • M-LVDS Differential Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-----|------|------|
| Differential output voltage swing (for MSIO I/O bank only) | V_{OD} | 300 | 650 | mV |
| Output common mode voltage (for MSIO I/O bank only) | V_{OCM} | 0.3 | 2.1 | V |
| Input common mode voltage | V_{ICM} | 0.3 | 1.2 | V |
| Input differential voltage | V_{ID} | 50 | 2400 | mV |

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

| Parameter | Symbol | Max | Unit | Conditions |
|-------------------|-----------|-----|------|---|
| Maximum data rate | D_{MAX} | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

Table 188 • M-LVDS AC Impedance Specifications

| Parameter | Symbol | Typ | Unit |
|------------------------|--------|-----|----------|
| Termination resistance | R_T | 50 | Ω |

Table 189 • M-LVDS AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|--|------------|-------------|----------|
| Measuring/trip point for data path | V_{TRIP} | Cross point | V |
| Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | R_{ENT} | 2K | Ω |
| Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ}) | C_{ENT} | 5 | pF |

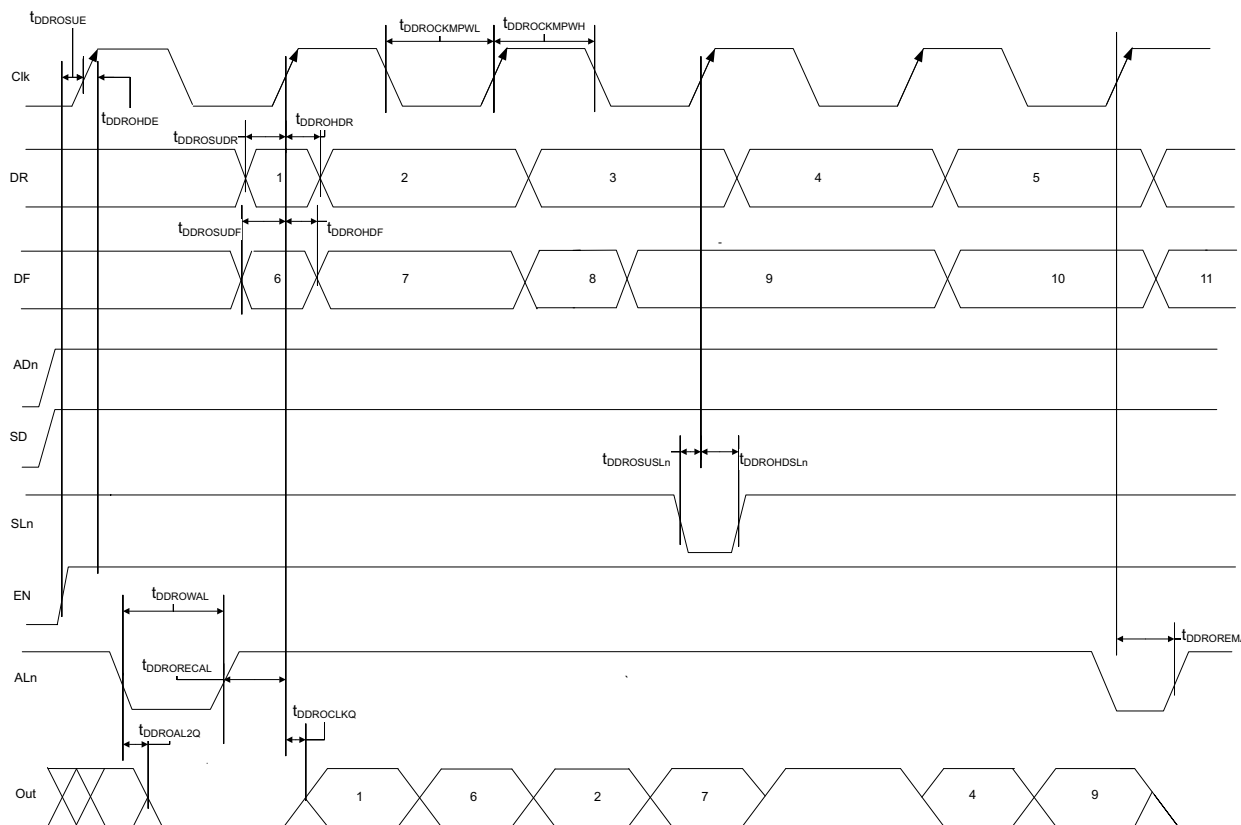
AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

| On-Die Termination (ODT) | T_{PY} | | Unit |
|--------------------------|----------|-------|------|
| | -1 | -Std | |
| None | 2.738 | 3.221 | ns |
| 100 | 2.735 | 3.218 | ns |

Figure 13 • Output DDR Timing Diagram



2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 222 • Output DDR Propagation Delays

| Symbol | Description | Measuring Nodes (from, to) | -1 | -Std | Unit |
|-----------------|--|----------------------------|-------|-------|------|
| $T_{DDROCLKQ}$ | Clock-to-out of DDR for output DDR | E, G | 0.263 | 0.309 | ns |
| $T_{DDROSUDF}$ | Data_F data setup for output DDR | F, E | 0.143 | 0.168 | ns |
| $T_{DDROSUDR}$ | Data_R data setup for output DDR | A, E | 0.19 | 0.223 | ns |
| $T_{DDROHDF}$ | Data_F data hold for output DDR | F, E | 0 | 0 | ns |
| $T_{DDROHDR}$ | Data_R data hold for output DDR | A, E | 0 | 0 | ns |
| $T_{DDROSUE}$ | Enable setup for input DDR | B, E | 0.419 | 0.493 | ns |
| T_{DDROHE} | Enable hold for input DDR | B, E | 0 | 0 | ns |
| $T_{DDROSUSLn}$ | Synchronous load setup for input DDR | D, E | 0.196 | 0.231 | ns |
| $T_{DDROHSLn}$ | Synchronous load hold for input DDR | D, E | 0 | 0 | ns |
| $T_{DDROAL2Q}$ | Asynchronous load-to-out for output DDR | C, G | 0.528 | 0.621 | ns |
| $T_{DDROEMAL}$ | Asynchronous load removal time for output DDR | C, E | 0 | 0 | ns |
| $T_{DDRORECAL}$ | Asynchronous load recovery time for output DDR | C, E | 0.034 | 0.04 | ns |

Table 222 • Output DDR Propagation Delays (continued)

| Symbol | Description | Measuring Nodes (from, to) | -1 | -Std | Unit |
|------------------|--|----------------------------|-------|-------|------|
| $T_{DDROWAL}$ | Asynchronous load minimum pulse width for output DDR | C, C | 0.304 | 0.357 | ns |
| $T_{DDROCKMPWH}$ | Clock minimum pulse width high for the output DDR | E, E | 0.075 | 0.088 | ns |
| $T_{DDROCKMPWL}$ | Clock minimum pulse width low for the output DDR | E, E | 0.159 | 0.187 | ns |

2.3.10 Logic Element Specifications

2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see [SmartFusion2 and IGLOO2 Macro Library Guide](#).

Figure 14 • LUT-4

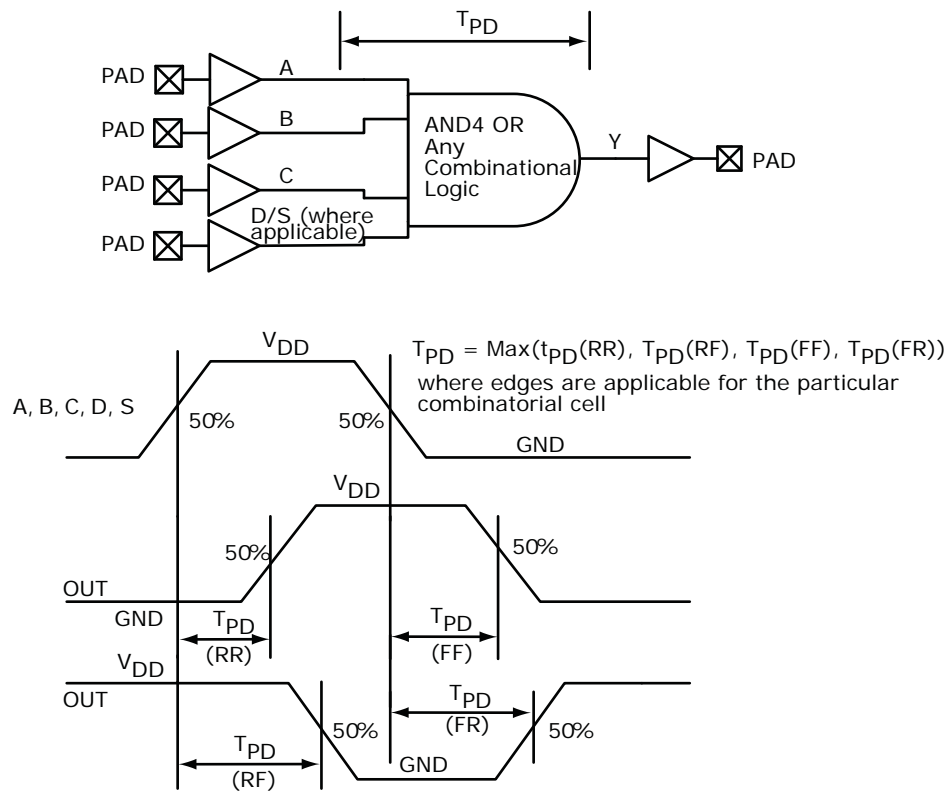


Table 240 • μ SRAM (RAM128x8) in 128 x 8 Mode (continued)

| Parameter | Symbol | -1 | | -Std | | Unit |
|---|----------------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | |
| Read address hold time in synchronous mode | T_{ADDRHD} | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | -0.778 | | -0.915 | | ns |
| Read enable setup time | T_{RDENSU} | 0.278 | | 0.327 | | ns |
| Read enable hold time | T_{RDENHD} | 0.057 | | 0.067 | | ns |
| Read block select setup time | T_{BLKSU} | 1.839 | | 2.163 | | ns |
| Read block select hold time | T_{BLKHD} | -0.65 | | -0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | T_{BLK2Q} | | 2.036 | | 2.396 | ns |
| Read asynchronous reset removal time (pipelined clock) | T_{RSTREM} | -0.023 | | -0.027 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | T_{RSTREC} | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | T_{R2Q} | | 0.835 | | 0.982 | ns |
| Read synchronous reset setup time | T_{SRSTSU} | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | T_{SRSTHD} | 0.061 | | 0.071 | | ns |
| Write clock period | T_{CCY} | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | T_{BLKCSU} | 0.404 | | 0.476 | | ns |
| Write block hold time | T_{BLKCHD} | 0.007 | | 0.008 | | ns |
| Write input data setup time | T_{DINCSU} | 0.115 | | 0.135 | | ns |
| Write input data hold time | T_{DINCHD} | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | T_{WECSU} | 0.397 | | 0.467 | | ns |
| Write enable hold time | T_{WECHD} | -0.026 | | -0.03 | | ns |
| Maximum frequency | F_{MAX} | | 250 | | 250 | MHz |

Table 242 • μ SRAM (RAM512x2) in 512 x 2 Mode (continued)

| Parameter | Symbol | -1 | | -Std | | Unit |
|--------------------------------------|----------------|-------|-----|-------|-----|------|
| | | Min | Max | Min | Max | |
| Write clock period | T_{CCY} | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | T_{BLKCSU} | 0.404 | | 0.476 | | ns |
| Write block hold time | T_{BLKCHD} | 0.007 | | 0.008 | | ns |
| Write input data setup time | T_{DINCSU} | 0.101 | | 0.118 | | ns |
| Write input data hold time | T_{DINCHD} | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | T_{WECSU} | 0.397 | | 0.467 | | ns |
| Write enable hold time | T_{WECHD} | -0.03 | | -0.03 | | ns |
| Maximum frequency | F_{MAX} | | 250 | | 250 | MHz |

The following table lists the μ SRAM in 1024 x 1 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 243 • μ SRAM (RAM1024x1) in 1024 x 1 Mode

| Parameter | Symbol | -1 | | -Std | | Unit |
|---|-----------------|-------|-------|-------|-------|------|
| | | Min | Max | Min | Max | |
| Read clock period | T_{CY} | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | T_{PLCY} | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | T_{CLK2Q} | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | | 1.78 | | 2.1 |
| Read address setup time in synchronous mode | T_{ADDRSU} | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | | 1.978 | | 2.327 | |
| Read address hold time in synchronous mode | T_{ADDRHD} | 0.137 | | 0.161 | | ns |
| Read address hold time in asynchronous mode | | | -0.6 | | -0.71 | |
| Read enable setup time | T_{RDENSU} | 0.278 | | 0.327 | | ns |
| Read enable hold time | T_{RDENHD} | 0.057 | | 0.067 | | ns |
| Read block select setup time | T_{BLKSU} | 1.839 | | 2.163 | | ns |
| Read block select hold time | T_{BLKHHD} | -0.65 | | -0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | T_{BLK2Q} | | 2.16 | | 2.54 | ns |
| Read asynchronous reset removal time (pipelined clock) | T_{RSTREM} | -0.02 | | -0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | | 0.046 | | 0.054 | |

Table 243 • μ SRAM (RAM1024x1) in 1024 x 1 Mode (continued)

| Parameter | Symbol | -1 | | -Std | | Unit |
|---|----------------|-------|------|-------|------|------|
| | | Min | Max | Min | Max | |
| Read asynchronous reset recovery time (pipelined clock) | T_{RSTREC} | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | T_{R2Q} | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | T_{SRSTSU} | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | T_{SRSTHD} | 0.061 | | 0.071 | | ns |
| Write clock period | T_{CCY} | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | T_{BLKCSU} | 0.404 | | 0.476 | | ns |
| Write block hold time | T_{BLKCHD} | 0.007 | | 0.008 | | ns |
| Write input data setup time | T_{DINCSU} | 0.003 | | 0.004 | | ns |
| Write input data hold time | T_{DINCHD} | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | T_{WECSU} | 0.397 | | 0.467 | | ns |
| Write enable hold time | T_{WECHD} | -0.03 | | -0.03 | | ns |
| Maximum frequency | F_{MAX} | | 250 | | 250 | MHz |

2.3.13 Programming Times

The following tables list the programming times in typical conditions when $T_J = 25\text{ }^\circ\text{C}$, $V_{DD} = 1.2\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 244 • JTAG Programming (Fabric Only)

| M2S/M2GL | | | | |
|----------|------------------|---------|--------|------|
| Device | Image size Bytes | Program | Verify | Unit |
| 005 | 302672 | 22 | 10 | Sec |
| 010 | 568784 | 28 | 18 | Sec |
| 025 | 1223504 | 51 | 26 | Sec |
| 050 | 2424832 | 66 | 54 | Sec |
| 060 | 2418896 | 77 | 54 | Sec |
| 090 | 3645968 | 113 | 126 | Sec |
| 150 | 6139184 | 155 | 193 | Sec |

Table 245 • JTAG Programming (eNVM Only)

| M2S/M2GL | | | | |
|-----------------|-------------------------|----------------|---------------|-------------|
| Device | Image size Bytes | Program | Verify | Unit |
| 005 | 137536 | 39 | 4 | Sec |
| 010 | 274816 | 78 | 9 | Sec |
| 025 | 274816 | 78 | 9 | Sec |
| 050 | 278528 | 84 | 8 | Sec |
| 060 | 268480 | 76 | 8 | Sec |
| 090 | 544496 | 154 | 15 | Sec |
| 150 | 544496 | 155 | 15 | Sec |

Table 246 • JTAG Programming (Fabric and eNVM)

| M2S/M2GL | | | | |
|-----------------|-------------------------|----------------|---------------|-------------|
| Device | Image size Bytes | Program | Verify | Unit |
| 005 | 439296 | 59 | 11 | Sec |
| 010 | 842688 | 107 | 20 | Sec |
| 025 | 1497408 | 120 | 35 | Sec |
| 050 | 2695168 | 162 | 59 | Sec |
| 060 | 2686464 | 158 | 70 | Sec |
| 090 | 4190208 | 266 | 147 | Sec |
| 150 | 6682768 | 316 | 231 | Sec |

Table 247 • 2 Step IAP Programming (Fabric Only)

| M2S/M2GL | | | | | |
|-----------------|-------------------------|---------------------|----------------|---------------|-------------|
| Device | Image size Bytes | Authenticate | Program | Verify | Unit |
| 005 | 302672 | 4 | 17 | 6 | Sec |
| 010 | 568784 | 7 | 23 | 12 | Sec |
| 025 | 1223504 | 14 | 33 | 23 | Sec |
| 050 | 2424832 | 29 | 52 | 40 | Sec |
| 060 | 2418896 | 39 | 61 | 50 | Sec |
| 090 | 3645968 | 60 | 84 | 73 | Sec |
| 150 | 6139184 | 100 | 132 | 120 | Sec |

Table 265 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)

| M2S/M2GL Device | Auto Programming | | | Unit |
|-----------------|------------------|---------------|---------------|------|
| | 100 kHz | 25 MHz | 12.5 MHz | |
| 005 | 69 | 49 | 50 | Sec |
| 010 | 99 | 57 | 57 | Sec |
| 025 | 150 | 64 | 63 | Sec |
| 050 | 55 ¹ | Not Supported | Not Supported | Sec |
| 060 | 313 | 105 | 104 | Sec |
| 090 | 449 | 131 | 130 | Sec |
| 150 | 730 | 179 | 183 | Sec |

1. Auto programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

Table 266 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)

| M2S/M2GL Device | Auto Programming | | | Unit |
|-----------------|------------------|---------------|---------------|------|
| | 100 kHz | 25 MHz | 12.5 MHz | |
| 005 | 63 | 70 | 71 | Sec |
| 010 | 108 | 109 | 109 | Sec |
| 025 | 109 | 107 | 108 | Sec |
| 050 | 107 | Not Supported | Not Supported | Sec |
| 060 | 100 | 108 | 108 | Sec |
| 090 | 176 | 184 | 184 | Sec |
| 150 | 183 | 183 | 183 | Sec |

Table 267 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)

| M2S/M2GL Device | Auto Programming | | | Unit |
|-----------------|------------------|---------------|---------------|------|
| | 100 kHz | 25 MHz | 12.5 MHz | |
| 005 | 109 | 89 | 88 | Sec |
| 010 | 183 | 135 | 135 | Sec |
| 025 | 251 | 142 | 143 | Sec |
| 050 | 134 | Not Supported | Not Supported | Sec |
| 060 | 390 | 183 | 180 | Sec |
| 090 | 604 | 283 | 282 | Sec |
| 150 | 889 | 331 | 332 | Sec |

2.3.22 JTAG

Table 284 • JTAG 1532 for 005, 010, 025, and 050 Devices

| Parameter | Symbol | 005 | | 010 | | 025 | | 050 | | Unit |
|-----------------------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | -1 | -Std | |
| Clock to Q (data out) | T_{TCK2Q} | 7.47 | 8.79 | 7.73 | 9.09 | 7.75 | 9.12 | 7.89 | 9.28 | ns |
| Reset to Q (data out) | T_{RSTB2Q} | 7.65 | 9 | 6.43 | 7.56 | 6.13 | 7.21 | 7.40 | 8.70 | ns |
| Test data input setup time | T_{DISU} | -1.05 | -0.89 | -0.69 | -0.59 | -0.67 | -0.57 | -0.30 | -0.25 | ns |
| Test data input hold time | T_{DIHD} | 2.38 | 2.8 | 2.38 | 2.8 | 2.42 | 2.85 | 2.09 | 2.45 | ns |
| Test mode select setup time | T_{TMSSU} | -0.73 | -0.62 | -1.03 | -1.21 | -1.1 | -0.94 | 0.28 | 0.33 | ns |
| Test mode select hold time | T_{TMDHD} | 1.36 | 1.6 | 1.43 | 1.68 | 1.93 | 2.27 | 0.16 | 0.19 | ns |
| ResetB removal time | $T_{TRSTREM}$ | -0.77 | -0.65 | -1.08 | -0.92 | -1.33 | -1.13 | -0.45 | -0.38 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | -0.76 | -0.65 | -1.07 | -0.91 | -1.34 | -1.14 | -0.45 | -0.38 | ns |
| TCK maximum frequency | F_{TCKMAX} | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | 25.00 | 21.25 | MHz |

Table 285 • JTAG 1532 for 060, 090, and 150 Devices

| Parameter | Symbol | 060 | | 090 | | 150 | | Unit |
|-----------------------------|---------------|-------|-------|-------|-------|-------|-------|------|
| | | -1 | -Std | -1 | -Std | -1 | -Std | |
| Clock to Q (data out) | T_{TCK2Q} | 8.38 | 9.86 | 8.96 | 10.54 | 8.66 | 10.19 | ns |
| Reset to Q (data out) | T_{RSTB2Q} | 8.54 | 10.04 | 7.75 | 9.12 | 8.79 | 10.34 | ns |
| Test data input setup time | T_{DISU} | -1.18 | -1 | -1.31 | -1.11 | -0.96 | -0.82 | ns |
| Test data input hold time | T_{DIHD} | 2.52 | 2.97 | 2.68 | 3.15 | 2.57 | 3.02 | ns |
| Test mode select setup time | T_{TMSSU} | -0.97 | -0.83 | -1.02 | -0.87 | -0.53 | -0.45 | ns |
| Test mode select hold time | T_{TMDHD} | 1.7 | 2 | 1.67 | 1.96 | 1.02 | 1.2 | ns |
| ResetB removal time | $T_{TRSTREM}$ | -1.21 | -1.03 | -0.76 | -0.65 | -1.03 | -0.88 | ns |
| ResetB recovery time | $T_{TRSTREC}$ | -1.21 | -1.03 | -0.77 | -0.65 | -1.03 | -0.88 | ns |
| TCK maximum frequency | F_{TCKMAX} | 25 | 21.25 | 25 | 21.25 | 25 | 21.25 | MHz |

2.3.23 System Controller SPI Characteristics

Table 293 • Flash*Freeze Entry and Exit Times (continued)

| Parameter | Symbol | Entry/Exit Timing FCLK = 100MHz | | | Entry/Exit Timing FCLK = 3 MHz | |
|--|----------|--|-----|-------------|-----------------------------------|--|
| | | 005, 010, 025, 060, 090, and 150 | 050 | All Devices | Unit | Conditions |
| Exit time with respect to the fabric PLL lock ¹ | TFF_EXIT | 1.5 | 1.5 | 1.5 | ms | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 1.5 | 1.5 | 1.5 | ms | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |
| Exit time with respect to the fabric buffer output | TFF_EXIT | 21 | 15 | 21 | μs | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 65 | 55 | 65 | μs | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |

1. PLL Lock Delay set to 1024 cycles (default).

2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 294 • DDR Memory Interface Characteristics

| Standard | Supported Data Rate | | Unit |
|----------|---------------------|-----|------|
| | Min | Max | |
| DDR3 | 667 | 667 | Mbps |
| DDR2 | 667 | 667 | Mbps |
| LPDDR | 50 | 400 | Mbps |

2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 295 • SFP Transceiver Electrical Characteristics

| Pin | Direction | Differential Peak-Peak Voltage | | Unit |
|--------------------|-----------|--------------------------------|------|------|
| | | Min | Max | |
| RD+/- ¹ | Output | 1600 | 2400 | mV |
| TD+/- ² | Input | 350 | 2400 | mV |

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 299 • SerDes Reference Clock AC Specifications

| Parameter | Symbol | Min | Max | Unit |
|---------------------------------|---------------|------|------|------|
| Reference clock frequency | F_{REFCLK} | 100 | 160 | MHz |
| Reference clock rise time | T_{RISE} | 0.6 | 4 | V/ns |
| Reference clock fall time | T_{FALL} | 0.6 | 4 | V/ns |
| Reference clock duty cycle | T_{CYC} | 40 | 60 | % |
| Reference clock mismatch | $M_{MREFCLK}$ | -300 | 300 | ppm |
| Reference spread spectrum clock | SSC_{ref} | 0 | 5000 | ppm |

Table 300 • HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------|-------|-----|-------|------|
| Recommended DC Operating Conditions | | | | | |
| Supply voltage | V_{DDI} | 2.375 | 2.5 | 2.625 | V |
| HCSL DC Input Voltage Specification | | | | | |
| DC Input voltage | V_I | 0 | | 2.625 | V |
| HCSL Differential Voltage Specification | | | | | |
| Input common mode voltage | V_{ICM} | 0.05 | | 2.4 | V |
| Input differential voltage | V_{IDIFF} | 100 | | 1100 | mV |

Table 301 • HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------------|-----------|-----|-----|-----|----------|
| HCSL AC Specifications | | | | | |
| Maximum data rate (for MSIO I/O bank) | F_{MAX} | | | 350 | Mbps |
| HCSL Impedance Specifications | | | | | |
| Termination resistance | R_t | | 100 | | Ω |

2.3.31 SmartFusion2 Specifications

2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 302 • Maximum Frequency for MSS Main Clock

| Symbol | Description | -1 | -Std | Unit |
|--------|--|-----|------|------|
| M3_CLK | Maximum frequency for the MSS main clock | 166 | 142 | MHz |

2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see [Figure 21](#), page 125.

The following table lists the I²C characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Table 303 • I²C Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|-----------------------|-----------------------|--------|--------|---------------|--|
| Input low voltage | V_{IL} | -0.3 | | 0.8 | V | See Single-Ended I/O Standards , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive. |
| Input high voltage | V_{IH} | 2 | | 3.45 | V | See Single-Ended I/O Standards , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive. |
| Hysteresis of schmitt triggered inputs for $V_{DDI} > 2\text{ V}$ | V_{HYS} | $0.05 \times V_{DDI}$ | | | V | See Table 28 , page 23 for more information. |
| Input current high | I_{IL} | | | 10 | μA | See Single-Ended I/O Standards , page 24 for more information. |
| Input current low | I_{IH} | | | 10 | μA | See Single-Ended I/O Standards , page 24 for more information. |
| Input rise time | T_{ir} | | | 1000 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Input fall time | T_{if} | | | 300 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$ | V_{OL} | | | 0.4 | V | See Single-Ended I/O Standards , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive. |
| Pin capacitance | C_{in} | | | 10 | pF | $V_{IN} = 0$, $f = 1.0\text{ MHz}$ |
| Output fall time from V_{IHMin} to V_{ILMax}^1 | t_{OF}^1 | | 21.04 | | ns | V_{IHmin} to V_{ILMax} , $C_{LOAD} = 400\text{ pF}$ |
| | | | 5.556 | | ns | V_{IHmin} to V_{ILMax} , $C_{LOAD} = 100\text{ pF}$ |
| Output rise time from V_{ILMax} to V_{IHMin}^1 | t_{OR}^1 | | 19.887 | | ns | V_{ILMax} to V_{IHmin} , $C_{LOAD} = 400\text{ pF}$ |
| | | | 5.218 | | ns | V_{ILMax} to V_{IHmin} , $C_{LOAD} = 100\text{ pF}$ |
| Output buffer maximum pull-down resistance ^{2,3} | $R_{pull-up}^{2,3}$ | | | 50 | Ω | |
| Output buffer maximum pull-up resistance ^{2,4} | $R_{pull-down}^{2,4}$ | | | 131.25 | Ω | |

Table 310 • SPI Characteristics for All Devices (continued)

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|--|--|-----------------------------|-------|-----|------|--|
| sp2 | SPI_[0 1]_CLK minimum pulse width high | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0 1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp3 | SPI_[0 1]_CLK minimum pulse width low | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0 1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0 1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0 1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0 1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp4 | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) ¹ | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C |
| sp5 | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) ¹ | | 2.906 | | ns | I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C |
| SPI master configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6m | SPI_[0 1]_DO setup time ² | (SPI_x_CLK_period/2) – 8.0 | | | ns | |
| sp7m | SPI_[0 1]_DO hold time ² | (SPI_x_CLK_period/2) – 2.5 | | | ns | |
| sp8m | SPI_[0 1]_DI setup time ² | 12 | | | ns | |
| sp9m | SPI_[0 1]_DI hold time ² | 2.5 | | | ns | |
| SPI slave configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6s | SPI_[0 1]_DO setup time ² | (SPI_x_CLK_period/2) – 17.0 | | | ns | |
| sp7s | SPI_[0 1]_DO hold time ² | (SPI_x_CLK_period/2) + 3.0 | | | ns | |
| sp8s | SPI_[0 1]_DI setup time ² | 2 | | | ns | |
| sp9s | SPI_[0 1]_DI hold time ² | 7 | | | ns | |