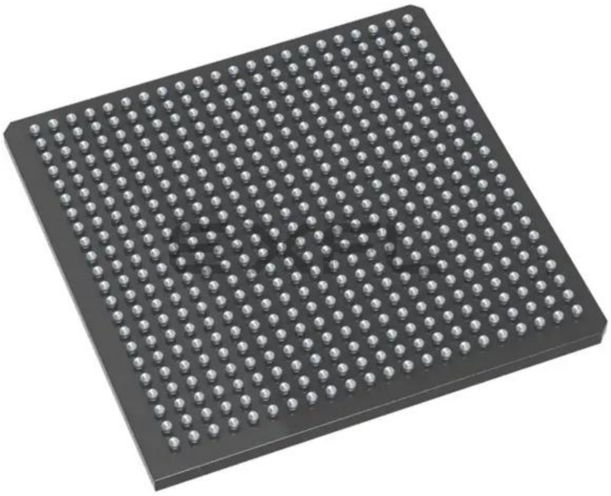

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 150K Logic Modules
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s150ts-1fcvg484

Contents

The following table lists the embedded operating flash limits.

Table 6 • **Embedded Operating Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Commercial	Embedded flash	Min T_J = 0 °C Max T_J = 85 °C	Min T_J = 0 °C Max T_J = 85 °C	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min T_J = 0 °C Max T_J = 85 °C	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years
Industrial	Embedded flash	Min T_J = –40 °C Max T_J = 100 °C	Min T_J = –40 °C Max T_J = 100 °C	< 1000 cycles per page, up to two million cycles per eNVM array	20 years
			Min T_J = –40 °C Max T_J = 100 °C	< 10000 cycles per page, up to 20 million cycles per eNVM array	10 years

Note: If your product qualification requires accelerated programming cycles, see *Microsemi SoC Products Quality and Reliability Report* about recommended methodologies.

Table 7 • **Device Storage Temperature and Retention**

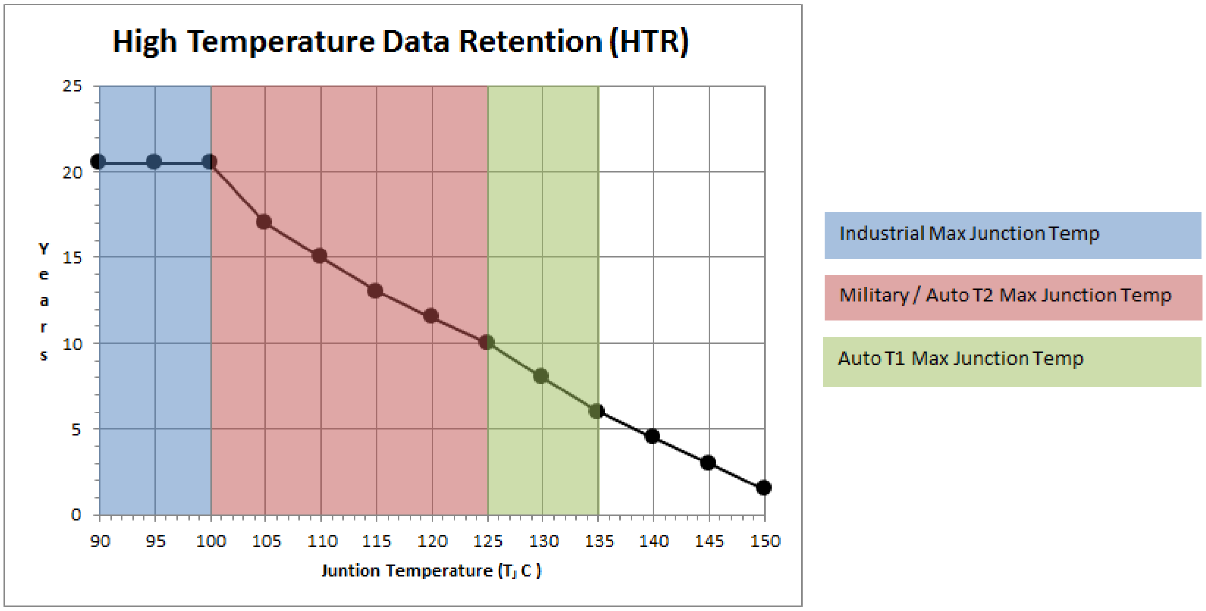
Product Grade	Storage Temperature (Tstg)	Retention
Commercial	Min T_J = 0 °C Max T_J = 85 °C	20 years
Industrial	Min T_J = –40 °C Max T_J = 100 °C	20 years

Table 8 • **High Temperature Data Retention (HTR) Lifetime**

T_J (C)	HTR Lifetime[1] (yrs)
90	20.5
95	20.5
100	20.5
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

1. HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

Figure 1 • **High Temperature Data Retention (HTR)**



2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to V_{CCI} + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

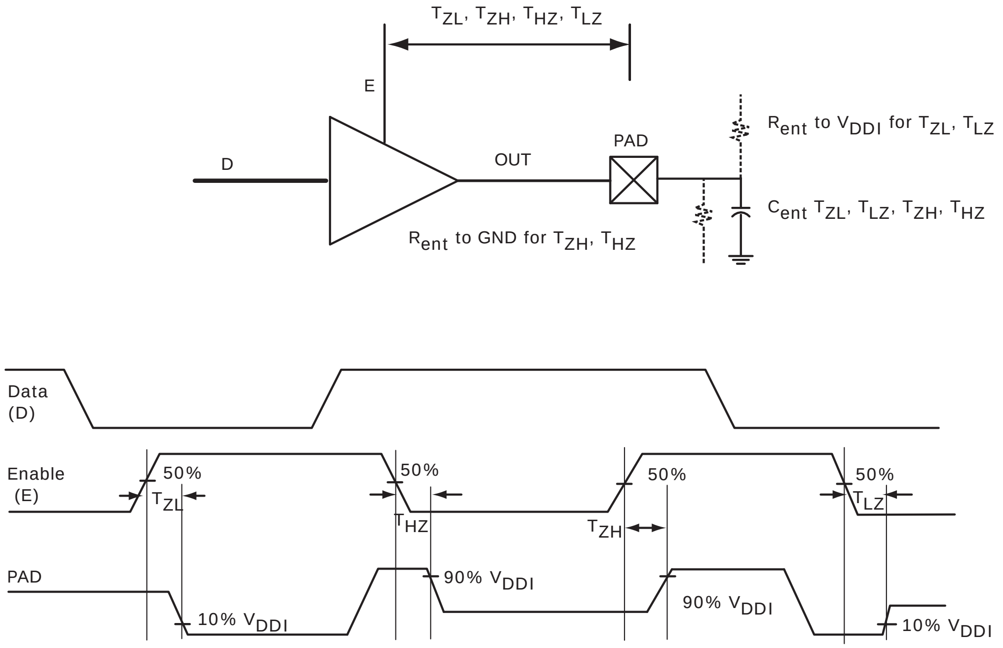
$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • **Tristate Buffer for Enable Path Test Point**



2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVCMOS 3.3 V	600			Mbps
LVCMOS 2.5 V	410	420	400	Mbps
LVCMOS 1.8 V	295	400	400	Mbps
LVCMOS 1.5 V	160	220	235	Mbps
LVCMOS 1.2 V	120	160	200	Mbps
LPDDR-LVCMOS 1.8 V mode			400	Mbps

Table 22 • **Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			200	MHz
HSTL1.5 V			200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V			334	MHz
SSTL 1.5 V			334	MHz

Table 23 • **Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	450		MHz
LVDS 3.3 V	267.5		MHz
LVDS 2.5 V	267.5	350	MHz
RSDS	260	350	MHz
BLVDS	250		MHz
MLVDS	250		MHz
Mini-LVDS	260	350	MHz

Table 43 • **LVCMOS 2.5 V AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	1.2	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ωσ
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 44 • **LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	**MSIOD I/O Bank**	**DDRIO I/O Bank (With Software Default Fixed Code)**	**Min**	**Max**		
2 mA	2 mA	2 mA	V_{DDI} – 0.4	0.4	2	2
4 mA	4 mA	4 mA	V_{DDI} – 0.4	0.4	4	4
6 mA	6 mA	6 mA	V_{DDI} – 0.4	0.4	6	6
8 mA	8 mA	8 mA	V_{DDI} – 0.4	0.4	8	8
12 mA	12 mA	12 mA	V_{DDI} – 0.4	0.4	12	12
16 mA		16 mA	V_{DDI} – 0.4	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 45 • **LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

	On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
		–1	**–Std**	**–1**	**–Std**	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.29	2.694	2.305	2.712	ns

Table 46 • **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns

2.3.6.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 103 • **DDR1/SSTL2 DC Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V
Termination voltage	V_{TT}	1.164	1.250	1.339	V
Input reference voltage	V_{REF}	1.164	1.250	1.339	V

Table 104 • **DDR1/SSTL2 DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	V_{REF} + 0.15	2.625	V
DC input logic low	V_{IL} (DC)	–0.3	VREF – 0.15	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

[1] See Table 24, page 22.

Table 105 • **DDR1/SSTL2 DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
SSTL2 Class I (DDR Reduced Drive)				
DC output logic high	V_{OH}	V_{TT} + 0.608		V
DC output logic low	V_{OL}		V_{TT} – 0.608	V
Output minimum source DC current	I_{OH} at V_{OH}	8.1		mA
Output minimum sink current	I_{OL} at V_{OL}	–8.1		mA
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Bank Only				
DC output logic high	V_{OH}	V_{TT} + 0.81		V
DC output logic low	V_{OL}		V_{TT} – 0.81	V
Output minimum source DC current	I_{OH} at V_{OH}	16.2		mA
Output minimum sink current	I_{OL} at V_{OL}	–16.2		mA

Table 106 • **DDR1/SSTL2 DC Differential Voltage Specification**

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.3	V

Table 162 • LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 163 • LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	V_{OD}	250	350	450	mV
Output common mode voltage	V_{OCM}	1.125	1.25	1.375	V
Input common mode voltage	V_{ICM}	0.05	1.25	2.35	V
Input differential voltage	V_{ID}	100	350	600	mV

Table 164 • LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	535	Mbps	AC loading: 12 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	D_{MAX}	620	Mbps	AC loading: 10 pF / 100 Ω differential load
		700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 165 • LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Max	Unit
Termination resistance	RT	100		Ω

Table 166 • LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF

LVDS25 AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.774	3.263	ns
100	2.775	3.264	ns

Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY} –1	T_{PY} –Std	Unit
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T_{DP} –1	T_{DP} –Std	T_{ZL} –1	T_{ZL} –Std	T_{ZH} –1	T_{ZH} –Std	T_{HZ} –1	T_{HZ} –Std	T_{LZ} –1	T_{LZ} –Std	Unit
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 193 • Mini-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 194 • Mini-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC Input voltage	V_I	0	2.925	V

Table 195 • Mini-LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 196 • Mini-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V_{OD}	300	600	mV
Output common mode voltage	V_{OCM}	1	1.4	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	100	600	mV

Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 198 • Mini-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	100	Ω

Table 199 • Mini-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 200 • Mini-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

	T_{PY}		
On-Die Termination (ODT)	–1	–Std	Unit
None	2.855	3.359	ns
100	2.85	3.353	ns
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 201 • Mini-LVDS AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)

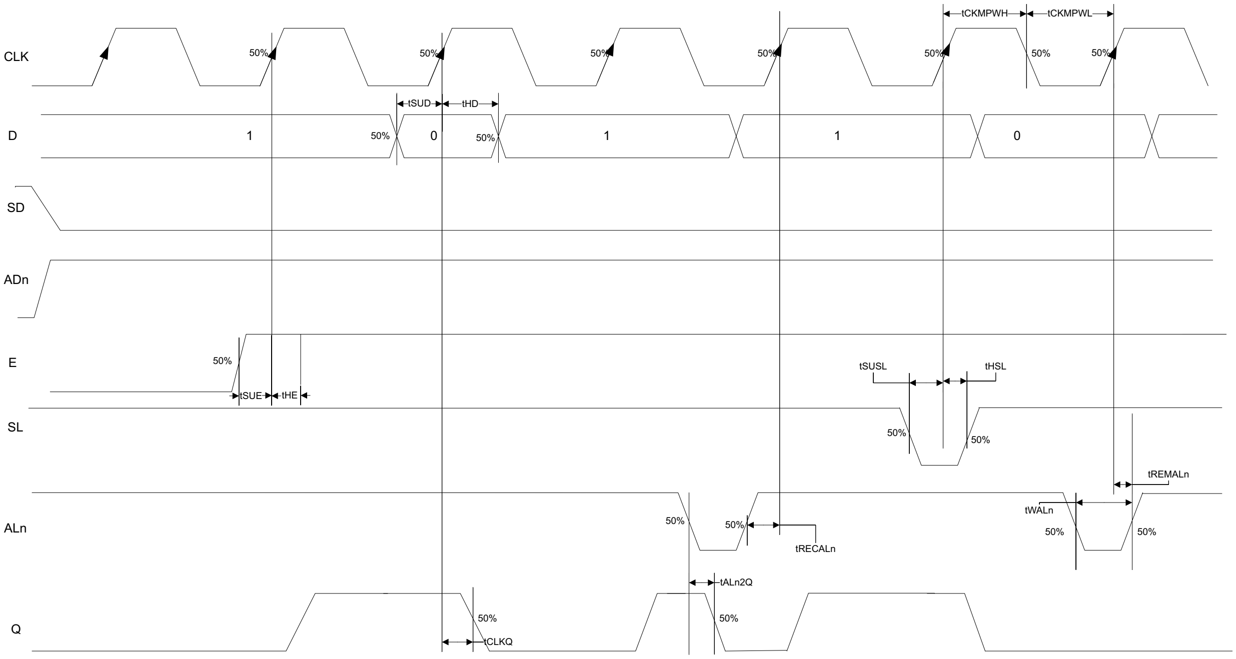
T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
2.097	2.467	2.308	2.715	2.296	2.701	1.964	2.31	1.949	2.293	ns

Table 202 • Mini-LVDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
No pre-emphasis	1.614	1.899	1.562	1.837	1.553	1.826	1.593	1.874	1.578	1.856	ns
Min pre-emphasis	1.604	1.887	1.745	2.053	1.731	2.036	1.892	2.225	1.861	2.189	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

Figure 16 • **Sequential Module Timing Diagram**



2.3.10.3.1 Timing Characteristics

The following table lists the register delays in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 224 • **Register Delays**

Parameter	Symbol	–1	–Std	Unit
Clock-to-Q of the core register	T_{CLKQ}	0.108	0.127	ns
Data setup time for the core register	T_{SUD}	0.254	0.298	ns
Data hold time for the core register	T_{HD}	0	0	ns
Enable setup time for the core register	T_{SUE}	0.335	0.394	ns
Enable hold time for the core register	T_{HE}	0	0	ns
Synchronous load setup time for the core register	T_{SUSL}	0.335	0.394	ns
Synchronous load hold time for the core register	T_{HSL}	0	0	ns
Asynchronous Clear-to-Q of the core register (ADn = 1)	T_{ALN2Q}	0.473	0.556	ns
Asynchronous preset-to-Q of the core register (ADn = 0)		0.451	0.531	ns
Asynchronous load removal time for the core register	T_{REMALN}	0	0	ns
Asynchronous load recovery time for the core register	T_{RECALN}	0.353	0.415	ns
Asynchronous load minimum pulse width for the core register	T_{WALN}	0.266	0.313	ns
Clock minimum pulse width high for the core register	T_{CKMPWH}	0.065	0.077	ns
Clock minimum pulse width low for the core register	T_{CKMPWL}	0.139	0.164	ns

The following table lists the 010 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 229 • 010 Device Global Resource

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.626	0.669	0.627	0.668	ns
Input high delay for global clock	T_{RCKH}	1.112	1.182	1.308	1.393	ns
Maximum skew for global clock	T_{RCKSW}		0.07		0.085	ns

The following table lists the 005 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 230 • 005 Device Global Resource

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.625	0.66	0.628	0.66	ns
Input high delay for global clock	T_{RCKH}	1.126	1.187	1.325	1.397	ns
Maximum skew for global clock	T_{RCKSW}		0.061		0.072	ns

2.3.12 FPGA Fabric SRAM

See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 1K × 18 in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.334		0.393	ns
Read access time without pipeline register			2.273		2.674	ns
Access time with feed-through write timing			1.529		1.799	ns
Address setup time	T_{ADDRSU}	0.441		0.519		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.341		0.401		ns
Data hold time	T_{DHD}	0.107		0.126		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns

Table 237 • **μSRAM (RAM64x18) in 64 × 18 Mode *(continued)***

Parameter	Symbol	–1 Min	–1 Max	–Std Min	–Std Max	Unit
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μSRAM in 64 × 16 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 238 • **μSRAM (RAM64x16) in 64 × 16 Mode**

Parameter	Symbol	–1 Min	–1 Max	–Std Min	–Std Max	Unit
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

Table 239* • µSRAM (RAM128x9) in 128 × 9 Mode *(continued)

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the µSRAM in 128 × 8 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

***Table 240* • µSRAM (RAM128x8) in 128 × 8 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns

2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 288 • **Power-up to Functional Times for SmartFusion2**

				Maximum Power-up to Functional Time for SmartFusion2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESET_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Table 291 • **DEVRST_N to Functional Times for SmartFusion2 *(continued)***

				Maximum Power-up to Functional Time for SmartFusion2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	233	289	216	213	237	234	219
$T_{DEVRST2MSSRST}$	DEVRST_N	MSS_RESET_N_M2F	V_{DD} at its minimum threshold level to MSS	702	765	712	688	636	630	866
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

Figure 19 • **DEVRST_N to Functional Timing Diagram for SmartFusion2**

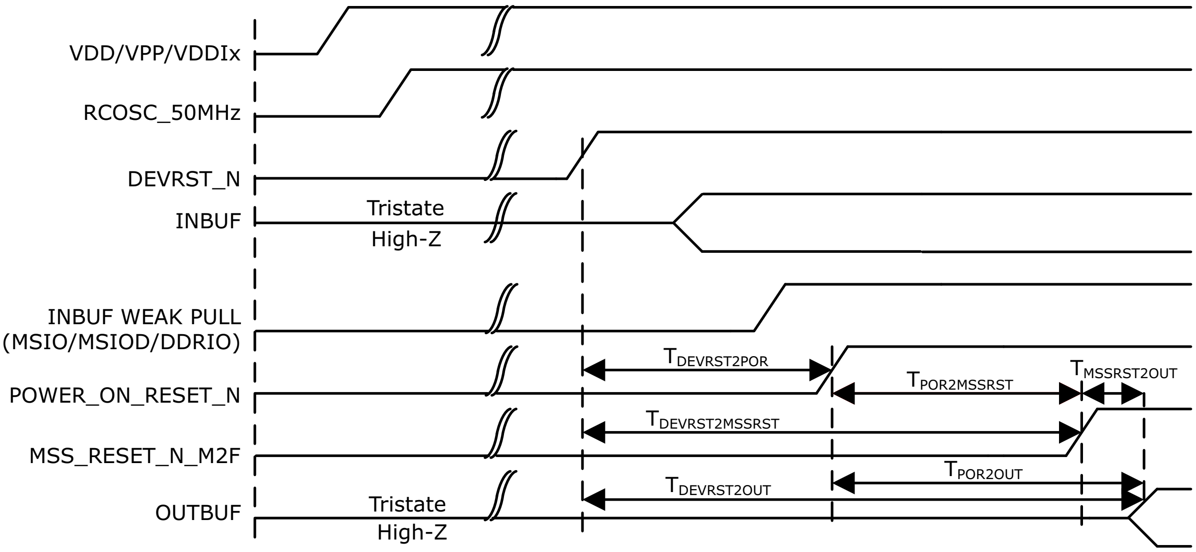
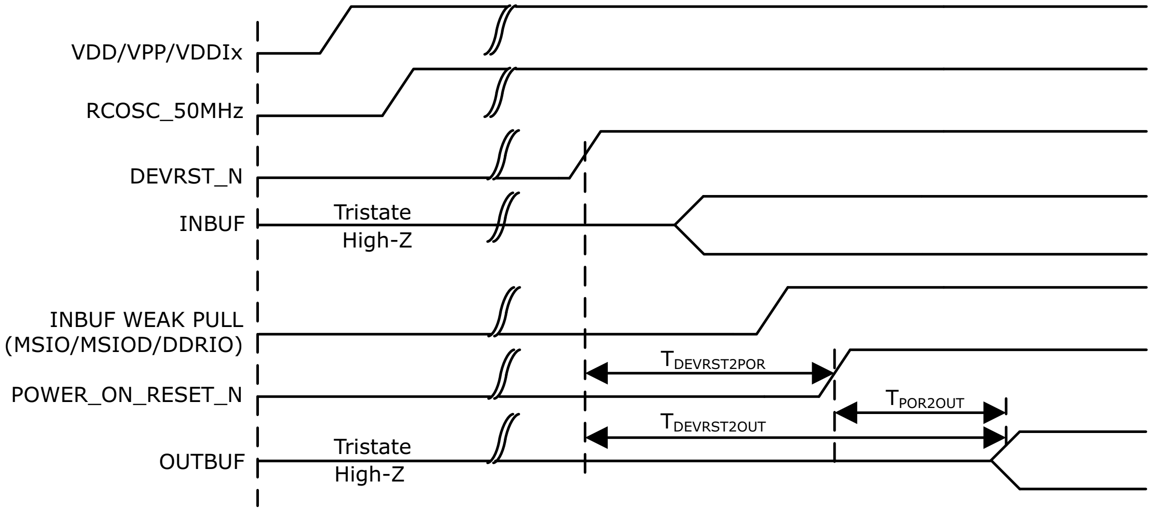


Figure 20 • **DEVRST_N to Functional Timing Diagram for IGLOO2**



2.3.27 Flash*Freeze Timing Characteristics

The following table lists the Flash*Freeze entry and exit times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 293 • **Flash*Freeze Entry and Exit Times**

		Entry/Exit Timing FCLK = 100MHz		**Entry/Exit Timing FCLK = 3 MHz**		
Parameter	**Symbol**	**005, 010, 025, 060, 090, and 150**	**050**	**All Devices**	**Unit**	**Conditions**
Entry time	TFF_ENTRY	160	150	320	µs	eNVM and MSS/HPMS PLL = ON
		215	200	430	µs	eNVM and MSS/HPMS PLL= OFF
Exit time with respect to the MSS PLL Lock	TFF_EXIT	100	100	140	µs	eNVM and MSS/HPMS PLL = ON during F*F
		136	120	190	µs	eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit
		200	200	285	µs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
		200	200	285	µs	eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit

Table 293 • **Flash*Freeze Entry and Exit Times *(continued)***

		Entry/Exit Timing FCLK = 100MHz		Entry/Exit Timing FCLK = 3 MHz		
Parameter	**Symbol**	**005, 010, 025, 060, 090, and 150**	**050**	**All Devices**	**Unit**	**Conditions**
Exit time with respect to the fabric PLL lock[1]	TFF_EXIT	1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = ON during F*F
		1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
Exit time with respect to the fabric buffer output	TFF_EXIT	21	15	21	µs	eNVM and MSS/HPMS PLL = ON during F*F
		65	55	65	µs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit

1. PLL Lock Delay set to 1024 cycles (default).

2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 294 • **DDR Memory Interface Characteristics**

	Supported Data Rate		
Standard	**Min**	**Max**	**Unit**
DDR3	667	667	Mbps
DDR2	667	667	Mbps
LPDDR	50	400	Mbps

2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 295 • **SFP Transceiver Electrical Characteristics**

		Differential Peak-Peak Voltage		
Pin	**Direction**	**Min**	**Max**	**Unit**
RD+/-[1]	Output	1600	2400	mV
TD+/-[2]	Input	350	2400	mV

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 296 • **Transmitter Parameters**

Symbol	Description	Min	Max	Unit
VTX-DIFF-PP	Differential swing (2.5 Gbps, 5.0 Gbps)	0.8	1.2	V
VTX-CM-AC-P	Output common mode voltage (2.5 Gbps)		20	mV
VTX-CM-AC-PP	Output common mode voltage (5.0 Gbps)		100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%, 2.5 Gbps)	0.125		UI
	Rise and fall time (20% to 80%, 5.0 Gbps)	0.15		UI
ZTX-DIFF-DC	Output impedance–differential	80	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SerDes block (2.5 Gbps)		500 ps + 2 UI	ps
	Lane-to-lane TX skew within a SerDes block (5.0 Gbps)		500 ps + 4 UI	ps
RLTX-DIFF	Return loss differential mode (2.5 Gbps)	–10		dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10		dB
	1.25 GHz to 2.5 GHz	–8		dB
RLTX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6		dB
TX-LOCK-RST	Transmit PLL lock time from reset		10	µs
VTX-AMP	100 mV setting	90	150	mV
	400 mV setting	320	480	mV
	800 mV setting	660	940	mV
	1200 mV setting	950	1400	mV

Table 303 • **I2C Characteristics *(continued)***

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	D_{MAX}			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	T_{FILT}		50		ns	Fast mode

1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDIx}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
3. R(PULL-DOWN-MAX) = (VOLspec)/IOLspec.
4. R(PULL-UP-MAX) = (VDDImax–VOHspec)/IOHspec.

The following table lists the I^2C switching characteristics in worst-case industrial conditions when $T_J = 100$ °C, $V_{DD} = 1.14$ V

Table 304 • **I2C Switching Characteristics**

		–1	Std	
Parameter	**Symbol**	**Min**	**Min**	**Unit**
Low period of I2C_x_SCL	T_{LOW}	1	1	PCLK cycles
High period of I2C_x_SCL	T_{HIGH}	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

Figure 21 • **I^2C Timing Parameter Definition**