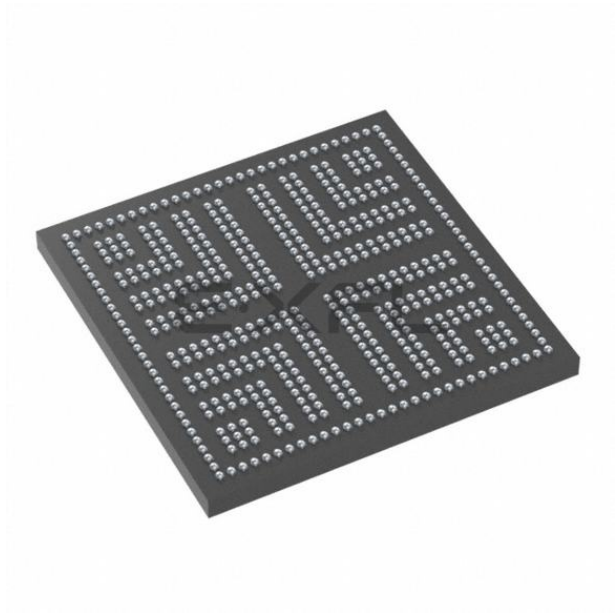

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 512KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 150K Logic Modules |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 536-LFBGA, CSPBGA |
| Supplier Device Package | 536-CSPBGA (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s150ts-fcs536i |

## 1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

## 1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

## 1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

## 2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:
http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga
http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview

## 2.3 Electrical Specifications

### 2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

***Table 3 •*** **Absolute Maximum Ratings**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC core supply voltage. Must always power this pin. | $V_{DD}$ | –0.3 | 1.32 | V |
| Power supply for charge pumps (for normal operation and programming). Must always power this pin. | $V_{PP}$ | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | MSS_MDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | HPMS_MDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for FDDR PLL | FDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | PLL0_PLL1_MSS_MDDR_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | PLL0_PLL1_HPMS_MDDR_VDDA | –0.3 | 3.63 | V |
| Analog power pad for PLL0–5 | CCC_XX[01]_PLL_VDDA | –0.3 | 3.63 | V |
| High supply voltage for PLL SerDes[01] | SERDES_[01]_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply. | SERDES_[01]_L[0123]_VDDAPLL | –0.3 | 2.75 | V |
| TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply. | SERDES_[01]_L[0123]_VDDAIO | –0.3 | 1.32 | V |
| PCIe/PCS power supply | SERDES_[01]_VDD | –0.3 | 1.32 | V |
| DC FPGA I/O buffer supply voltage for MSIO I/O bank | $V_{DDIx}$ | –0.3 | 3.63 | V |
| DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks | $V_{DDIx}$ | –0.3 | 2.75 | V |
| I/O Input voltage for MSIO I/O bank | $V_I$ | –0.3 | 3.63 | V |
| I/O Input voltage for MSIOD/DDRIO I/O bank | $V_I$ | –0.3 | 2.75 | V |
| Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$. | $V_{PPNVM}$ | –0.3 | 3.63 | V |
| Storage temperature[1] | $T_{STG}$ | –65 | 150 | °C |
| Junction temperature | $T_J$ | –55 | 135 | °C |

***Table 15 •*** **Inrush Currents at Power up, –40 °C <= $T_J$ <= 100 °C – Typical Process**

| Power Supplies | Voltage (V) | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | 1.26 | 25 | 32 | 38 | 48 | 45 | 77 | 109 | mA |
| $V_{PP}$ | 3.46 | 33 | 49 | 36 | 180 | 13 | 36 | 51 | mA |
| $V_{DDI}$ | 2.62 | 134 | 141 | 161 | 187 | 93 | 272 | 388 | mA |
| Number of banks | | 7 | 8 | 8 | 10 | 10 | 9 | 19 | |

## 2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to $T_J$ = 85 °C, in worst-case $V_{DD}$ = 1.14 V.

***Table 16 •*** **Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays**

| Array Voltage $V_{DD}$ (V) | –40 °C | 0 °C | 25 °C | 70 °C | 85 °C | 100 °C |
|---|---|---|---|---|---|---|
| 1.14 | 0.83 | 0.89 | 0.92 | 0.98 | **1.00** | 1.02 |
| 1.2 | 0.75 | 0.80 | 0.83 | 0.89 | 0.91 | 0.93 |
| 1.26 | 0.69 | 0.73 | 0.76 | 0.81 | 0.83 | 0.85 |

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at $V_{OH}/V_{OL}$ Level.

***Table 26 •*** **I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**

| | R(WEAK PULL-UP) at $V_{OH}$ (Ω) | | R(WEAK PULL-DOWN) at $V_{OL}$ (Ω) | |
|---|---|---|---|---|
| **$V_{DDI}$ Domain** | **Min** | **Max** | **Min** | **Max** |
| 3.3 V | 9.9K | 17.1K | 9.98K | 17.5K |
| 2.5 V[1, 2] | 10K | 17.6K | 10.1K | 18.4K |
| 1.8 V[1, 2] | 10.4K | 19.1K | 10.4K | 20.4K |
| 1.5 V[1, 2] | 10.7K | 20.4K | 10.8K | 22.2K |
| 1.2 V[1, 2] | 11.3K | 23.2K | 11.5K | 26.7K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at $V_{OH}/V_{OL}$ Level.

***Table 27 •*** **I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank**

| | R(WEAK PULL-UP) at $V_{OH}$ (Ω) | | R(WEAK PULL-DOWN) at $V_{OL}$ (Ω) | |
|---|---|---|---|---|
| **$V_{DDI}$ Domain** | **Min** | **Max** | **Min** | **Max** |
| 2.5 V[1, 2] | 9.6K | 16.6K | 9.5K | 16.4K |
| 1.8 V[1, 2] | 9.7K | 17.3K | 9.7K | 17.1K |
| 1.5 V[1, 2] | 9.9K | 18K | 9.8K | 17.6K |
| 1.2 V[1, 2] | 10.3K | 19.6K | 10K | 19.1K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

***Table 28 •*** **Schmitt Trigger Input Hysteresis**

| Input Buffer Configuration | Hysteresis Value (Typical, unless otherwise noted) |
|---|---|
| 3.3 V LVTTL/LVCMOS/ PCI/PCI-X | 0.05 × $V_{DDI}$ (worst-case) |
| 2.5 V LVCMOS | 0.05 × $V_{DDI}$ (worst-case) |
| 1.8 V LVCMOS | 0.1 × $V_{DDI}$ (worst-case) |
| 1.5 V LVCMOS | 60 mV |
| 1.2 V LVCMOS | 20 mV |

***Table 62 •*** **LVCMOS 1.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | VOH | $V_{DDI}$ × 0.75 | | V |
| DC output logic low | VOL | | $V_{DDI}$ × 0.25 | V |

***Table 63 •*** **LVCMOS 1.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 235 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 220 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 64 •*** **LVCMOS 1.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 40 | Ω |

***Table 65 •*** **LVCMOS 1.5 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 66 •*** **LVCMOS 1.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 6 | 6 |
| 8 mA | | 8 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 8 | 8 |
| | | 10 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 10 | 10 |
| | | 12 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 12 | 12 |

**Note:** For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

***Table 70 •*** **LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers) *(continued)***

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 6 mA | Slow | 4.244 | 4.993 | 3.465 | 4.076 | 4.233 | 4.979 | 6.39 | 7.518 | 5.736 | 6.748 | ns |
| | Medium | 3.774 | 4.44 | 3.05 | 3.587 | 3.762 | 4.426 | 6.114 | 7.193 | 5.397 | 6.35 | ns |
| | Medium fast | 3.544 | 4.17 | 2.839 | 3.339 | 3.529 | 4.152 | 5.978 | 7.033 | 5.27 | 6.2 | ns |
| | Fast | 3.519 | 4.14 | 2.82 | 3.317 | 3.504 | 4.122 | 5.965 | 7.017 | 5.259 | 6.187 | ns |
| 8 mA | Slow | 4.099 | 4.823 | 3.311 | 3.894 | 4.087 | 4.807 | 6.584 | 7.746 | 5.854 | 6.888 | ns |
| | Medium | 3.656 | 4.301 | 2.927 | 3.443 | 3.642 | 4.284 | 6.311 | 7.425 | 5.553 | 6.533 | ns |
| | Medium fast | 3.437 | 4.044 | 2.731 | 3.213 | 3.42 | 4.023 | 6.182 | 7.273 | 5.435 | 6.394 | ns |
| | Fast | 3.41 | 4.012 | 2.715 | 3.193 | 3.393 | 3.991 | 6.178 | 7.269 | 5.425 | 6.383 | ns |
| 10 mA | Slow | 4.029 | 4.74 | 3.238 | 3.809 | 4.015 | 4.723 | 6.732 | 7.921 | 5.965 | 7.018 | ns |
| | Medium | 3.601 | 4.237 | 2.867 | 3.372 | 3.586 | 4.218 | 6.473 | 7.615 | 5.669 | 6.669 | ns |
| | Medium fast | 3.384 | 3.981 | 2.672 | 3.143 | 3.365 | 3.958 | 6.351 | 7.471 | 5.55 | 6.529 | ns |
| | Fast | 3.357 | 3.949 | 2.655 | 3.123 | 3.338 | 3.927 | 6.345 | 7.464 | 5.54 | 6.518 | ns |
| 12 mA | Slow | 3.974 | 4.675 | 3.196 | 3.759 | 3.958 | 4.656 | 6.842 | 8.049 | 6.068 | 7.139 | ns |
| | Medium | 3.55 | 4.176 | 2.827 | 3.326 | 3.534 | 4.157 | 6.584 | 7.746 | 5.751 | 6.766 | ns |
| | Medium fast | 3.345 | 3.935 | 2.638 | 3.103 | 3.325 | 3.911 | 6.488 | 7.633 | 5.641 | 6.637 | ns |
| | Fast | 3.316 | 3.902 | 2.621 | 3.083 | 3.297 | 3.878 | 6.486 | 7.63 | 5.626 | 6.619 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 71 •*** **LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 4.423 | 5.203 | 5.397 | 6.35 | 5.686 | 6.69 | 5.609 | 6.599 | 5.561 | 6.542 | ns |
| 4 mA | Slow | 4.05 | 4.765 | 4.503 | 5.298 | 4.92 | 5.788 | 7.358 | 8.657 | 6.525 | 7.677 | ns |
| 6 mA | Slow | 4.081 | 4.801 | 4.259 | 5.012 | 4.699 | 5.528 | 7.659 | 9.011 | 6.709 | 7.893 | ns |
| 8 mA | Slow | 4.234 | 4.98 | 4.068 | 4.786 | 4.521 | 5.319 | 8.218 | 9.668 | 7.05 | 8.294 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 95 •*** **HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| | **HSTL Class I** | | | |
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |
| Output minimum source DC current (MSIO and DDRIO I/O banks) | $I_{OH}$ at $V_{OH}$ | –8.0 | | mA |
| Output minimum sink current (MSIO and DDRIO I/O banks) | $I_{OL}$ at $V_{OL}$ | 8.0 | | mA |
| | **HSTL Class II** | | | |
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | –16.0 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | 16.0 | | mA |

***Table 96 •*** **HSTL DC Differential Voltage Specification**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.2 | V |

***Table 97 •*** **HSTL AC Differential Voltage Specifications**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ | 0.4 | | V |
| AC differential cross point voltage | $V_x$ | 0.68 | 0.9 | V |

***Table 98 •*** **HSTL Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

***Table 99 •*** **HSTL Impedance Specification**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | $R_{REF}$ | 25.5, 47.8 | Ω | Reference resistance = 191 Ω |
| Effective impedance value (ODT for DDRIO I/O bank only) | $R_{TT}$ | 47.8 | Ω | Reference resistance = 191 Ω |

***Table 128 •*** **DDR2/SSTL18 Transmitter Characteristics (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **SSTL18 Class I (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.413 | 2.84 | 2.797 | 3.29 | 2.797 | 3.29 | 2.282 | 2.685 | 2.282 | 2.685 | ns |
| **SSTL18 Class II (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.315 | 2.724 | 2.698 | 3.173 | 2.698 | 3.173 | 2.242 | 2.639 | 2.242 | 2.639 | ns |

### *2.3.6.5 Stub-Series Terminated Logic 1.5 V (SSTL15)*

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

The following table lists the SSTL15 DC voltage specifications for DDRIO bank.

***Table 129 •*** **SSTL15 DC Recommended DC Operating Conditions (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

***Table 130 •*** **SSTL15 DC Input Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}(DC)$ | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}(DC)$ | –0.3 | $V_{REF}$ – 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 136 •*** **SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL15 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL15 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.425 V

***Table 137 •*** **DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 20 | 1.616 | 1.901 | ns |
| | 30 | 1.613 | 1.897 | ns |
| | 40 | 1.611 | 1.895 | ns |
| | 60 | 1.609 | 1.893 | ns |
| | 120 | 1.607 | 1.89 | ns |
| True differential | None | 1.623 | 1.91 | ns |
| | 20 | 1.637 | 1.926 | ns |
| | 30 | 1.63 | 1.918 | ns |
| | 40 | 1.626 | 1.914 | ns |
| | 60 | 1.622 | 1.91 | ns |
| | 120 | 1.619 | 1.905 | ns |

***Table 138 •*** **DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.533 | 2.98 | 2.522 | 2.967 | 2.523 | 2.968 | 2.427 | 2.855 | 2.428 | 2.856 | ns |
| Differential | 2.555 | 3.005 | 3.073 | 3.615 | 3.073 | 3.615 | 2.416 | 2.843 | 2.416 | 2.843 | ns |
| **DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)** | | | | | | | | | | | |
| Single-ended | 2.53 | 2.977 | 2.514 | 2.958 | 2.516 | 2.96 | 2.422 | 2.849 | 2.425 | 2.852 | ns |
| Differential | 2.552 | 3.002 | 2.591 | 3.048 | 2.59 | 3.047 | 2.882 | 3.391 | 2.881 | 3.39 | ns |

The following table lists the input data register propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

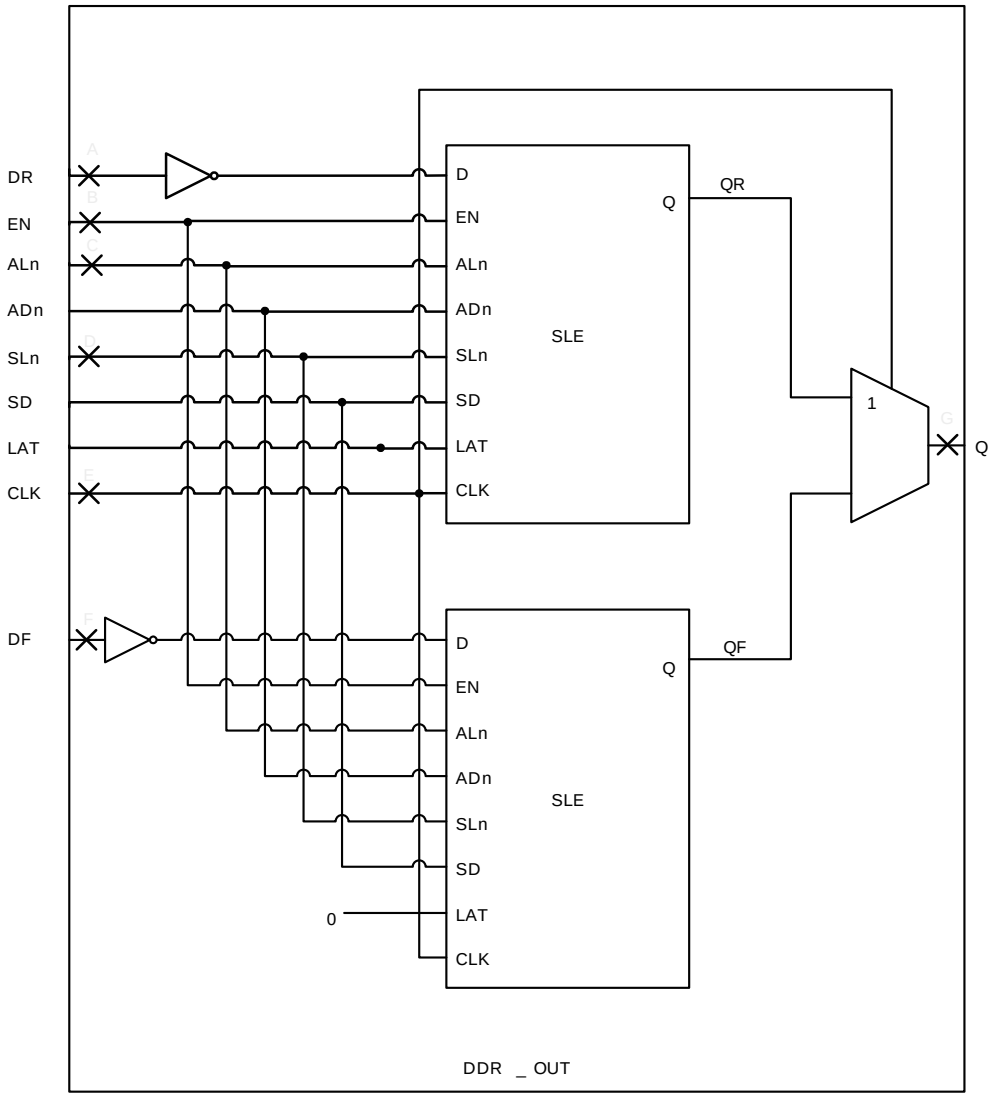
***Table 219 •*** **Input Data Register Propagation Delays**

| Parameter | Symbol | Measuring Nodes (from, to)[1] | –1 | –Std | Unit |
|---|---|---|---|---|---|
| Bypass delay of the input register | $T_{IBYP}$ | F, G | 0.353 | 0.415 | ns |
| Clock-to-Q of the input register | $T_{ICLKQ}$ | E, G | 0.16 | 0.188 | ns |
| Data setup time for the input register | $T_{ISUD}$ | A, E | 0.357 | 0.421 | ns |
| Data hold time for the input register | $T_{IHD}$ | A, E | 0 | 0 | ns |
| Enable setup time for the input register | $T_{ISUE}$ | B, E | 0.46 | 0.542 | ns |
| Enable hold time for the input register | $T_{IHE}$ | B, E | 0 | 0 | ns |
| Synchronous load setup time for the input register | $T_{ISUSL}$ | D, E | 0.46 | 0.542 | ns |
| Synchronous load hold time for the input register | $T_{IHSL}$ | D, E | 0 | 0 | ns |
| Asynchronous clear-to-Q of the input register (ADn=1) | $T_{IALN2Q}$ | C, G | 0.625 | 0.735 | ns |
| Asynchronous preset-to-Q of the input register (ADn=0) | | C, G | 0.587 | 0.69 | ns |
| Asynchronous load removal time for the input register | $T_{IREMALN}$ | C, E | 0 | 0 | ns |
| Asynchronous load recovery time for the input register | $T_{IRECALN}$ | C, E | 0.074 | 0.087 | ns |
| Asynchronous load minimum pulse width for the input register | $T_{IWALN}$ | C, C | 0.304 | 0.357 | ns |
| Clock minimum pulse width high for the input register | $T_{ICKMPWH}$ | E, E | 0.075 | 0.088 | ns |
| Clock minimum pulse width low for the input register | $T_{ICKMPWL}$ | E, E | 0.159 | 0.187 | ns |

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

### 2.3.9.4 Output DDR Module

**Figure 12 • Output DDR Module**



The following table lists the RAM1K18 – dual-port mode for depth × width configuration 8K × 2 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 234 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.32 | | 0.377 | ns |
| Read access time without pipeline register | | | 2.272 | | 2.673 | ns |
| Access time with feed-through write timing | | | 1.511 | | 1.778 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.612 | | 0.72 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.33 | | 0.388 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.511 | | 1.778 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.529 | | 0.622 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.528 | | 1.797 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.488 | | 0.574 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

***Table 241 •*** **µSRAM (RAM256x4) in 256 × 4 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Write address hold time | $T_{ADDRCHD}$ | 0.245 | | 0.288 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 512 × 2 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 242 •*** **µSRAM (RAM512x2) in 512 × 2 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.76 | | 2.08 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.96 | | 2.306 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.137 | | 0.161 | | ns |
| Read address hold time in asynchronous mode | | –0.58 | | –0.68 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.14 | | 2.52 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |

***Table 251 •*** **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only) *(continued)***

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 150 | 544496 | 10 | 158 | 15 | Sec |

***Table 252 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 9 | 61 | 11 | Sec |
| 010 | 842688 | 15 | 107 | 21 | Sec |
| 025 | 1497408 | 26 | 121 | 35 | Sec |
| 050 | 2695168 | 43 | 141 | 55 | Sec |
| 060 | 2686464 | 48 | 143 | 60 | Sec |
| 090 | 4190208 | 75 | 244 | 91 | Sec |
| 150 | 6682768 | 117 | 296 | 141 | Sec |

***Table 253 •*** **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric Only)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 47 | 27 | 28 | Sec |
| 010 | 77 | 35 | 35 | Sec |
| 025 | 150 | 42 | 41 | Sec |
| 050 | 33[1] | Not Supported | Not Supported | Sec |
| 060 | 291 | 83 | 82 | Sec |
| 090 | 427 | 109 | 108 | Sec |
| 150 | 708 | 157 | 160 | Sec |

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

***Table 254 •*** **Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 41 | 48 | 49 | Sec |
| 010 | 86 | 87 | 87 | Sec |
| 025 | 87 | 85 | 86 | Sec |
| 050 | 85 | Not Supported | Not Supported | Sec |
| 060 | 78 | 86 | 86 | Sec |
| 090 | 154 | 162 | 162 | Sec |

**Table 254 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (eNVM Only) *(continued)***

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 150 | 161 | 161 | 161 | Sec |

**Table 255 • Programming Times with 100 kHz, 25 MHz, and 12.5 MHz SPI Clock Rates (Fabric and eNVM)**

| M2S/M2GL Device | Auto Programming 100 kHz | Auto Update 25 MHz | Programming Recovery 12.5 MHz | Unit |
|---|---|---|---|---|
| 005 | 47 | 27 | 28 | Sec |
| 010 | 77 | 35 | 35 | Sec |
| 025 | 150 | 42 | 41 | Sec |
| 050 | 33[1] | Not Supported | Not Supported | Sec |
| 060 | 291 | 83 | 82 | Sec |
| 090 | 427 | 109 | 108 | Sec |
| 150 | 708 | 157 | 160 | Sec |
| 005 | 41 | 48 | 49 | Sec |
| 010 | 86 | 87 | 87 | Sec |
| 025 | 87 | 85 | 86 | Sec |
| 050 | 85 | Not Supported | Not Supported | Sec |
| 060 | 78 | 86 | 86 | Sec |
| 090 | 154 | 162 | 162 | Sec |
| 150 | 161 | 161 | 161 | Sec |
| 005 | 87 | 67 | 66 | Sec |
| 010 | 161 | 113 | 113 | Sec |
| 025 | 229 | 120 | 121 | Sec |
| 050 | 112 | Not Supported | Not Supported | Sec |
| 060 | 368 | 161 | 158 | Sec |
| 090 | 582 | 261 | 260 | Sec |
| 150 | 867 | 309 | 310 | Sec |

1. Auto Programming in 050 device is done through SC_SPI, and SPI CLK is set to 6.25 MHz.

***Table 262 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 6 | 41 | 8 | Sec |
| 010 | 568784 | 10 | 48 | 14 | Sec |
| 025 | 1223504 | 21 | 61 | 29 | Sec |
| 050 | 2424832 | 39 | 82 | 50 | Sec |
| 060 | 2418896 | 44 | 87 | 54 | Sec |
| 090 | 3645968 | 66 | 112 | 79 | Sec |
| 150 | 6139184 | 108 | 162 | 128 | Sec |

***Table 263 •*** **SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 3 | 64 | 4 | Sec |
| 010 | 274816 | 4 | 104 | 7 | Sec |
| 025 | 274816 | 4 | 104 | 8 | Sec |
| 050 | 2,78,528 | 4 | 102 | 8 | Sec |
| 060 | 268480 | 6 | 102 | 8 | Sec |
| 090 | 544496 | 10 | 179 | 15 | Sec |
| 150 | 544496 | 10 | 180 | 15 | Sec |

***Table 264 •*** **SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 9 | 83 | 11 | Sec |
| 010 | 842688 | 15 | 129 | 21 | Sec |
| 025 | 1497408 | 26 | 143 | 35 | Sec |
| 050 | 2695168 | 43 | 163 | 55 | Sec |
| 060 | 2686464 | 48 | 165 | 60 | Sec |
| 090 | 4190208 | 75 | 266 | 91 | Sec |
| 150 | 6682768 | 117 | 318 | 141 | Sec |

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)** ***(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 0.8 | ms | 005, 010, 025, and 050 devices |
| | | | | 1.0 | ms | 090 and 150 devices |

***Table 278 •*** **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 2 | | MHz | |
| Accuracy | ACCXTAL | | | 0.00105 | % | 050 devices |
| | | | | 0.003 | % | 005, 010, 025, 090, and 150 devices |
| | | | | 0.004 | % | 060 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 1 | 5 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 1 | 5 | ns | |
| Operating current | IDYNXTAL | | 0.3 | | mA | |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 4.5 | ms | 010 and 050 devices |
| | | | | 5 | ms | 005 and 025 devices |
| | | | | 7 | ms | 090 and 150 devices |

***Table 279 •*** **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

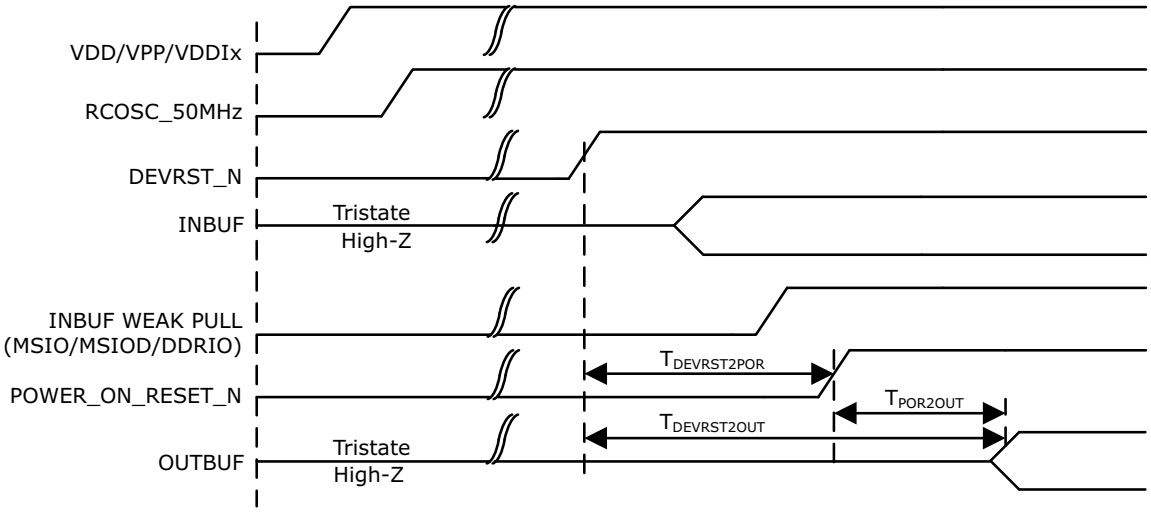
| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 32 | | kHz | |
| Accuracy | ACCXTAL | | | 0.004 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.005 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 150 | 300 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 150 | 300 | ns | |
| Operating current | IDYNXTAL | | 0.044 | | mA | 010 and 050 devices |
| | | | 0.060 | | mA | 005, 025, 060, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 115 | ms | 005, 025, 050, 090, and 150 devices |
| | | | | 126 | ms | 010 devices |

The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 292 •*** **DEVRST_N to Functional Times for IGLOO2**

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 116 | 113 | 113 | 115 | 115 | 114 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 314 | 353 | 314 | 307 | 343 | 341 | 341 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 200 | 238 | 201 | 195 | 230 | 229 | 227 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

***Figure 20 •*** **DEVRST_N to Functional Timing Diagram for IGLOO2**




## 2.3.27 Flash*Freeze Timing Characteristics

The following table lists the Flash*Freeze entry and exit times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 293 •*** **Flash*Freeze Entry and Exit Times**

| | | Entry/Exit Timing FCLK = 100MHz | | Entry/Exit Timing FCLK = 3 MHz | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **005, 010, 025, 060, 090, and 150** | **050** | **All Devices** | **Unit** | **Conditions** |
| Entry time | TFF_ENTRY | 160 | 150 | 320 | µs | eNVM and MSS/HPMS PLL = ON |
| | | 215 | 200 | 430 | µs | eNVM and MSS/HPMS PLL= OFF |
| Exit time with respect to the MSS PLL Lock | TFF_EXIT | 100 | 100 | 140 | µs | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 136 | 120 | 190 | µs | eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit |
| | | 200 | 200 | 285 | µs | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |
| | | 200 | 200 | 285 | µs | eNVM = OFF and MSS/HPMS PLL = ON during F*F and eNVM turned back on at exit |

***Table 305 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%–90%)[1] | | 2.906 | | ns | IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C |
| SPI master configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 8.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 2.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 12 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |
| SPI slave configuration (applicable for 005, 010, 025, and 050 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 17.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) + 3.0 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 2 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 7 | | | ns | |
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.