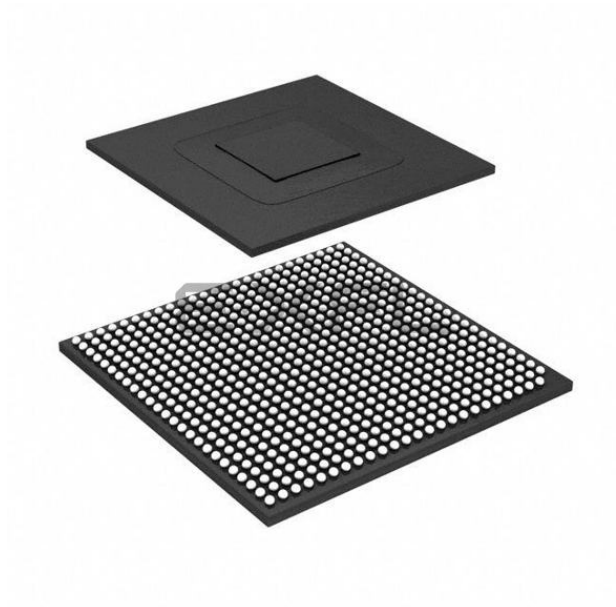

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s5dvm10ac

- Snoop Control Unit (SCU)
- 512 KB unified I/D L2 cache:
  - Used by one core in i.MX 6Solo
  - Shared by two cores in i.MX 6DualLite
- Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache), as per Table 9, "Operating Ranges," on page 24.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (512 KB)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces: The i.MX 6Solo/6DualLite processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
  - 16/32-bit LP-DDR2-800, 16/32-bit DDR3-800 and LV-DDR3-800 in i.MX 6Solo; 16/32/64-bit LP-DDR2-800, 16/32/64-bit DDR3-800 and LV-DDR3-800, supporting DDR interleaving mode for 2x32 LPDDR2-800 in i.MX 6DualLite
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Solo/6DualLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to two interfaces may be active in parallel (excluding EPDC).
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
  - HDMI 1.4 port

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Solo/6DualLite processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 1 Gbps speed per data lane.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Solo/6DualLite platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Solo/6DualLite processor has two such modules.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
eCSPI1-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-3 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6Solo/6DualLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

Table 10. On-Chip LDOs[1] and their On-Chip Loads (continued)

Voltage Source	Load	Comment
VDDSOC_CAP	HDMI_VP	Board-level connection to VDDSOC_CAP[2] [3]
	PCIE_VP	
	PCIE_VPTX	

1 On-chip LDOs are designed to supply i.MX6 loads and must not be used to supply external loads.

2 VDDARM_CAP should not exceed VDDSOC_CAP by more than 50 mV.

3 There is no requirement for VDDSOC_CAP to track within 50 mV as long as it is greater than VDDARM_CAP.

4.1.4 External Clock Sources

Each i.MX 6Solo/6DualLite processor has two external input system clocks: a low frequency (CKIL) and a high frequency (XTAL).

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the CKIL, in case accuracy is not important.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

Table 11. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
CKIL Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTAL Oscillator[2,4]	f_{xtal}		24		MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

3 Recommended nominal frequency 32.768 kHz.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors in typical condition. Table 14 shows the USB interface current consumption in power down mode..

Table 14. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 PCIe 2.0 Power Consumption

Table 15 provides PCIe PHY currents under certain Tx operating modes.

Table 15. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
PO: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
POs: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Reocvery Time Latency, Lower Power State		PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down		PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

Table 25. DDR3/DDR3L I/O DC Electrical Characteristics (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
240 Ω unit calibration resolution	Rres			10	Ω
Keeper Circuit Resistance	Rkeep		105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

2 Vref – DDR3/DDR3L external reference voltage

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

Table 26 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 26. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS		1.125	1.2	1.375	V

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

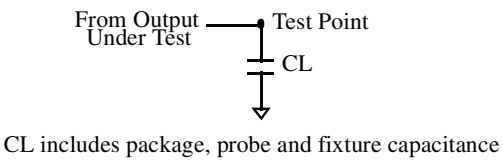

Figure 4. Load Circuit for Output

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 22 shows the basic timing parameters. The timing parameters for this diagram appear in Table 41.

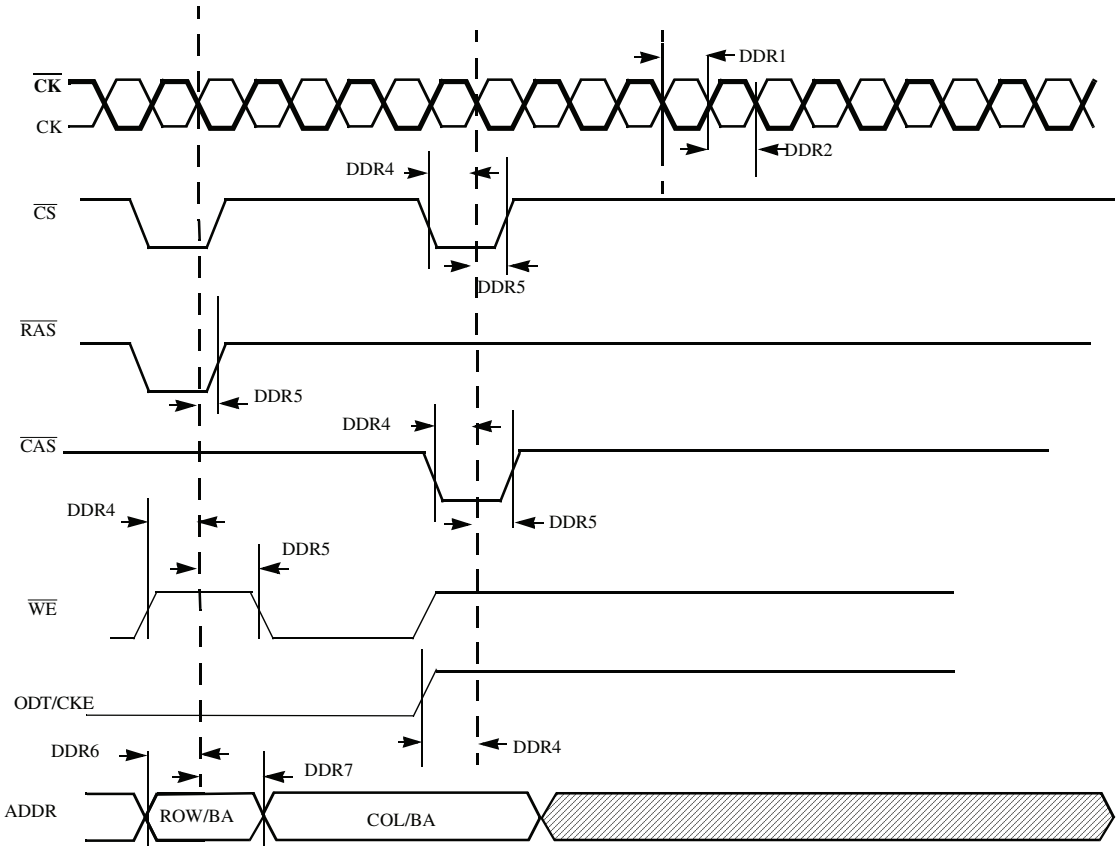

Figure 22. DDR3 Command and Address Timing Parameters

Table 41. DDR3/DDR3L Timing Parameter Table

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	t_{CH}	0.47	0.53	t_{CK}
DDR2	CK clock low-level width	t_{CL}	0.47	0.53	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	800	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	580	—	ps
DDR6	Address output setup time	t_{IS}	800	—	ps
DDR7	Address output hold time	t_{IH}	580	—	ps

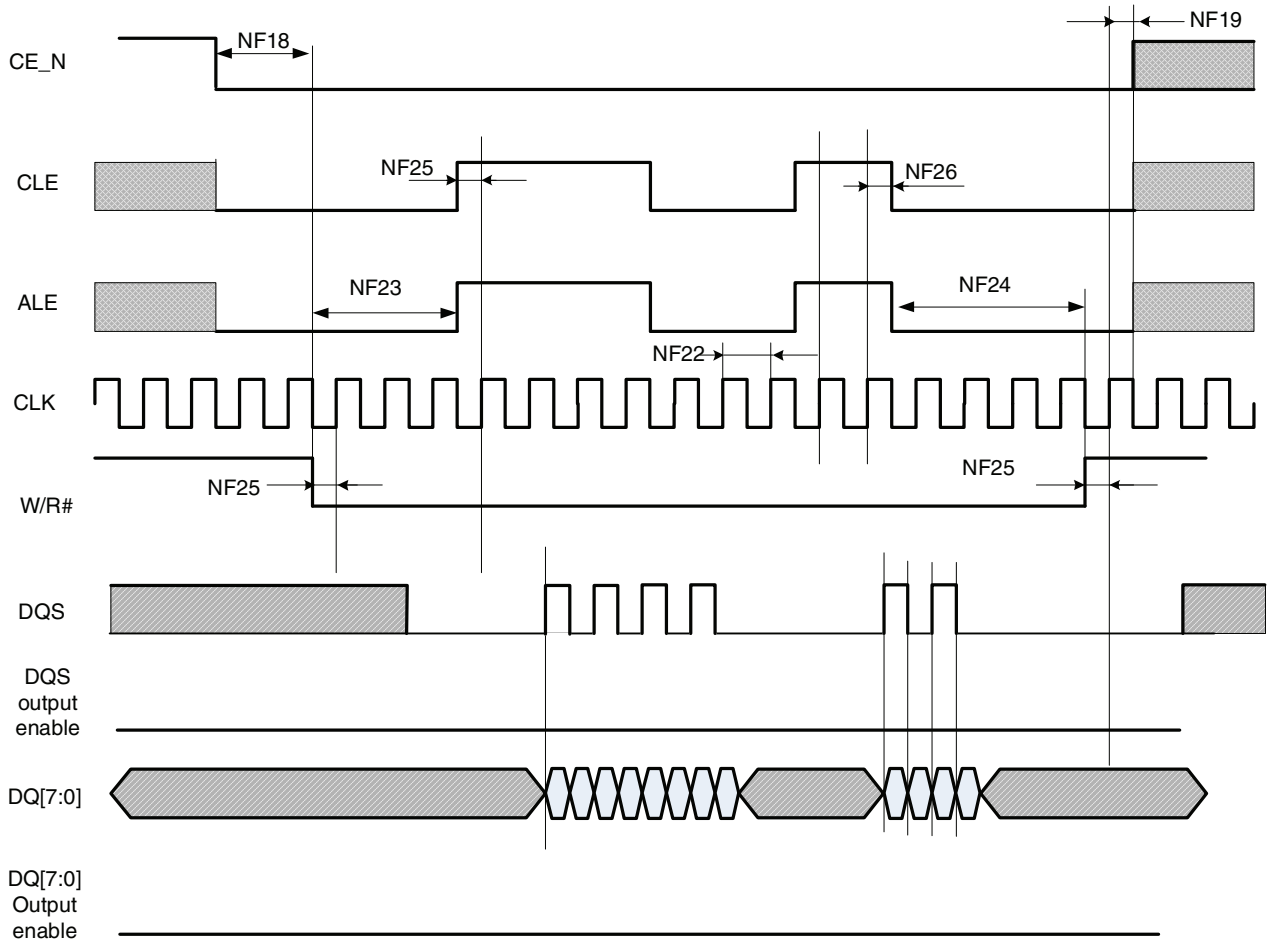

Figure 34. Source Synchronous Mode Data Read Timing Diagram

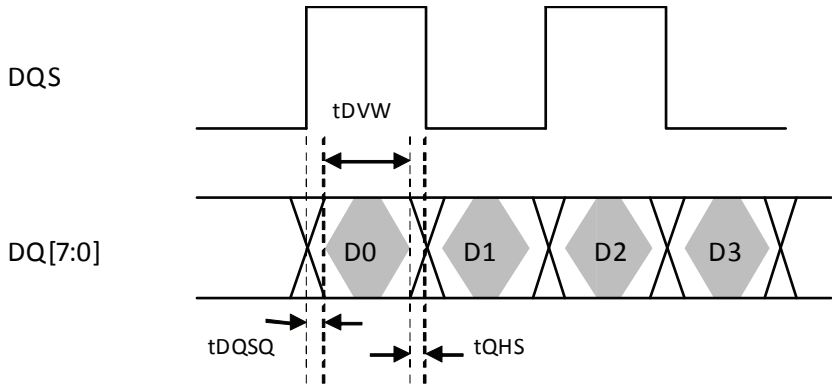

Figure 35. DQS/DQ Read Valid Window

4.10.3.2 Read and Write Timing

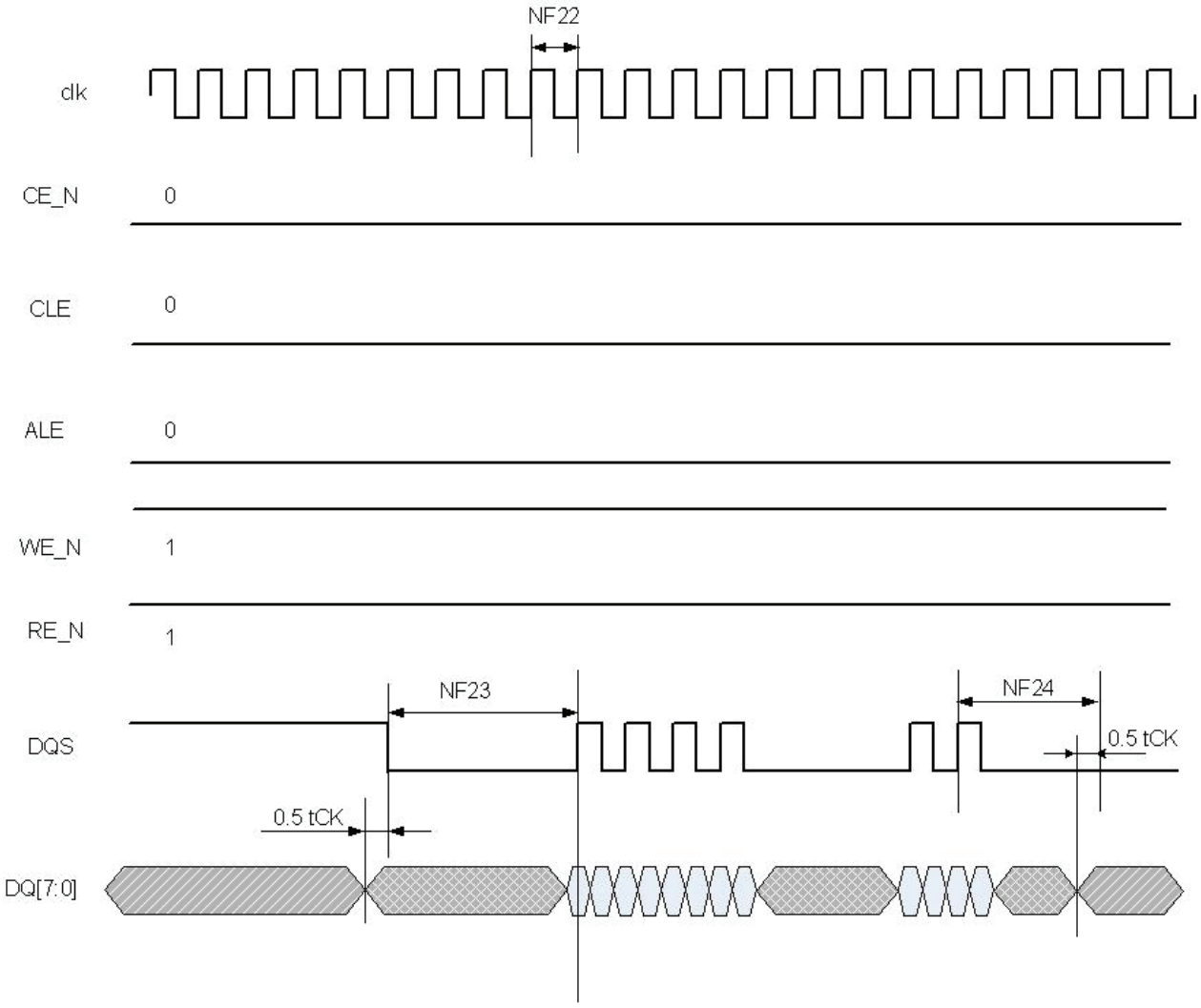

Figure 36. Samsung Toggle Mode Data Write Timing

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

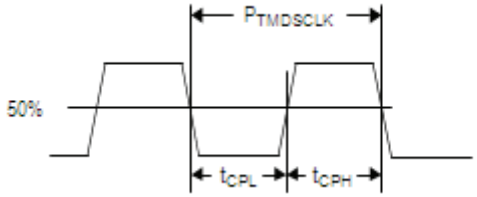

Figure 56. TMDS Clock Signal Definitions

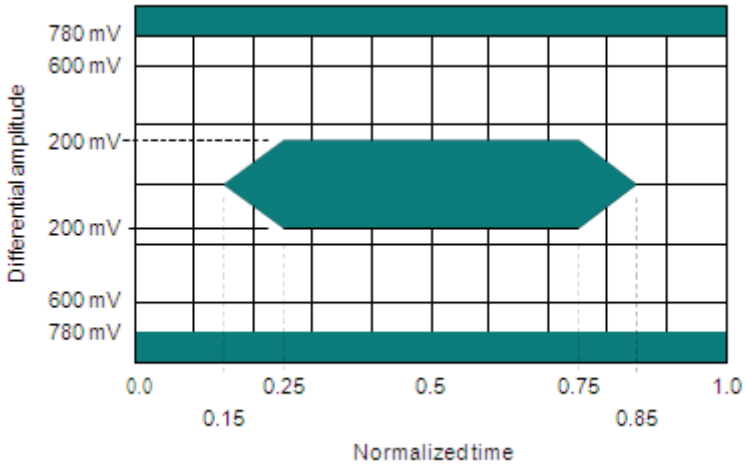

Figure 57. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

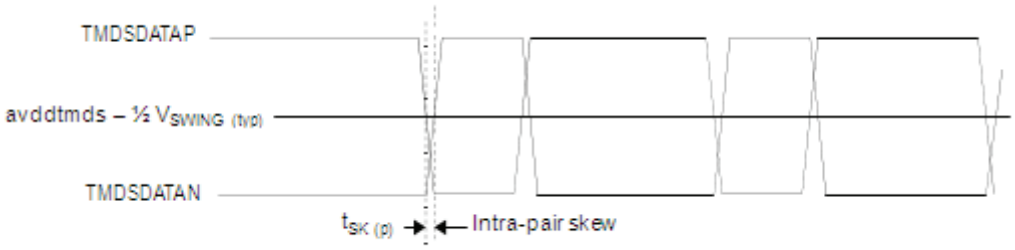

Figure 58. Intra-Pair Skew Definition

4.11.10.3 Electrical Characteristics

Figure 64 depicts the sensor interface timing. SENSB_MCLK signal described here is not generated by the IPU. Table 66 lists the sensor interface timing characteristics.

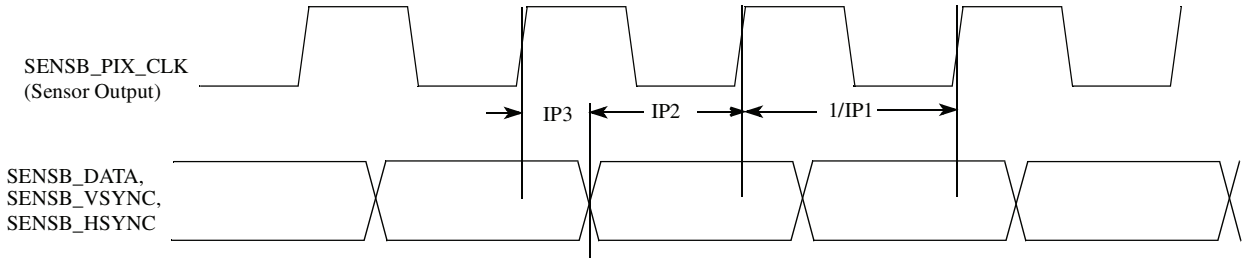

Figure 64. Sensor Interface Timing Diagram

Table 66. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 67 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 72. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω			25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF			25	ns
t_{reo}		30% to 85%, C_L<70 pF			35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	Vps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

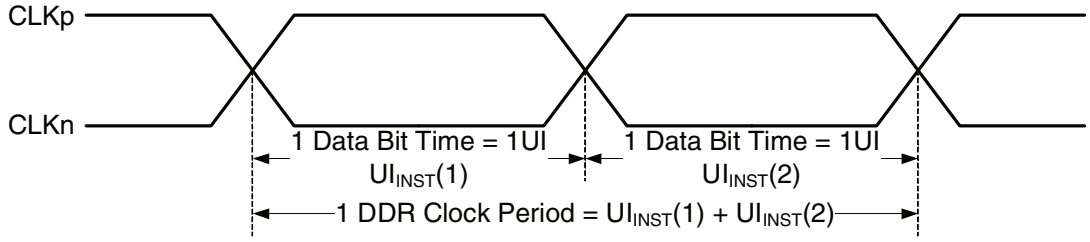

Figure 72. DDR Clock Definition

4.11.13.4 Synchronized Data Flow Transmission with Wake

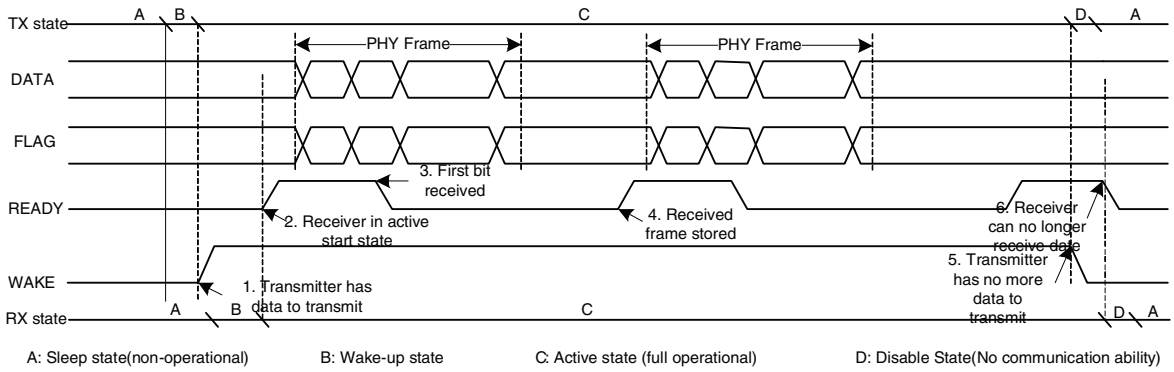

Figure 79. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

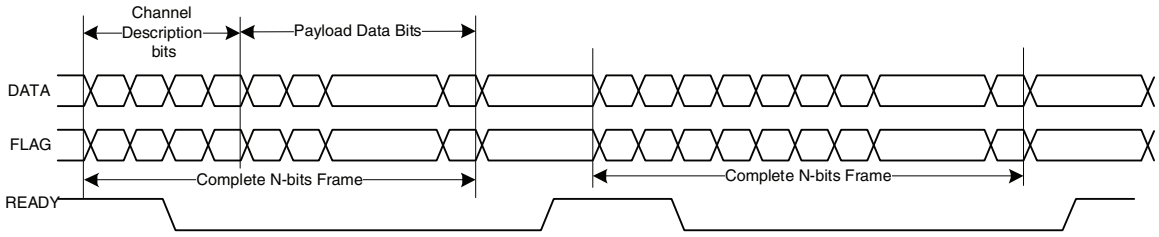

Figure 80. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

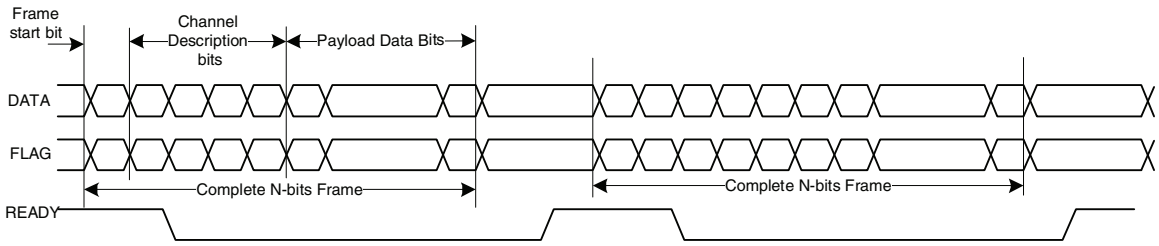

Figure 81. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

Table 78. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.20.2 Receive Timing

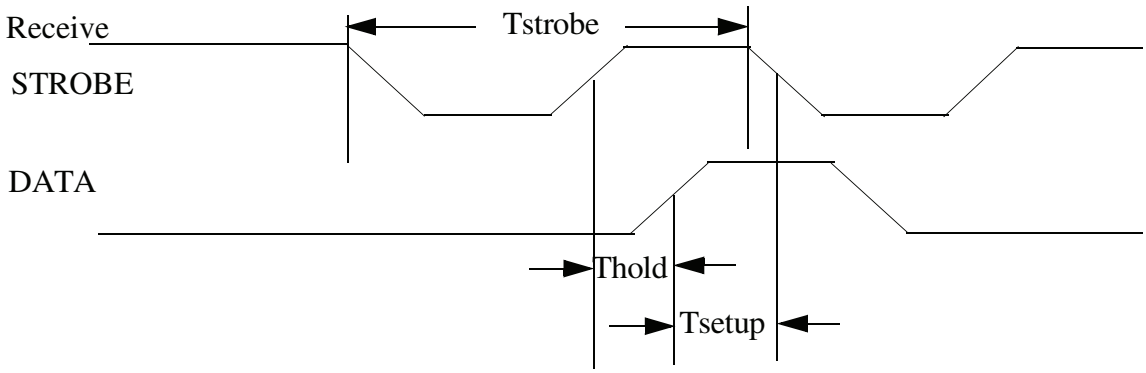

Figure 100. USB HSIC Receive Waveform

Table 88. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.11.21 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

Table 89. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
EIM_DA0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_DA1	Input	BOOT_CFG1[1]	
EIM_DA2	Input	BOOT_CFG1[2]	
EIM_DA3	Input	BOOT_CFG1[3]	
EIM_DA4	Input	BOOT_CFG1[4]	
EIM_DA5	Input	BOOT_CFG1[5]	
EIM_DA6	Input	BOOT_CFG1[6]	
EIM_DA7	Input	BOOT_CFG1[7]	
EIM_DA8	Input	BOOT_CFG2[0]	
EIM_DA9	Input	BOOT_CFG2[1]	
EIM_DA10	Input	BOOT_CFG2[2]	
EIM_DA11	Input	BOOT_CFG2[3]	
EIM_DA12	Input	BOOT_CFG2[4]	
EIM_DA13	Input	BOOT_CFG2[5]	
EIM_DA14	Input	BOOT_CFG2[6]	
EIM_DA15	Input	BOOT_CFG2[7]	
EIM_A16	Input	BOOT_CFG3[0]	
EIM_A17	Input	BOOT_CFG3[1]	
EIM_A18	Input	BOOT_CFG3[2]	
EIM_A19	Input	BOOT_CFG3[3]	
EIM_A20	Input	BOOT_CFG3[4]	
EIM_A21	Input	BOOT_CFG3[5]	
EIM_A22	Input	BOOT_CFG3[6]	
EIM_A23	Input	BOOT_CFG3[7]	
EIM_A24	Input	BOOT_CFG4[0]	
EIM_WAIT	Input	BOOT_CFG4[1]	
EIM_LBA	Input	BOOT_CFG4[2]	
EIM_EB0	Input	BOOT_CFG4[3]	
EIM_EB1	Input	BOOT_CFG4[4]	
EIM_RW	Input	BOOT_CFG4[5]	
EIM_EB2	Input	BOOT_CFG4[6]	
EIM_EB3	Input	BOOT_CFG4[7]	

Table 91. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NC	G13	
NC	N12	

Table 92 shows an alpha-sorted list of functional contact assignments for the 21 x 21 mm package.

Table 92. 21 x 21 mm Functional Contact Assignments[1]

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[0]	Input	100 kΩ pull-down
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[1]	Input	100 kΩ pull-down
CLK1_N	C7	VDDHIGH_CAP					
CLK1_P	D7	VDDHIGH_CAP					
CLK2_N	C5	VDDHIGH_CAP					
CLK2_P	D5	VDDHIGH_CAP					
CSI_CLK0M	F4	NVCC_MIPI	ANALOG				
CSI_CLK0P	F3	NVCC_MIPI	ANALOG				
CSI_D0M	E4	NVCC_MIPI	ANALOG				
CSI_D0P	E3	NVCC_MIPI	ANALOG				
CSI_D1M	D1	NVCC_MIPI	ANALOG				
CSI_D1P	D2	NVCC_MIPI	ANALOG				
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[28]	Input	100 kΩ pull-up
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[29]	Input	100 kΩ pull-up
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[30]	Input	100 kΩ pull-up
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[31]	Input	100 kΩ pull-up
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[0]	Input	100 kΩ pull-up
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[1]	Input	100 kΩ pull-up
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[2]	Input	100 kΩ pull-up
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[3]	Input	100 kΩ pull-up
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[4]	Input	100 kΩ pull-up
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[5]	Input	100 kΩ pull-up
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[22]	Input	100 kΩ pull-up
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[23]	Input	100 kΩ pull-up

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[0]	Output	Low
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[1]	Output	Low
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[2]	Output	Low
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[3]	Output	Low
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[4]	Output	Low
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[5]	Output	Low
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[6]	Output	Low
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[7]	Output	Low
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_RAS	Output	Low
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_RESET	Output	Low
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[0]	Output	Low
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[1]	Output	Low
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[2]	Output	Low
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDCKE[0]	Output	Low
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDCKE[1]	Output	Low
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDCLK0	Output	Low
DRAM_SDCLK_0_B	AE15	NVCC_DRAM			DRAM_SDCLK_0_B	-	-
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDCLK1	Output	Low
DRAM_SDCLK_1_B	AE14	NVCC_DRAM			DRAM_SDCLK_1_B	-	-
DRAM_SDODT0	AC16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_ODT[0]	Output	Low
DRAM_SDODT1	AB17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_ODT[1]	Output	Low
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM			DRAM_SDQS0_B	-	-
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM			DRAM_SDQS1_B	-	-
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM			DRAM_SDQS2_B	-	-
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM			DRAM_SDQS3_B	-	-
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[4]	Input	Hi-Z

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[2]	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[3]	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[4]	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[5]	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[6]	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[7]	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[10]	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[9]	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	src.RESET_B	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH					
PCIE_RXP	B2	PCIE_VPH					
PCIE_TXM	A3	PCIE_VPH					
PCIE_TXP	B3	PCIE_VPH					
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	Output	Low
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm.PMIC_VSTBY_REQ	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src.POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[25]	Input	100 kΩ pull-up
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[27]	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[28]	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[29]	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[24]	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[30]	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[20]	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[21]	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[22]	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[23]	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[26]	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[19]	Input	100 kΩ pull-down