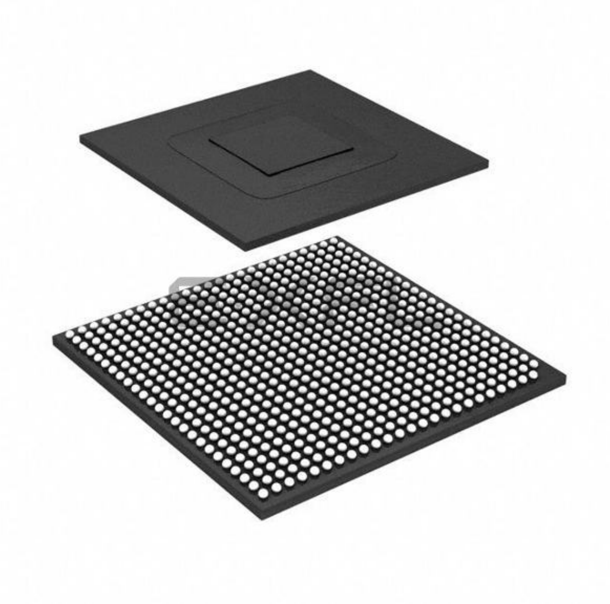

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s5evm10ab

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details. **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes. It is available in both i.MX 6DualLite and i.MX 6Solo.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit "set and forget" timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse fox accessible through OCOTP_CTRL interface.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3Dv5	Graphics Processing Unit, ver.5	Multimedia Peripherals	The GPU3Dv5 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
HDMI Tx	HDMI Tx i/f	Multimedia Peripherals	The HDMI module provides HDMI standard i/f port to an HDMI 1.4 compliant display.
HSI	MIPI HSI i/f	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3 I^2C-4	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Solo/6DualLite processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Solo/6DualLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 11 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 12. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN	996 MHz ARM clock based on Power Virus operation	2200	mA
VDDSOC_IN	996 MHz ARM clock	1260	mA
VDDHIGH_IN		125[1]	mA
VDD_SNVS_IN		275[2]	µA
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)		25[3]	mA
Primary Interface (IO) Supplies			

enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value for component selection), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.4 PLL’s Electrical Characteristics

4.4.1 Audio/Video PLL’s Electrical Parameters

Table 17. Audio/Video PLL’s Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 18. 528 MHz PLL’s Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

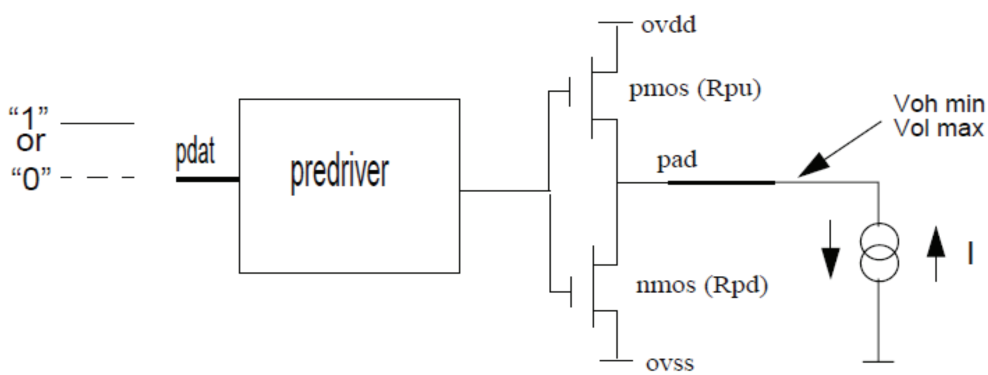


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 General Purpose I/O (GPIO) DC Parameters

Table 23 shows DC parameters for GPIO pads. The parameters in Table 23 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 23. GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
GPIO DC Electrical Characteristics					
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (ipp_dse=001,010) Ioh= -1mA (ipp_dse=011,100,101,110,111)	OVDD-0.15		V
Low-level output voltage[1]	VOL	Iol= 0.1mA (ipp_dse=001,010) Iol= 1mA (ipp_dse=011,100,101,110,111)	0.15	V	
High-Level input voltagev[1,2]	VIH		0.7*OVDD	OVDD	V

[1] t_{SKD} = | t_{PHLD} - t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

[2] Measurement levels are 20-80% from output voltage.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Solo/6DualLite processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

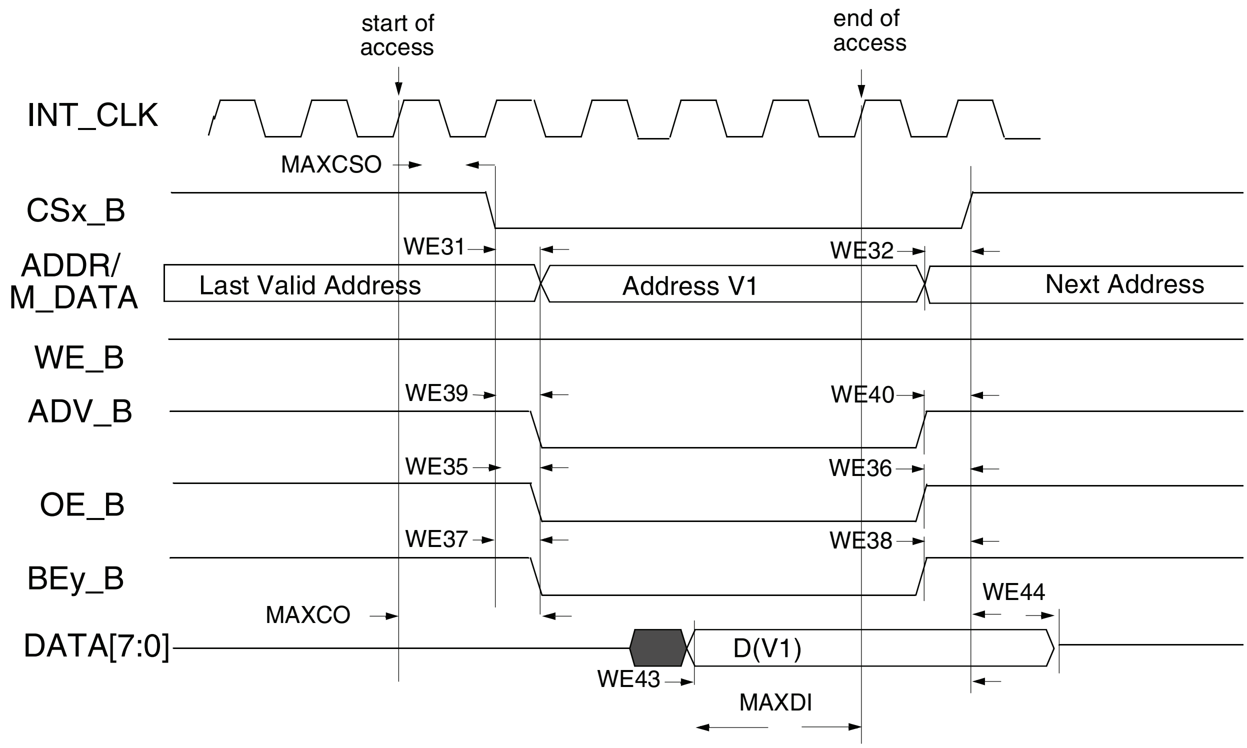


Figure 16. Asynchronous Memory Read Access (RWSC = 5)

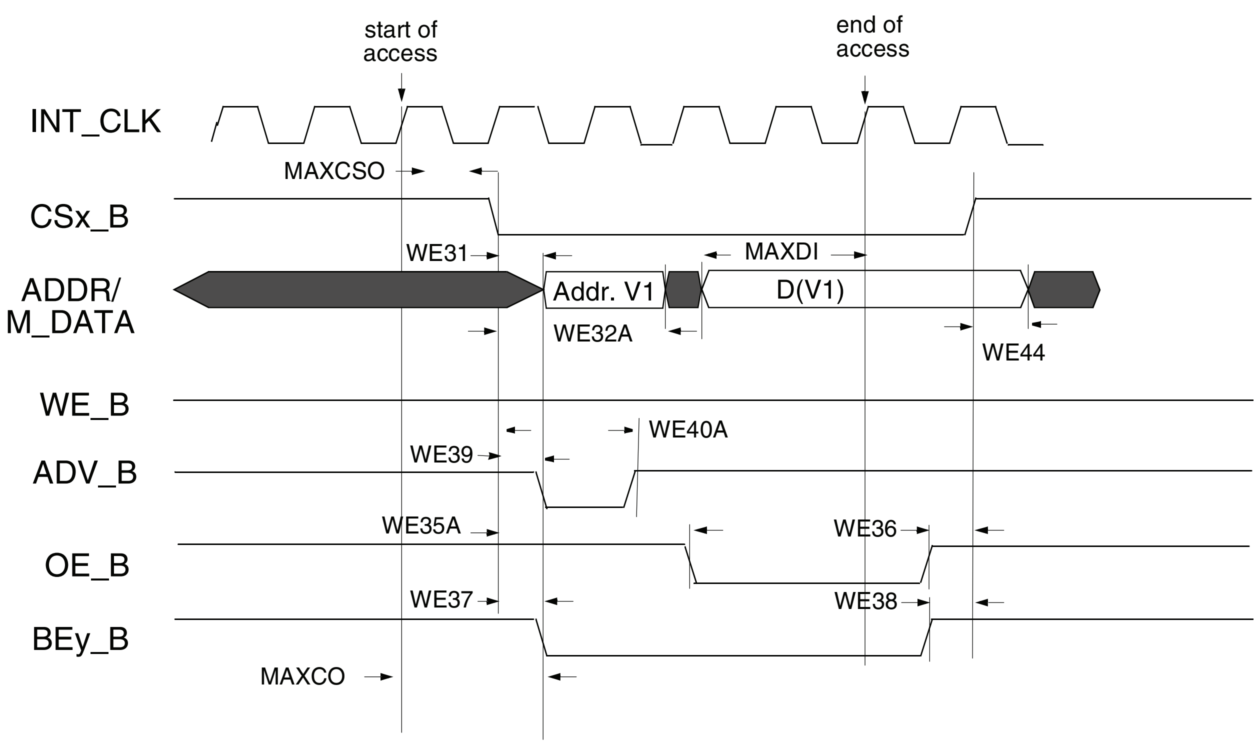


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 22 shows the basic timing parameters. The timing parameters for this diagram appear in Table 41.

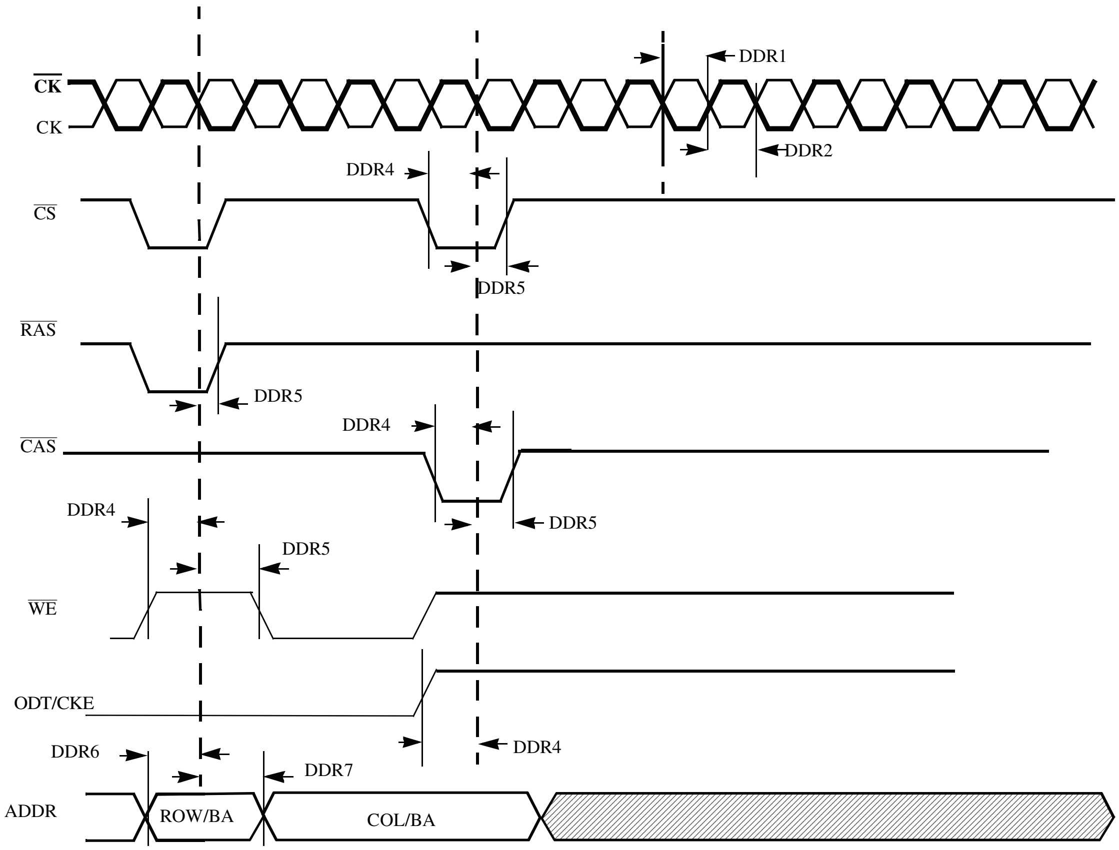


Figure 22. DDR3 Command and Address Timing Parameters

Table 41. DDR3/DDR3L Timing Parameter Table

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tCK
DDR2	CK clock low-level width	tCL	0.47	0.53	tCK
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	800	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	580	—	ps
DDR6	Address output setup time	tIS	800	—	ps
DDR7	Address output hold time	tIH	580	—	ps

4.10.3.2 Read and Write Timing

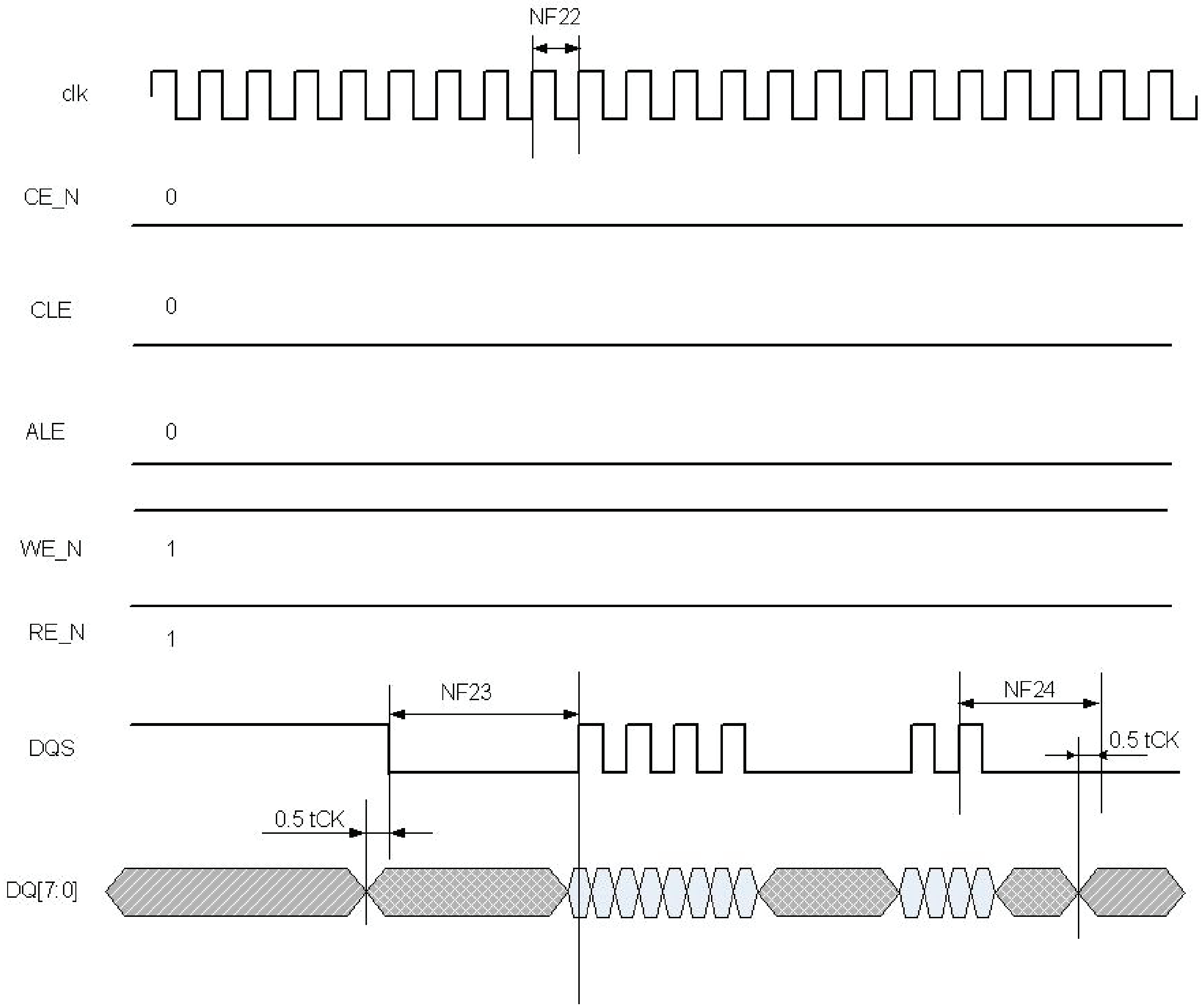


Figure 36. Samsung Toggle Mode Data Write Timing

Table 55. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5{*}t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 23, "GPIO DC Parameters," on page 37.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Table 61. RGMII Signal Switching Specifications[1] (continued)

Symbol	Description	Min.	Max.	Unit
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ps
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

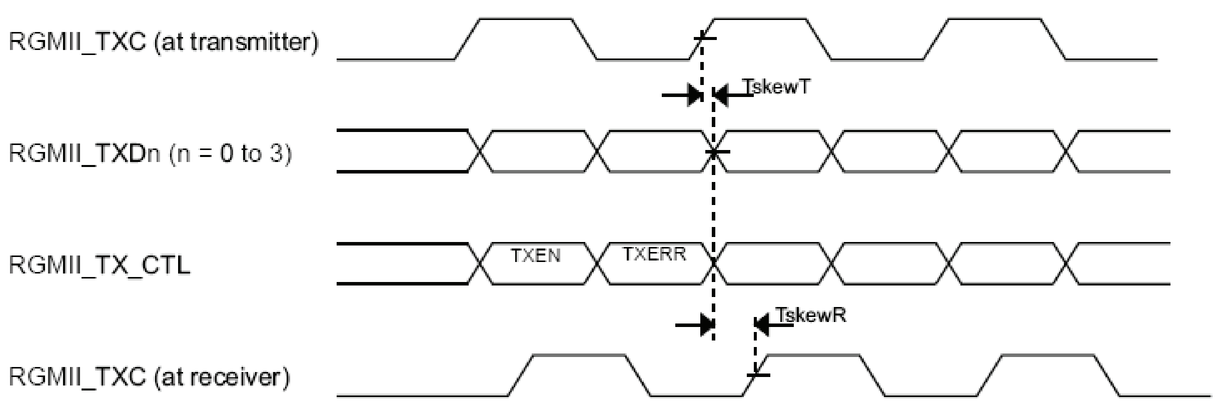


Figure 50. RGMII Transmit Signal Timing Diagram Original

Table 68. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$\mathrm{Tdicp} = \begin{cases} T_{\mathrm{diclk}} \times \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}, & \text{for integer } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \\ T_{\mathrm{diclk}}\left(\mathrm{floor}\left[\dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{\mathrm{T}}\mathrm{dicp} = T_{\mathrm{diclk}} \times \frac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$\mathrm{Accuracy} = (0.5 \times T_{\mathrm{diclk}}) \pm 0.62\mathrm{ns}$$

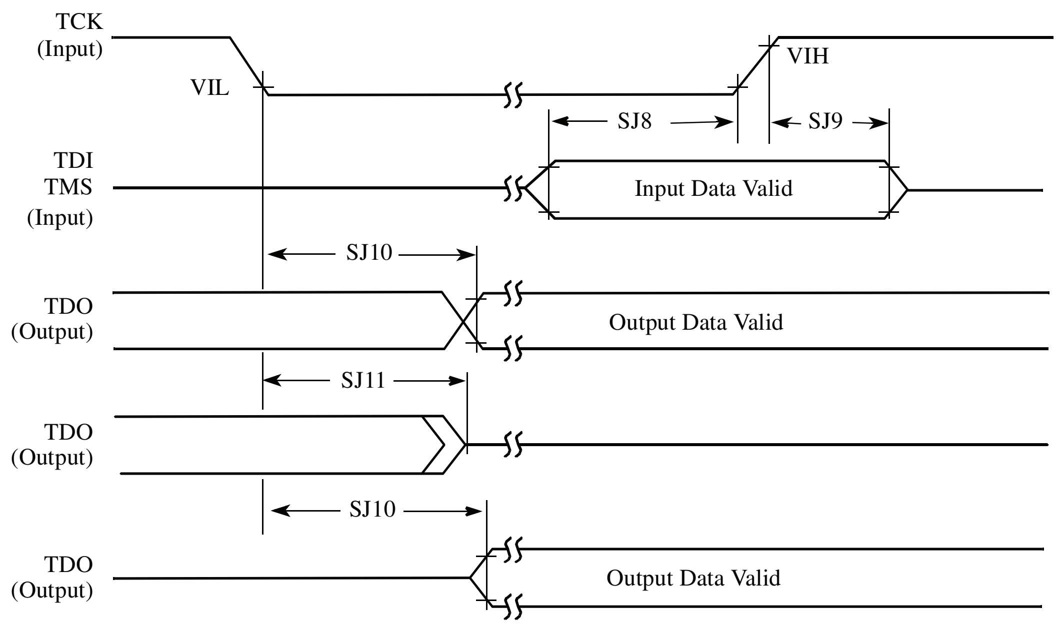


Figure 87. Test Access Port Timing Diagram

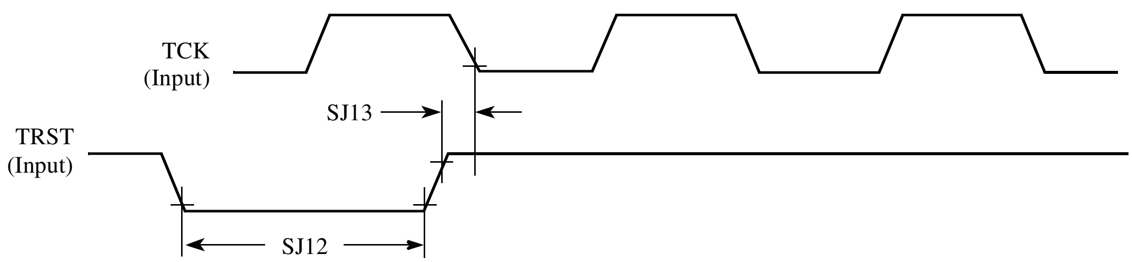
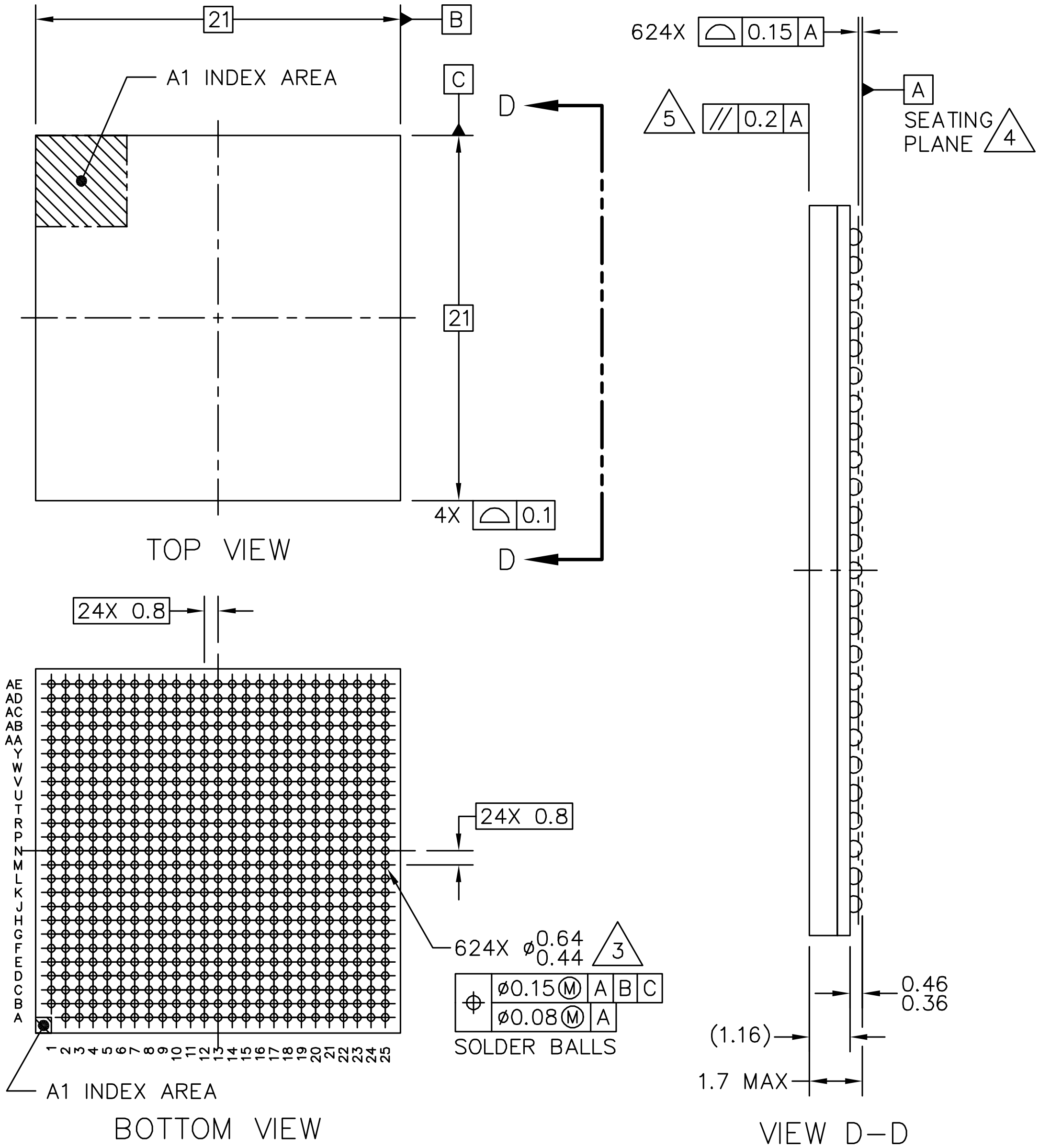


Figure 88. $\overline{\text{TRST}}$ Timing Diagram

Table 75. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: PBGA, LOW PROFILE, FINE PITCH, 624 I/O, 21 X 21 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00404D	REV: 0
	CASE NUMBER: 2240–01	27 SEP 2011
	STANDARD: NON–JEDEC	

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[19]	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[20]	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[21]	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[22]	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[23]	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[24]	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[25]	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[26]	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[27]	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[28]	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[29]	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[30]	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[31]	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[0]	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[1]	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[10]	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[11]	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[12]	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[13]	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[14]	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[15]	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[2]	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[3]	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[4]	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[5]	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[6]	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[7]	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[8]	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[9]	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[0]	Output	High

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[2]	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[3]	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[4]	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[5]	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[6]	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[7]	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[10]	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[9]	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	src.RESET_B	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH					
PCIE_RXP	B2	PCIE_VPH					
PCIE_TXM	A3	PCIE_VPH					
PCIE_TXP	B3	PCIE_VPH					
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVS_ WAKEUP_ALARM	Output	Low
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm.PMIC_VSTBY_RE Q	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src.POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[25]	Input	100 kΩ pull-up
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[27]	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[28]	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[29]	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[24]	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[30]	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[20]	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[21]	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[22]	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[23]	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[26]	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[19]	Input	100 kΩ pull-down

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
RTC_XTALI	D9	VDD_SNVS_CAP					
RTC_XTALO	C9	VDD_SNVS_CAP					
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[20]	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[18]	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[16]	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[17]	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[19]	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[21]	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[10]	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[11]	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[15]	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[14]	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[13]	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[12]	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[3]	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[2]	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[4]	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[5]	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[6]	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[7]	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[1]	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[0]	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[18]	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[17]	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[8]	Input	100 kΩ pull-up
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[10]	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[8]	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[10]	Input	100 kΩ pull-up

Table 94. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

N	P	R	T	U	V	W	Y
CSI0_DAT4	CSI0_PIXCLK	GPIO_17	GPIO_2	LVDS0_TX0_P	LVDS0_TX2_P	LVDS0_TX3_P	LVDS1_TX0_N
CSI0_VSYNC	CSI0_DAT5	GPIO_16	GPIO_9	LVDS0_TX0_N	LVDS0_TX2_N	LVDS0_TX3_N	LVDS1_TX0_P
CSI0_DAT7	CSI0_DATA_EN	GPIO_7	GPIO_6	LVDS0_TX1_P	LVDS0_CLK_P	GND	LVDS1_CLK_N
CSI0_DAT6	CSI0_MCLK	GPIO_5	GPIO_1	LVDS0_TX1_N	LVDS0_CLK_N	KEY_ROW2	LVDS1_CLK_P
CSI0_DAT9	GPIO_19	GPIO_8	GPIO_0	KEY_COL3	KEY_ROW4	KEY_COL0	GND
CSI0_DAT8	GPIO_18	GPIO_4	KEY_COL4	KEY_ROW1	KEY_ROW0	KEY_COL2	DRAM_RESET
NVCC_CSI	NVCC_GPIO	GPIO_3	KEY_ROW3	KEY_COL1	NVCC_LVDS2P5	GND	DRAM_D20
GND	GND	GND	GND	GND	GND	GND	DRAM_D21
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_DRAM	GND	DRAM_D19
GND	GND	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	GND	DRAM_D25
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	GND	GND	NVCC_DRAM	GND	DRAM_SDCKE0
NC	GND	GND	GND	GND	NVCC_DRAM	GND	DRAM_A15
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	GND	DRAM_A7
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	DRAM_A4	DRAM_A3
GND	GND	GND	GND	GND	NVCC_DRAM	GND	DRAM_SDBA1
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_DRAM	GND	DRAM_CS0
VDDPU_CAP	VDDPU_CAP	GND	GND	GND	NVCC_DRAM	GND	DRAM_D36
GND	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	DRAM_D37
DI0_DISP_CLK	NVCC_LCD	NVCC_ENET	GND	GND	GND	GND	DRAM_D40
DI0_PIN3	DISP0_DAT4	DISP0_DAT13	DISP0_DAT21	ENET_TXD0	ENET_MDC	ENET_TXD1	DRAM_D44
DI0_PIN15	DISP0_DAT3	DISP0_DAT10	DISP0_DAT16	ENET_CRS_DV	ENET_TX_EN	ENET_RXD0	DRAM_DQM7
EIM_BCLK	DISP0_DAT1	DISP0_DAT8	DISP0_DAT15	DISP0_DAT20	ENET_REF_CLK	ENET_RXD1	DRAM_D59
EIM_DA14	DISP0_DAT2	DISP0_DAT6	DISP0_DAT11	DISP0_DAT19	ENET_MDIO	ENET_RX_ER	DRAM_D62
EIM_DA15	DISP0_DAT0	DISP0_DAT7	DISP0_DAT12	DISP0_DAT17	DISP0_DAT22	DISP0_DAT23	GND
DI0_PIN2	DI0_PIN4	DISP0_DAT5	DISP0_DAT9	DISP0_DAT14	DISP0_DAT18	DRAM_D63	DRAM_D58
N	P	R	T	U	V	W	Y

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