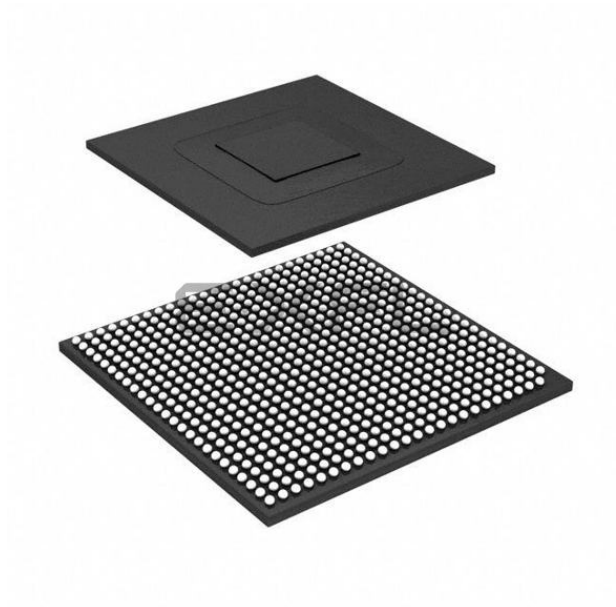

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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s5evm10ac

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supply voltages[6]	NVCC_CSI, NVCC_EIM, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	
	NVCC_LVDS2P5[7] NVCC_MIPI	2.25	2.5	2.75	V	
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	
	HDMI_VPH	2.25	2.5	2.75	V	
PCIe supply voltages	PCIE_VP	1.023	1.1	1.225	V	
	PCIE_VPH	2.325	2.5	2.75	V	
	PCIE_VPTX	1.023	1.1	1.225	V	
Junction temperature Extended consumer	T_J	-20	—	105	°C	Refer to Consumer qualification report for details.
Junction temperature Standard consumer	T_J	0	—	95	°C	Refer to Consumer qualification report for details.

1 Applying the maximum voltage results in maximum power consumption and heat generation. Freescale recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDDARM_IN and VDDSOC_IN must be 125 mV higher than the LDO Output Set Point for correct regulator supply voltage.

3 VDDSOC_CAP and VDDPU_CAP must be equal.

4 VDDSOC and VDDPU output voltage must be set to this rule: VDDARM - VDDSOC/PU < 100 mV.

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not and associated IO pins need to have a Pullup or Pulldown resistor applied to limit any floating gate current.

7 This supply also powers the pre-drivers of the DDR IO pins, hence, it must be always provided, even when LVDS is not used

Table 10 shows on-chip LDO regulators that can supply on-chip loads.

Table 10. On-Chip LDOs[1] and their On-Chip Loads

Voltage Source	Load	Comment
VDDHIGH_CAP	NVCC_LVDS2P5	Board-level connection to VDDHIGH_CAP
	NVCC_MIPI	
	HDMI_VPH	
	PCIE_VPH	

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 11 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available.

On-chip 40 kHz ring oscillator—this clock source has the following characteristics:

- Approximately 25 µA more Idd than crystal oscillator
- Approximately ±50% tolerance
- No external component required
- Starts up quicker than 32 kHz crystal oscillator

External crystal oscillator with on-chip support circuit:

- At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- Higher accuracy than ring oscillator
- If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 12. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN	996 MHz ARM clock based on Power Virus operation	2200	mA
VDDSOC_IN	996 MHz ARM clock	1260	mA
VDDHIGH_IN		125[1]	mA
VDD_SNVS_IN		275[2]	µA
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)		25[3]	mA
Primary Interface (IO) Supplies			

— VDDARM_IN supply must be turned ON together with VDDSOC_IN supply or not delayed more than 1 ms

— VDDARM_CAP must not exceed VDDSOC_CAP by more than 50 mV.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6Solo/6DualLite Reference Manual* for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of

Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

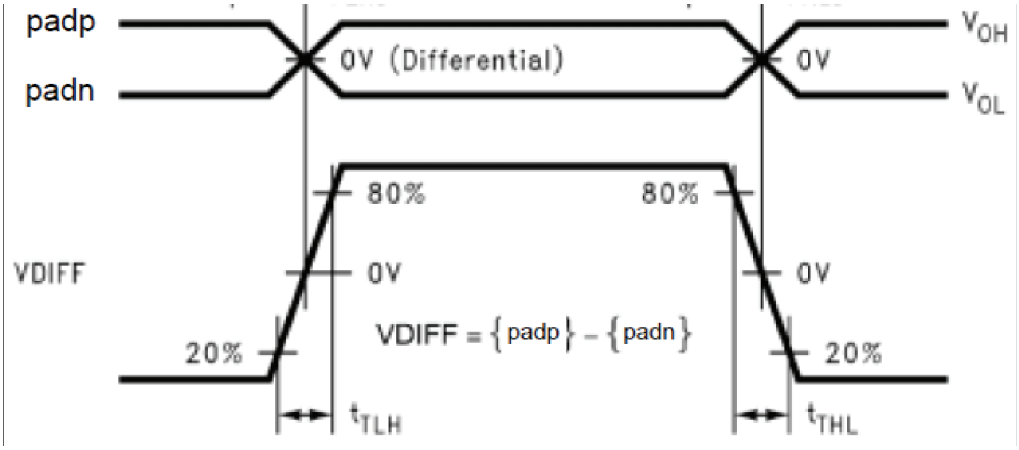


Figure 6. Differential LVDS Driver Transition Time Waveform

Table 31 shows the AC parameters for LVDS I/O.

Table 31. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} - t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

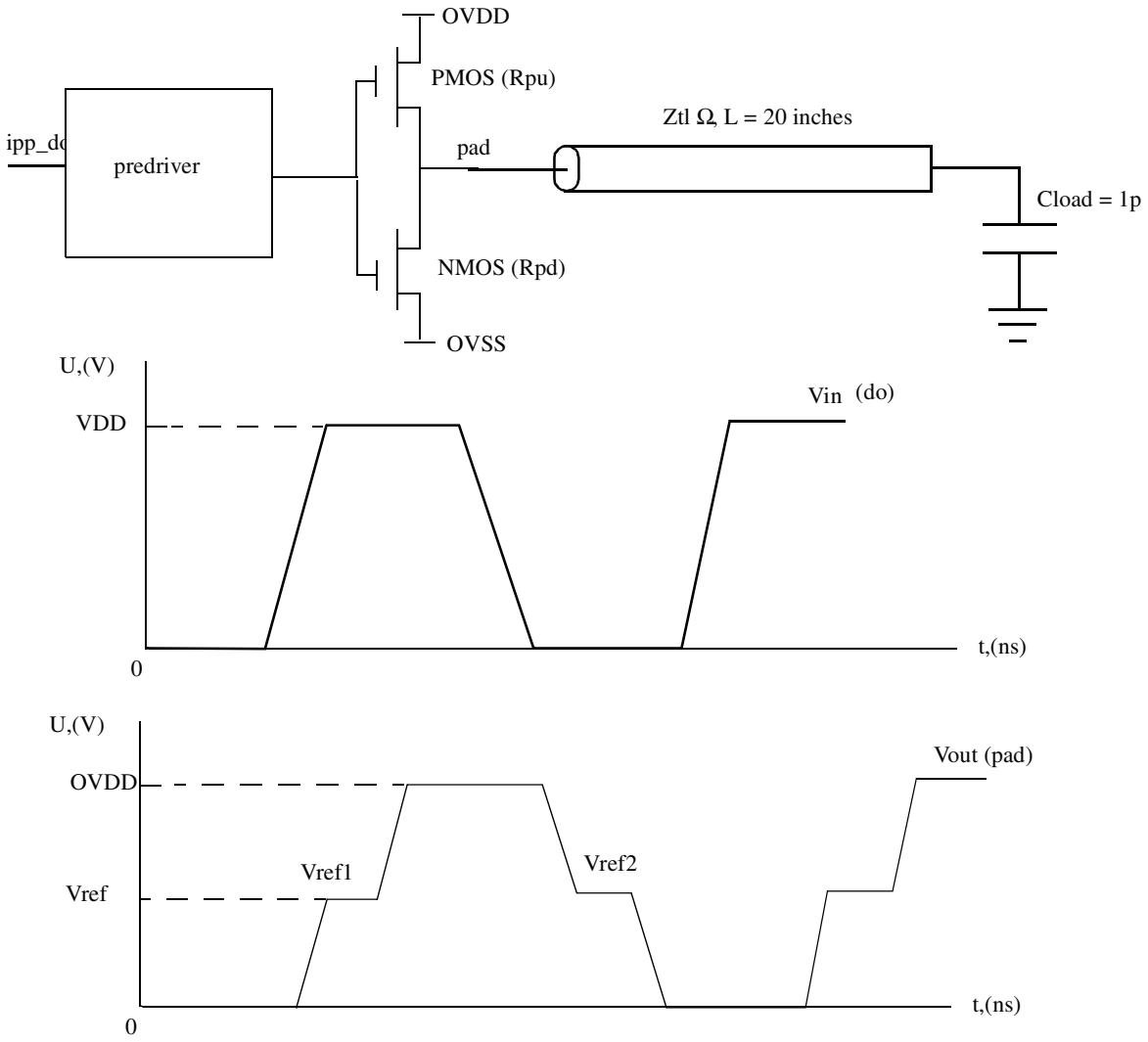
4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Solo/6DualLite processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 7. Impedance Matching Load for Measurement

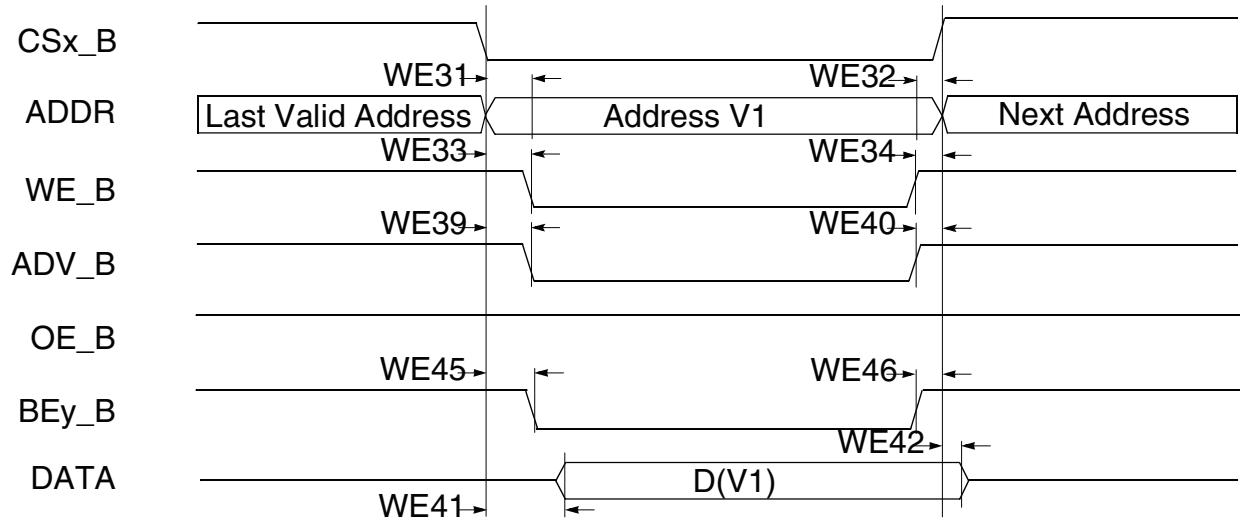


Figure 18. Asynchronous Memory Write Access

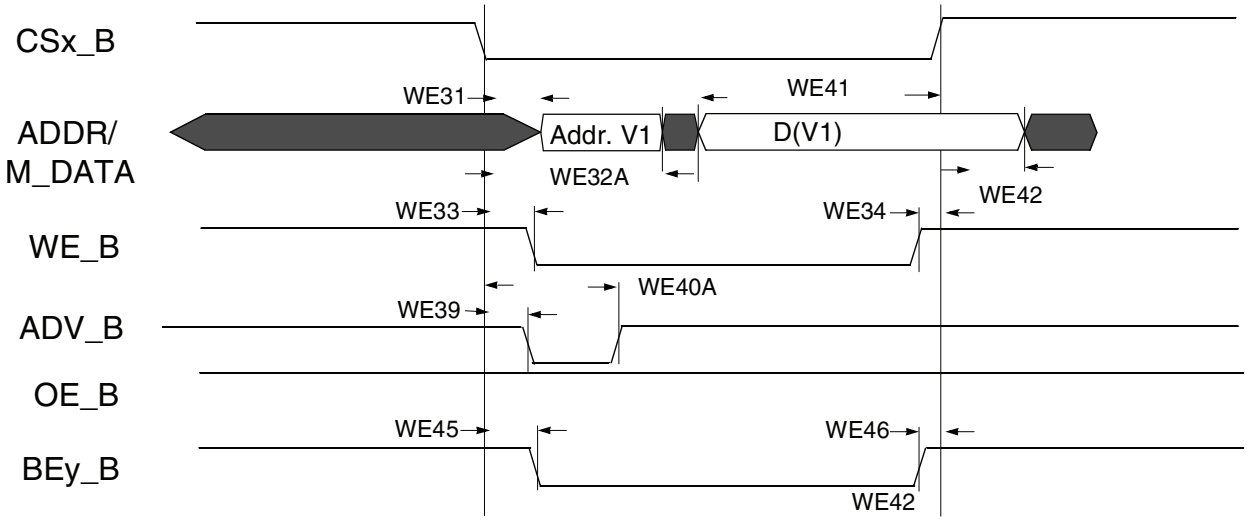


Figure 19. Asynchronous A/D Muxed Write Access

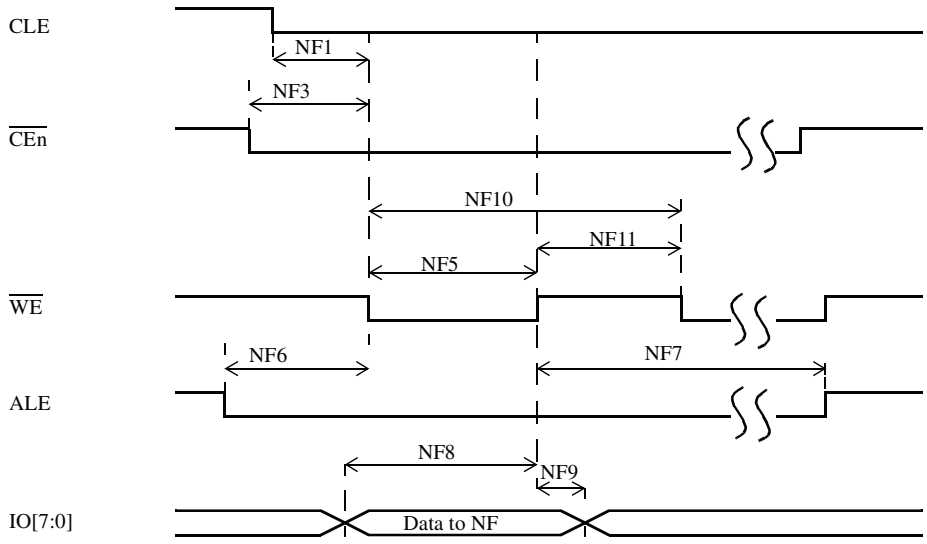


Figure 30. Write Data Latch Cycle Timing Diagram

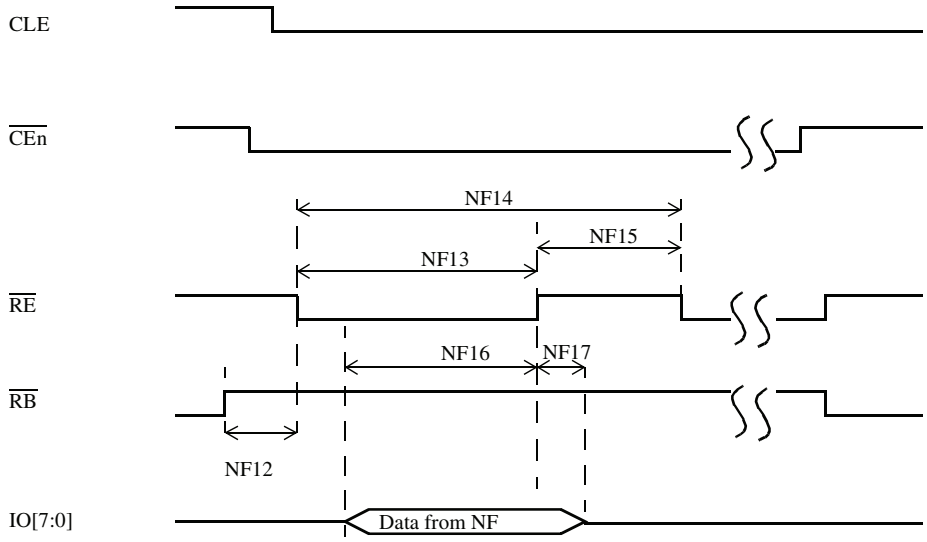


Figure 31. Read Data Latch Cycle Timing Diagram

Table 47. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1) x T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1) x T	—	20	—	ns
NF3	$\overline{\text{CEn}}$ setup time	tCS	(AS+1) x T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1) x T	—	20	—	ns

Table 48. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY x tCK	—	ns
NF19	CE# hold time	tCH	0.5 x tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5 x tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5 x tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

1 GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

For DDR Source sync mode, Figure 35 shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET(see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

4.11.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 52 shows the interface timing values. The number field in the table refers to timing signals found in Figure 40 and Figure 41.

Table 52. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period: • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 48 shows MII asynchronous input timings. Table 59 describes the timing parameters (M10–M15) shown in the figure.

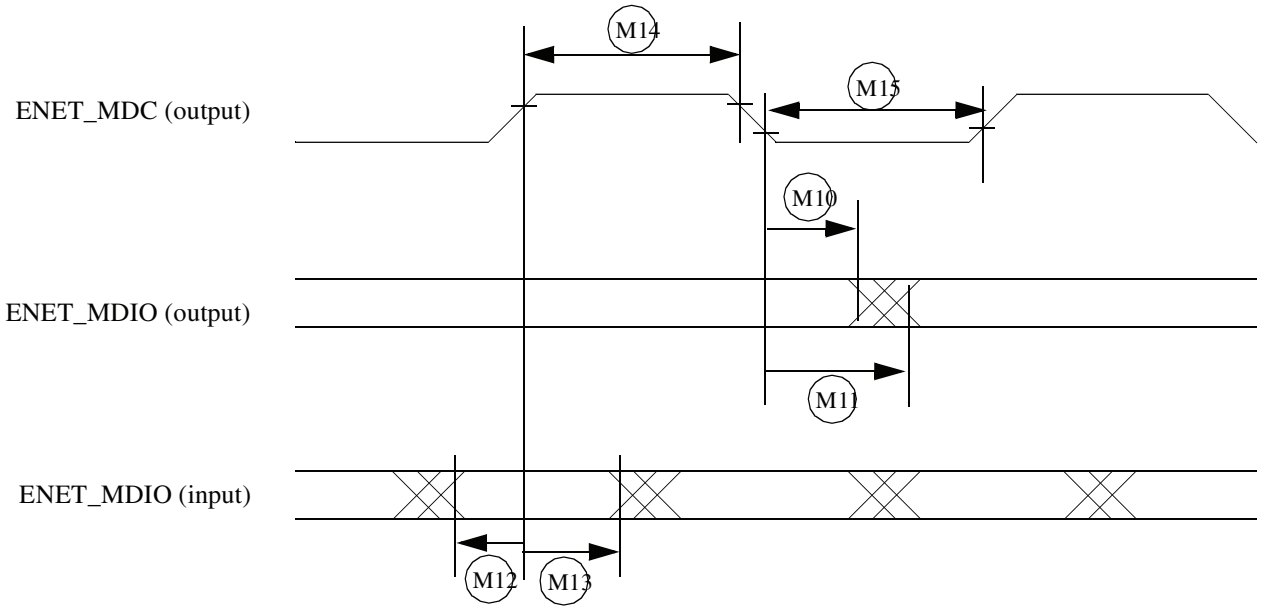


Figure 48. MII Serial Management Channel Timing Diagram

Table 59. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

Figure 49 shows RMII mode timings. Table 60 describes the timing parameters (M16–M21) shown in the figure.

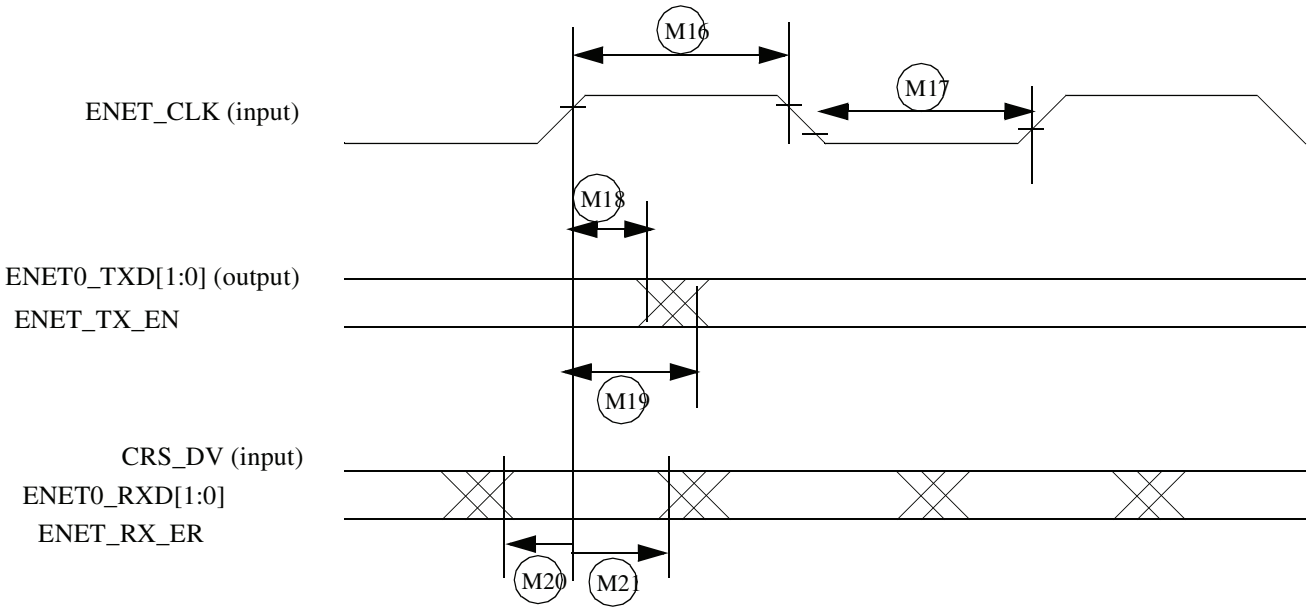


Figure 49. RMII Mode Signal Timing Diagram

Table 60. RMII Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	15	ns
M20	ENET0_RXD[1:0], CRS_DV(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET0_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.11.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 61. RGMII Signal Switching Specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps

NOTE

Table 67 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYCN) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 89 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Solo/6DualLite Fuse Map document and the System Boot chapter in *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 89. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	N/A	Boot Mode selection
BOOT_MODE0	Input	N/A	Boot Mode Selection

6.1.2 21 x 21 mm Supplies Contact Assignments and Functional Contact Assignments

Table 91 shows supplies contact assignments for the 21 x 21 mm package.

Table 91. 21 x 21 mm Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of the DDR interface
NVCC_EIM	K19, L19, M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the raw NAND Flash memories interface
NVCC_PLL_OUT	E8	
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DRAM_SDQS4_B	AE18	NVCC_DRAM			DRAM_SDQS4_B	-	-
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[5]	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM			DRAM_SDQS5_B	-	-
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[6]	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM			DRAM_SDQS6_B	-	-
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[7]	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM			DRAM_SDQS7_B	-	-
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDWE	Output	Low
DSI_CLK0M	H3	NVCC_MIPI	ANALOG				
DSI_CLK0P	H4	NVCC_MIPI	ANALOG				
DSI_D0M	G2	NVCC_MIPI	ANALOG				
DSI_D0P	G1	NVCC_MIPI	ANALOG				
DSI_D1M	H2	NVCC_MIPI	ANALOG				
DSI_D1P	H1	NVCC_MIPI	ANALOG				
EIM_A16	H25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[16]	Output	Low
EIM_A17	G24	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[17]	Output	Low
EIM_A18	J22	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[18]	Output	Low
EIM_A19	G25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[19]	Output	Low
EIM_A20	H22	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[20]	Output	Low
EIM_A21	H23	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[21]	Output	Low
EIM_A22	F24	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[22]	Output	Low
EIM_A23	J21	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[23]	Output	Low
EIM_A24	F25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[24]	Output	Low
EIM_A25	H19	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[25]	Output	Low
EIM_BCLK	N22	NVCC_EIM	GPIO	ALT0	weim.WEIM_BCLK	Output	Low
EIM_CS0	H24	NVCC_EIM	GPIO	ALT0	weim.WEIM_CS[0]	Output	High
EIM_CS1	J23	NVCC_EIM	GPIO	ALT0	weim.WEIM_CS[1]	Output	High
EIM_D16	C25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[16]	Input	100 kΩ pull-up
EIM_D17	F21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[17]	Input	100 kΩ pull-up
EIM_D18	D24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[18]	Input	100 kΩ pull-up

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
RTC_XTALI	D9	VDD_SNVS_CAP					
RTC_XTALO	C9	VDD_SNVS_CAP					
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[20]	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[18]	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[16]	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[17]	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[19]	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[21]	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[10]	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[11]	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[15]	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[14]	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[13]	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[12]	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[3]	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[2]	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[4]	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[5]	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[6]	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[7]	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[1]	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[0]	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[18]	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[17]	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[8]	Input	100 kΩ pull-up
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[10]	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[8]	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[10]	Input	100 kΩ pull-up

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[11]	Input	100 kΩ pull-up
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[12]	Input	100 kΩ pull-up
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[13]	Input	100 kΩ pull-up
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[14]	Input	100 kΩ pull-up
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[15]	Input	100 kΩ pull-up
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVS_TD1	Input	100 kΩ pull-down
TEST_MODE	E12	VDD_SNVS_IN	GPIO	ALT0	tcu.TEST_MODE	Input	100 kΩ pull-down
USB_H1_DN	F10	VDDUSB_CAP					
USB_H1_DP	E10	VDDUSB_CAP					
USB_OTG_CHD_B	B8	VDDUSB_CAP					
USB_OTG_DN	B6	VDDUSB_CAP					
USB_OTG_DP	A6	VDDUSB_CAP					
XTALI	A7	NVCC_PLL_OUT					
XTALO	B7	NVCC_PLL_OUT					
NC	A1						
NC	A12						
NC	A14						
NC	B12						
NC	B14						
NC	E1						
NC	E2						
NC	F1						
NC	F2						

1 DRAM_D32 to DRAM_D63 are only available for i.MX 6DualLite chip; for i.MX 6Solo chip, these pins are NC.

2 The state immediately after reset and before ROM firmware or software has executed.

Table 93. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

R	P	N	M	L	K	J	H
GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P
GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M
GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M
GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P
GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK
GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP
GND	GND	GND	GND	GND	GND	GND	GND
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
GND	GND	NC	GND	GND	GND	GND	GND
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
GND	GND	GND	GND	GND	GND	GND	GND
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND
NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25
DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21
DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0
DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16
R	P	N	M	L	K	J	H