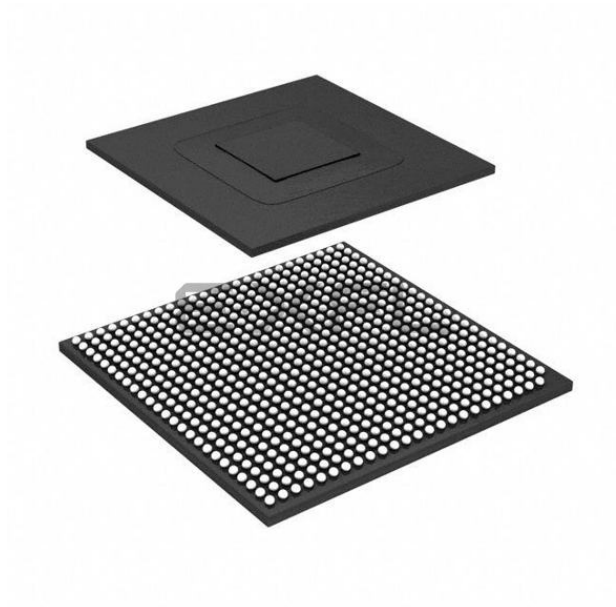

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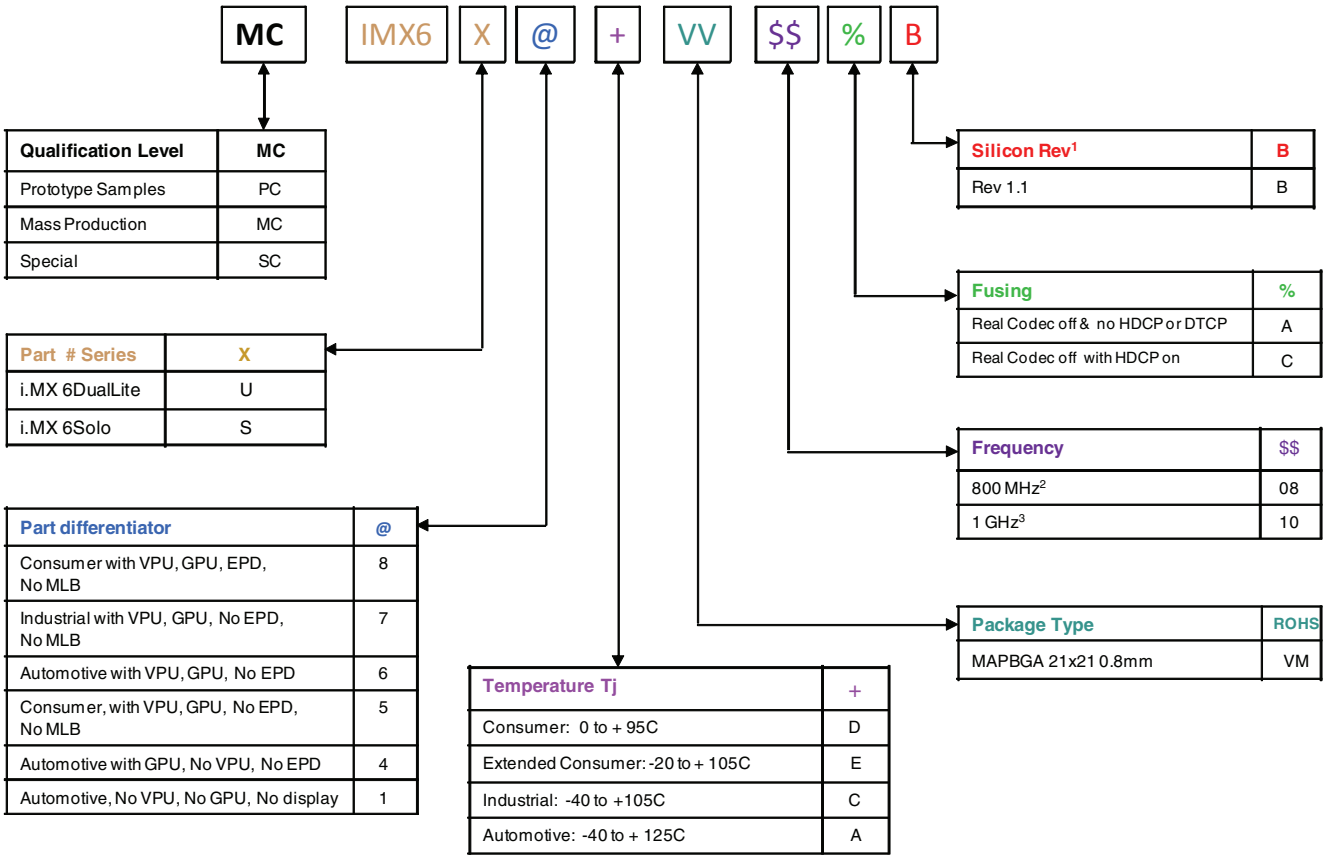
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s5evm10acr



1. See the freescale.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
3. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6DualLite and 6Solo

1.2 Features

The i.MX 6Solo/6DualLite processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- The i.MX 6Solo supports single ARM Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual ARM Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	-40	150	°C

1 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 8 displays the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	38 23	°C/W °C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	30 20	°C/W °C/W
Junction to Board[1,4]		$R_{\theta JB}$	14	°C/W
Junction to Case[1,5]		$R_{\theta JC}$	6	°C/W
Junction to Package Top[1,6]	Natural Convection	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

— VDDARM_IN supply must be turned ON together with VDDSOC_IN supply or not delayed more than 1 ms

— VDDARM_CAP must not exceed VDDSOC_CAP by more than 50 mV.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6Solo/6DualLite Reference Manual* for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of

2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Solo/6DualLite processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 35 lists the timing parameters.

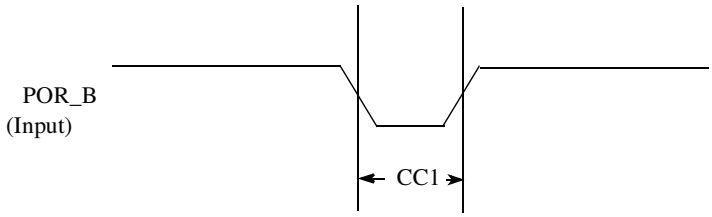


Figure 8. Reset Timing Diagram

Table 35. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid (input slope = 5 ns)	1	—	RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 36 lists the timing parameters.

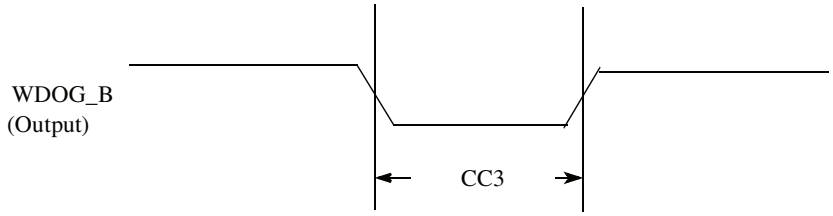


Figure 9. WDOG_B Timing Diagram

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 32 to Figure 34 show the write and read timing of Source Synchronous Mode.

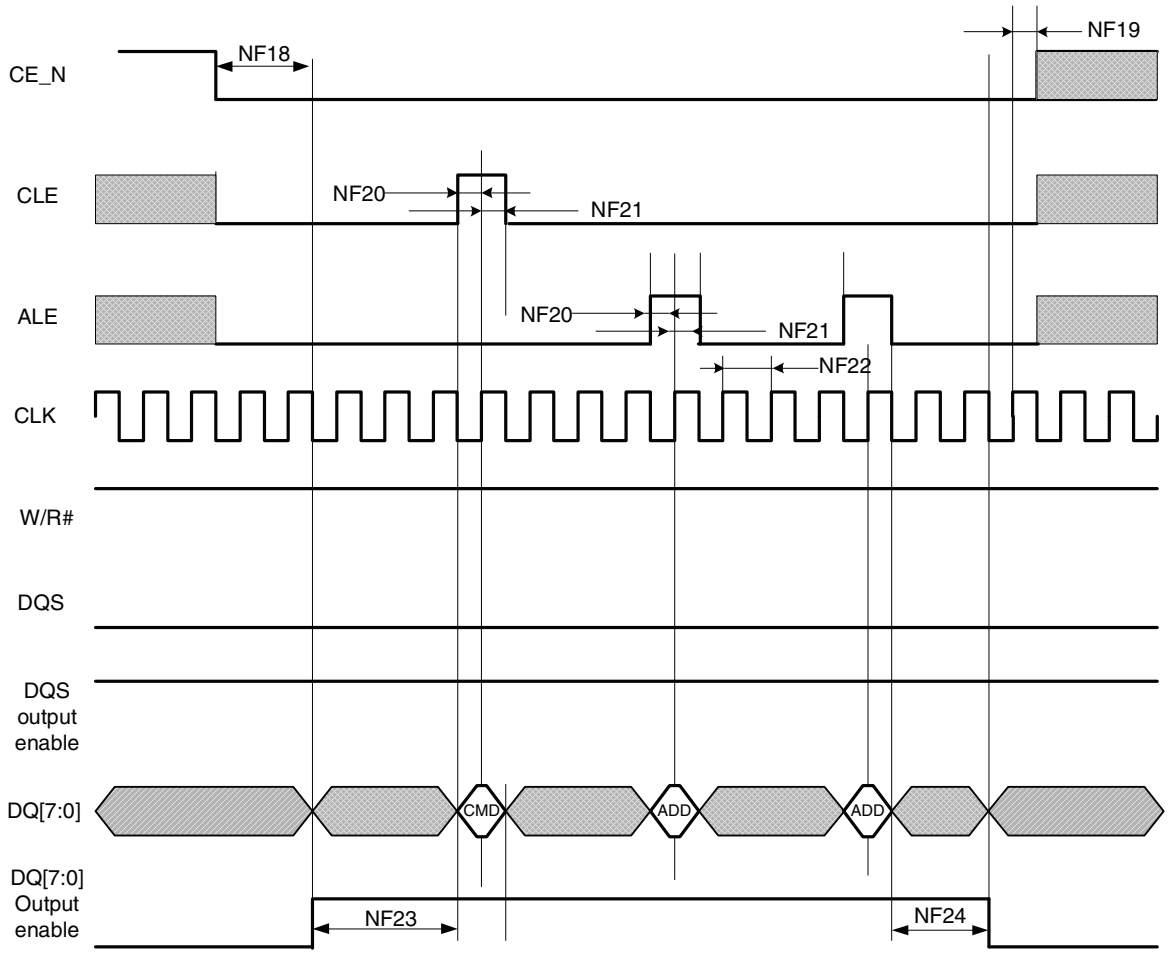


Figure 32. Source Synchronous Mode Command and Address Timing Diagram

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 42 depicts the timing of SD/eMMC4.3, and Table 53 lists the SD/eMMC4.3 timing characteristics.

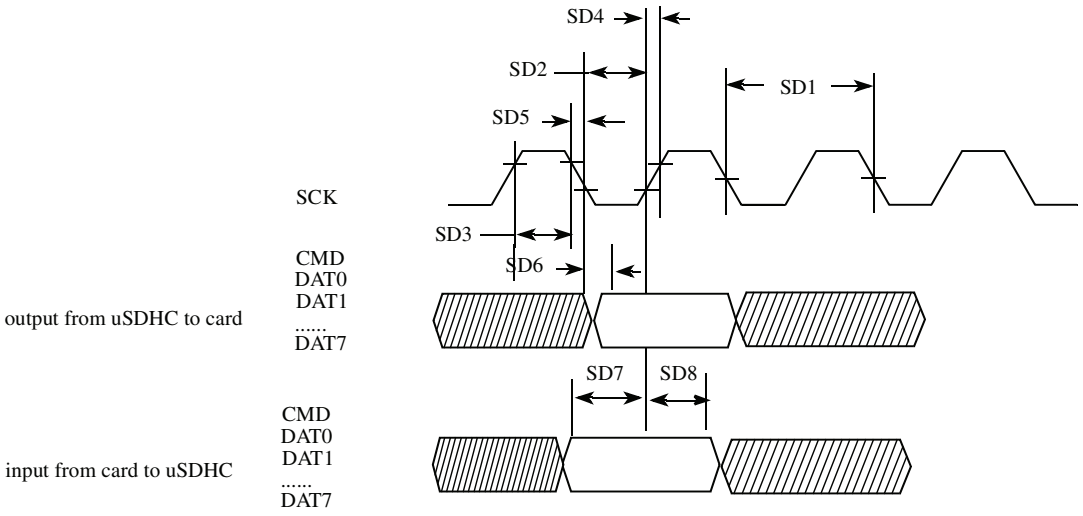


Figure 42. SD/eMMC4.3 Timing

Table 53. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Table 53. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	5.6	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4 (Dual Data Rate) AC Timing

Figure 43 depicts the timing of eMMC4.4. Table 54 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

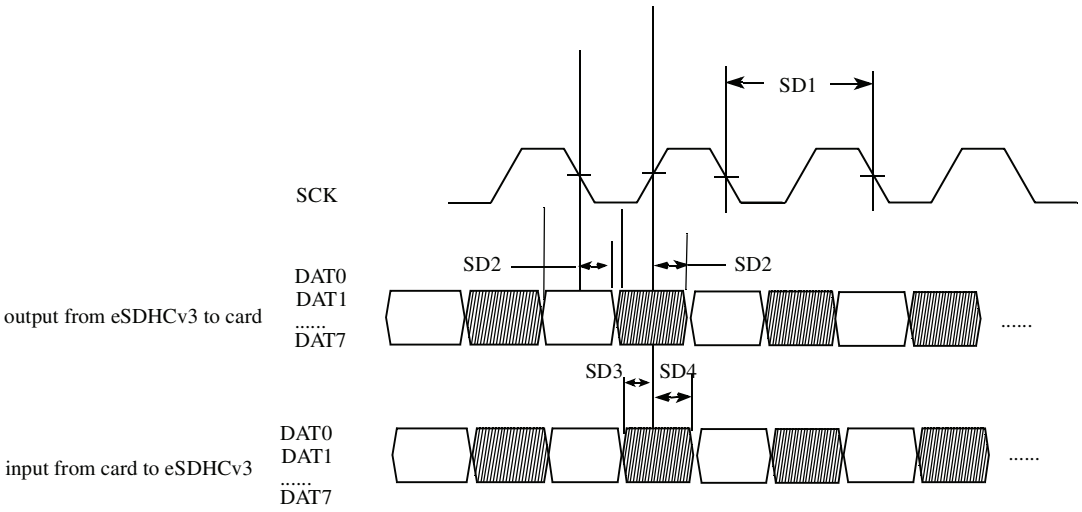


Figure 43. eMMC4.4 Timing

Table 54. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 48 shows MII asynchronous input timings. Table 59 describes the timing parameters (M10–M15) shown in the figure.

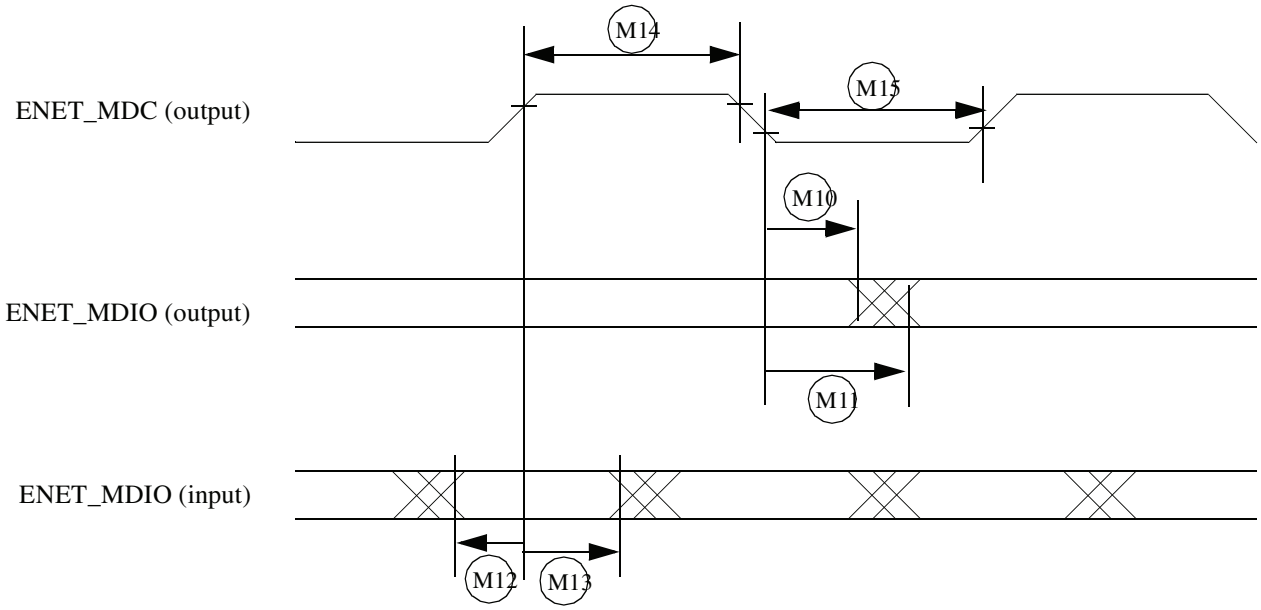


Figure 48. MII Serial Management Channel Timing Diagram

Table 59. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 μs.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

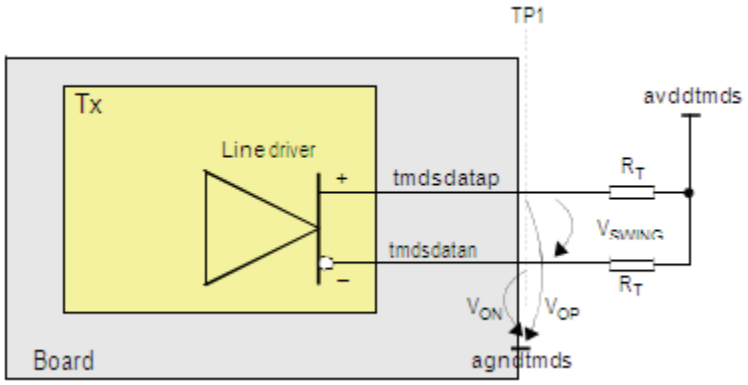


Figure 53. Driver Measuring Conditions

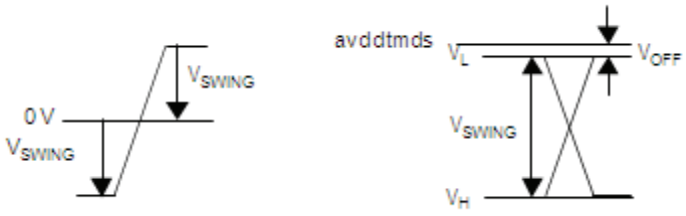


Figure 54. Driver Definitions

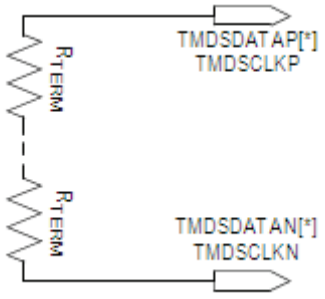


Figure 55. Source Termination

4.11.12.2 MIPI D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 69 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

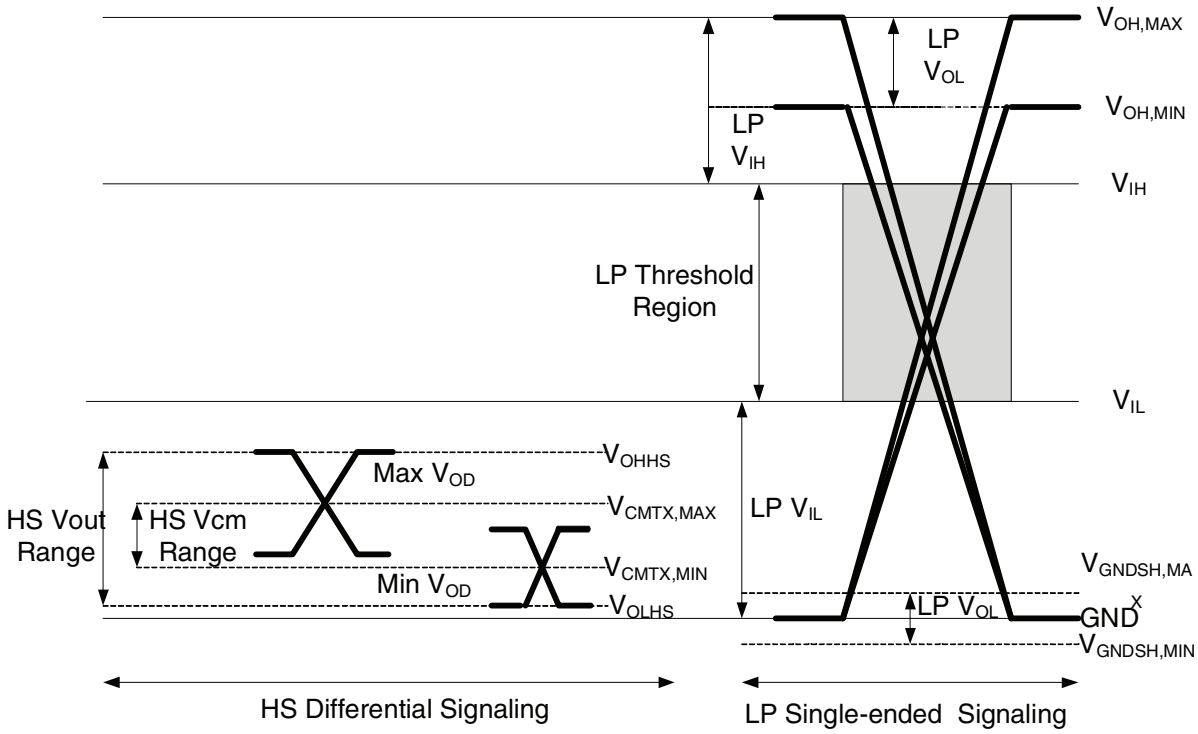


Figure 69. D-PHY Signaling Levels

4.11.12.3 MIPI HS Line Driver Characteristics

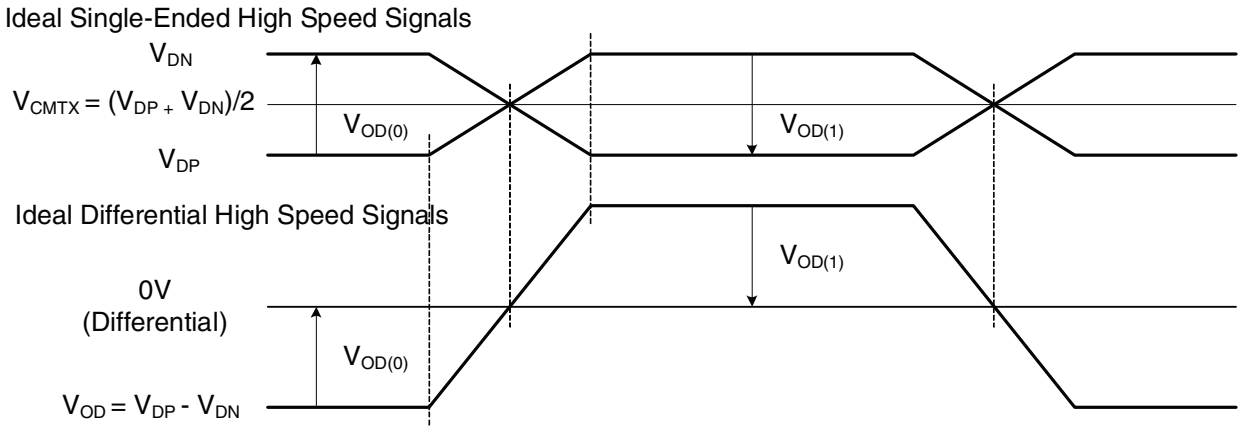


Figure 70. Ideal Single-ended and Resulting Differential HS Signals

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

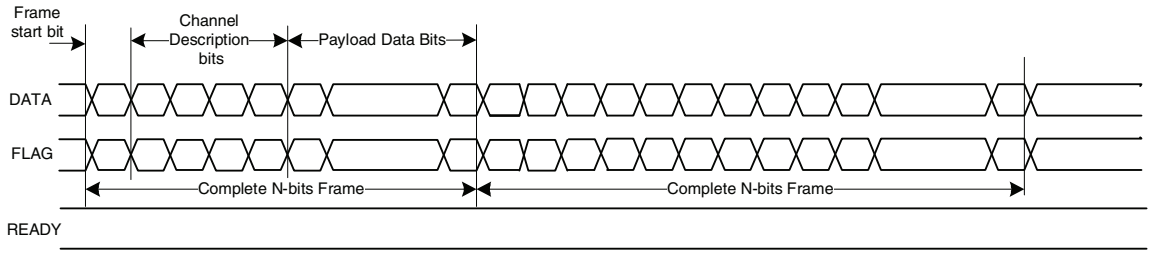


Figure 82. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 73. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10.0 ns	5.00 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2.00 ns	2.00 ns	1.00 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50.0 ns	0.5.0 ns	0.25 ns
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4.00 ns	2.00 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns	1.75 ns

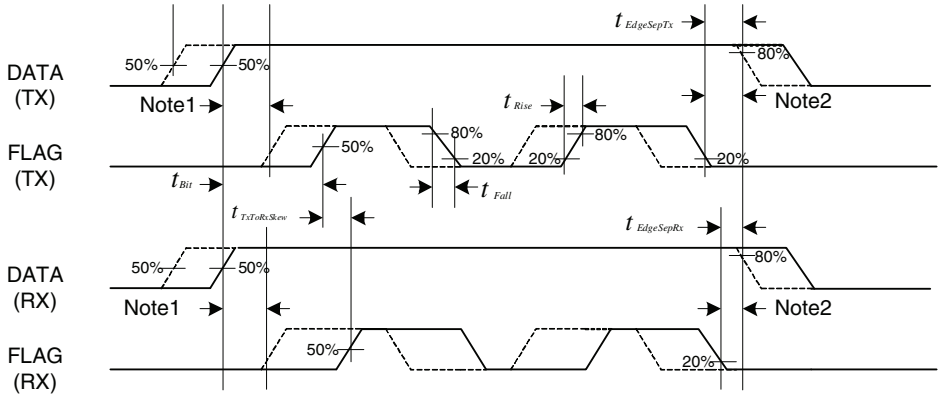


Figure 83. DATA and FLAG Signal Timing

Note:

1 This case shows that the DATA signal has slowed down more compared to the FLAG signal

2 This case shows that the FLAG signal has slowed down more compared to the DATA signal.

4.11.18.2 SSI Receiver Timing with Internal Clock

Figure 92 depicts the SSI receiver internal clock timing and Table 79 lists the timing parameters for the receiver timing with the internal clock.

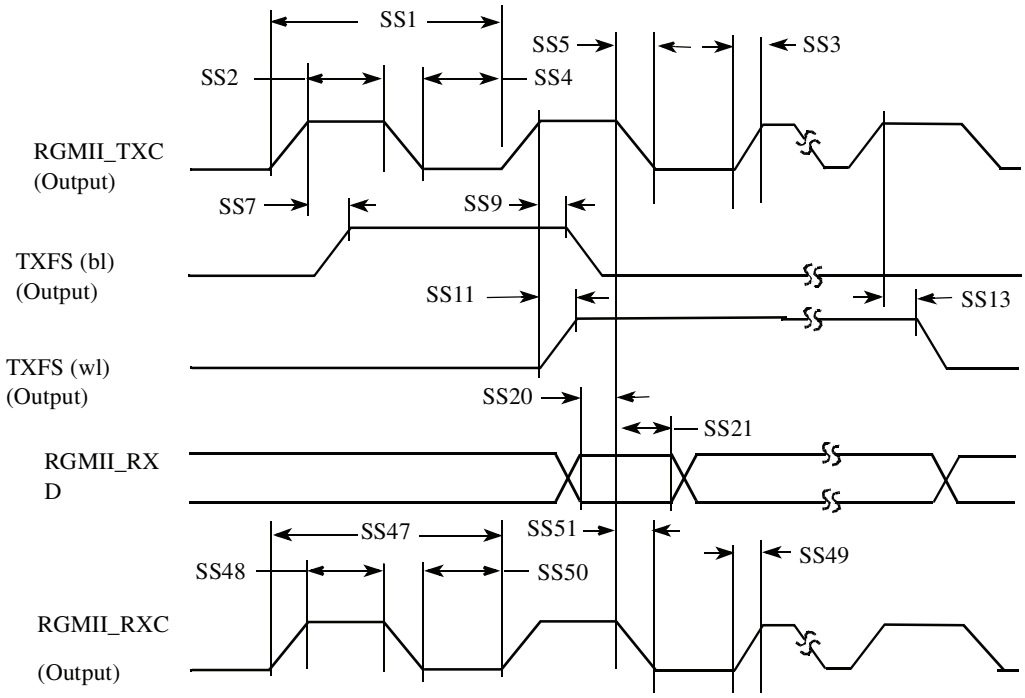


Figure 92. SSI Receiver Internal Clock Timing Diagram

Table 79. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

4.11.18.4 SSI Receiver Timing with External Clock

Figure 94 depicts the SSI receiver external clock timing and Table 81 lists the timing parameters for the receiver timing with the external clock.

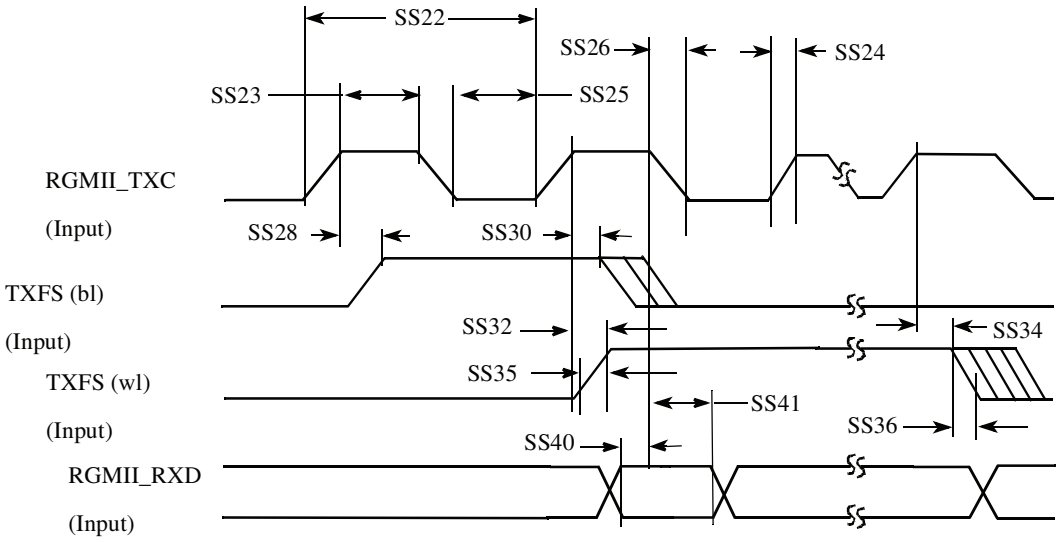


Figure 94. SSI Receiver External Clock Timing Diagram

Table 81. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	-10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	-10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

[1] The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.20 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.11.20.1 Transmit Timing

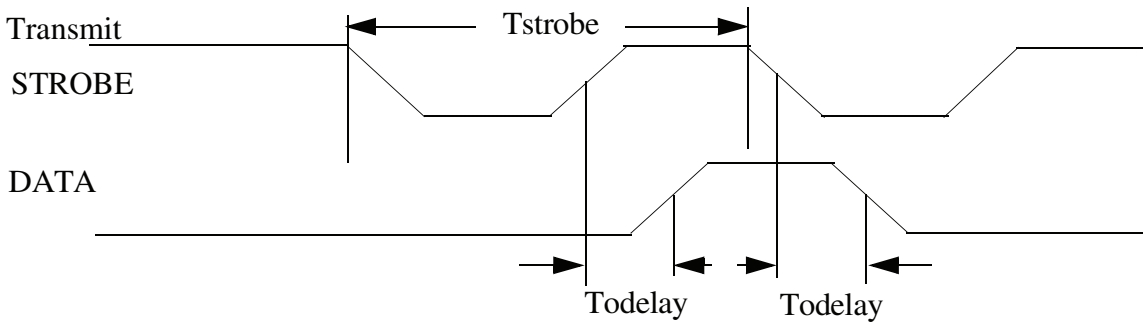
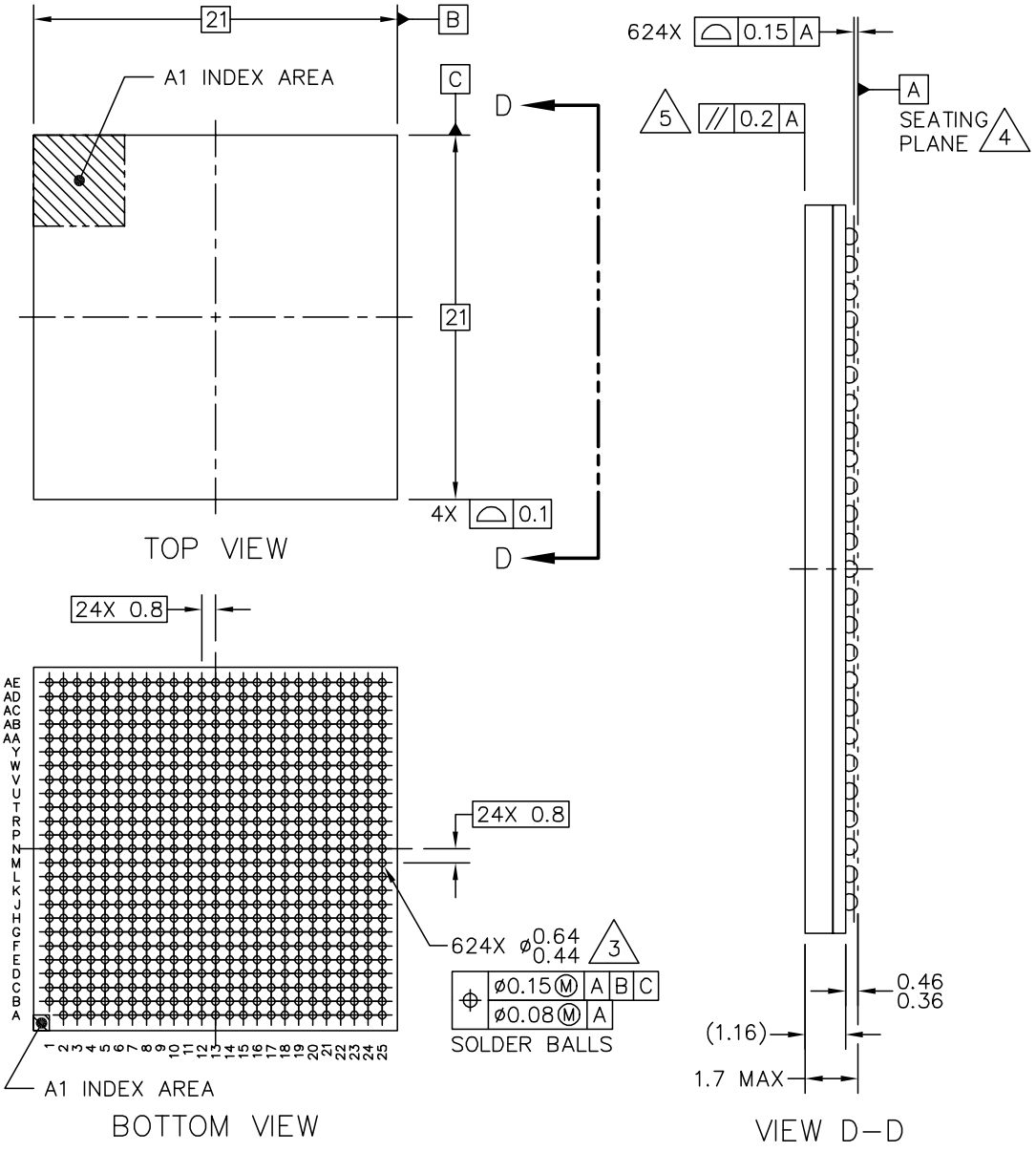


Figure 99. USB HSIC Transmit Waveform

Table 87. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points



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TITLE: PBGA, LOW PROFILE, FINE PITCH, 624 I/O, 21 X 21 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00404D	REV: O
	CASE NUMBER: 2240–01	27 SEP 2011
	STANDARD: NON–JEDEC	

Table 91. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NC	G13	
NC	N12	

Table 92 shows an alpha-sorted list of functional contact assignments for the 21 x 21 mm package.

Table 92. 21 x 21 mm Functional Contact Assignments[1]

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[0]	Input	100 kΩ pull-down
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[1]	Input	100 kΩ pull-down
CLK1_N	C7	VDDHIGH_CAP					
CLK1_P	D7	VDDHIGH_CAP					
CLK2_N	C5	VDDHIGH_CAP					
CLK2_P	D5	VDDHIGH_CAP					
CSI_CLK0M	F4	NVCC_MIPI	ANALOG				
CSI_CLK0P	F3	NVCC_MIPI	ANALOG				
CSI_D0M	E4	NVCC_MIPI	ANALOG				
CSI_D0P	E3	NVCC_MIPI	ANALOG				
CSI_D1M	D1	NVCC_MIPI	ANALOG				
CSI_D1P	D2	NVCC_MIPI	ANALOG				
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[28]	Input	100 kΩ pull-up
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[29]	Input	100 kΩ pull-up
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[30]	Input	100 kΩ pull-up
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[31]	Input	100 kΩ pull-up
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[0]	Input	100 kΩ pull-up
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[1]	Input	100 kΩ pull-up
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[2]	Input	100 kΩ pull-up
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[3]	Input	100 kΩ pull-up
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[4]	Input	100 kΩ pull-up
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[5]	Input	100 kΩ pull-up
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[22]	Input	100 kΩ pull-up
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[23]	Input	100 kΩ pull-up

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[9]	Input	100 kΩ pull-up
HDMI_CLKM	J5	HDMI_VPH					
HDMI_CLKP	J6	HDMI_VPH					
HDMI_D0M	K5	HDMI_VPH					
HDMI_D0P	K6	HDMI_VPH					
HDMI_D1M	J3	HDMI_VPH					
HDMI_D1P	J4	HDMI_VPH					
HDMI_D2M	K3	HDMI_VPH					
HDMI_D2P	K4	HDMI_VPH					
HDMI_HPD	K1	HDMI_VPH					
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	sjc.MOD	Input	100 kΩ pull-up
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	sjc.TCK	Input	47 kΩ pull-up
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	sjc.TDI	Input	47 kΩ pull-up
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	sjc.TDO	Output	Low
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	sjc.TMS	Input	47 kΩ pull-up
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	sjc.TRSTB	Input	47 kΩ pull-up
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[6]	Input	100 kΩ pull-up
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[8]	Input	100 kΩ pull-up
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[10]	Input	100 kΩ pull-up
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[12]	Input	100 kΩ pull-up
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[14]	Input	100 kΩ pull-up
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[7]	Input	100 kΩ pull-up
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[9]	Input	100 kΩ pull-up
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[11]	Input	100 kΩ pull-up
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[13]	Input	100 kΩ pull-up
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[15]	Input	100 kΩ pull-down
LVDS0_CLK_N	V4	NVCC_LVDS2P5					
LVDS0_CLK_P	V3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_CLK	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS2P5					
LVDS0_TX0_P	U1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX0	Input	Keeper

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
LVDS0_TX1_N	U4	NVCC_LVDS2P5					
LVDS0_TX1_P	U3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5					
LVDS0_TX2_P	V1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5					
LVDS0_TX3_P	W1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5					
LVDS1_CLK_P	Y4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5					
LVDS1_TX0_P	Y2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5					
LVDS1_TX1_P	AA1	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS2P5					
LVDS1_TX2_P	AB2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5					
LVDS1_TX3_P	AA4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX3	Input	Keeper
NC	A11						
NC	B11						
NC	B10						
NC	A10						
NC	A9						
NC	B9						
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[8]	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[7]	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[11]	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[14]	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[15]	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[16]	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[0]	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[1]	Input	100 kΩ pull-up

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[11]	Input	100 kΩ pull-up
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[12]	Input	100 kΩ pull-up
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[13]	Input	100 kΩ pull-up
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[14]	Input	100 kΩ pull-up
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[15]	Input	100 kΩ pull-up
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVS_TD1	Input	100 kΩ pull-down
TEST_MODE	E12	VDD_SNVS_IN	GPIO	ALT0	tcu.TEST_MODE	Input	100 kΩ pull-down
USB_H1_DN	F10	VDDUSB_CAP					
USB_H1_DP	E10	VDDUSB_CAP					
USB_OTG_CHD_B	B8	VDDUSB_CAP					
USB_OTG_DN	B6	VDDUSB_CAP					
USB_OTG_DP	A6	VDDUSB_CAP					
XTALI	A7	NVCC_PLL_OUT					
XTALO	B7	NVCC_PLL_OUT					
NC	A1						
NC	A12						
NC	A14						
NC	B12						
NC	B14						
NC	E1						
NC	E2						
NC	F1						
NC	F2						

1 DRAM_D32 to DRAM_D63 are only available for i.MX 6DualLite chip; for i.MX 6Solo chip, these pins are NC.

2 The state immediately after reset and before ROM firmware or software has executed.