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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6s8dvm10ab

NOTE

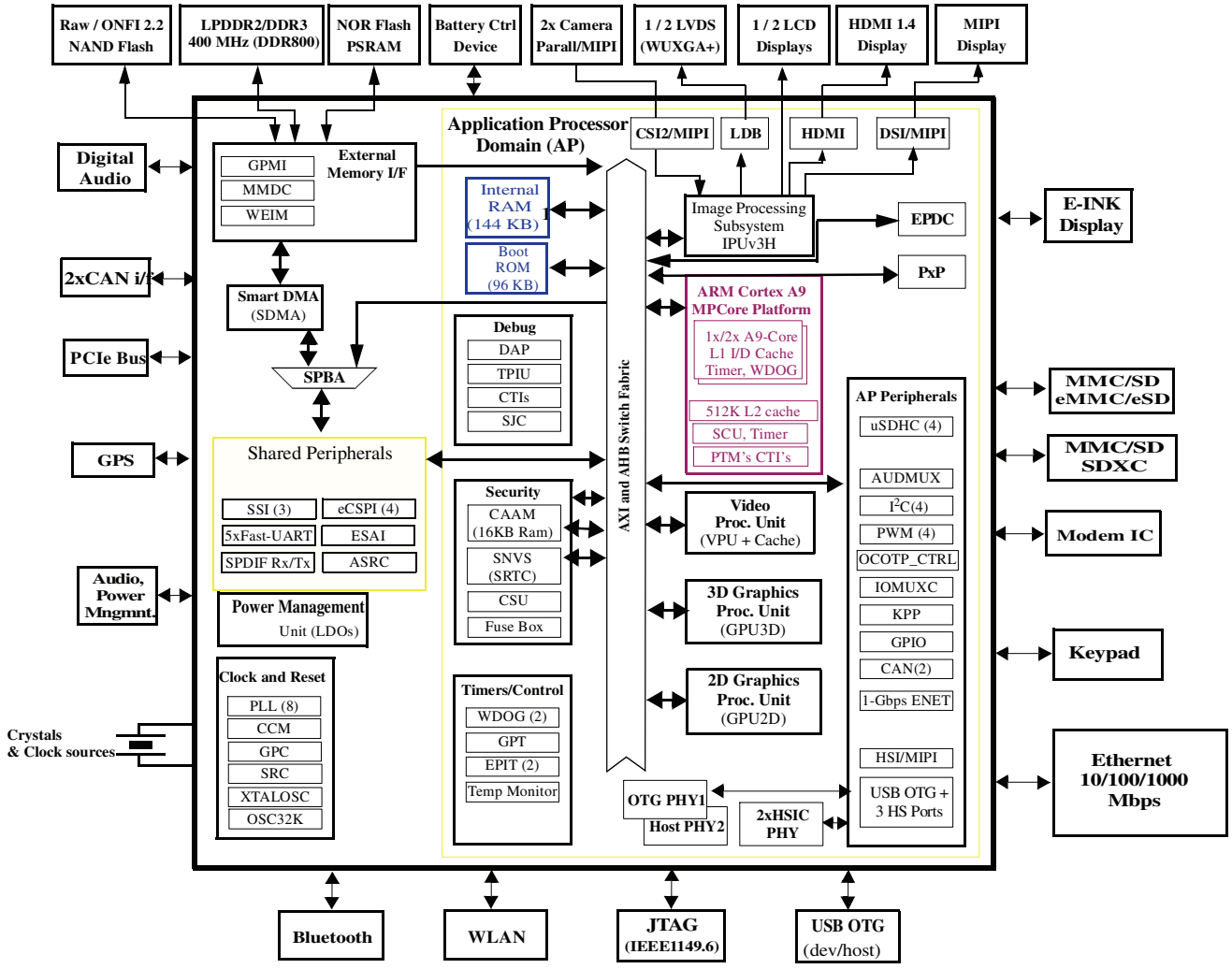
The actual feature set depends on the part numbers as described in Table 1, "Orderable Part Numbers," on page 3. Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Solo/6DualLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Solo/6DualLite processor system.



1 144 KB RAM including 16 KB RAM inside the CAAM.

[2] For i.MX 6Solo, there is only one A9-core platform in the chip; for i.MX 6DualLite, there are two A9-core platforms.

Figure 2. i.MX 6Solo/6DualLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6Solo/6DualLite processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Solo/6DualLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Core Platform includes 1x (Solo) Cortex-A9 core for i.MX 6Solo and 2x (Dual) Cortex-A9 cores for i.MX 6DualLite. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
APBH-DMA	NAND Flash and BCH ECC DMA controller	System Control Peripherals	DMA controller used for GPMI2 operation
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6Solo/6DualLite are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more that eight devices)
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
NVCC_LVDS2P5	The DDR pre-drivers share the NVCC_LVDS2P5 ball with the LVDS interface. This ball can be shorted to VDDHIGH_CAP on the circuit board.
VDD_FA FA_ANA	These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND.
GPANAIO	This signal is reserved for Freescale manufacturing use only. User must leave this connection floating.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6Solo/6DualLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	In normal mode may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for Freescale factory use. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
PCIE_REXT	The impedance calibration process requires connection of reference resistor 200 Ω 1% precision resistor on PCIE_REXT pad to ground.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
CSI_REXT	MIPI CSI PHY reference resistor. Use 6.04 KΩ 1% resistor connected between this pad and GND
DSI_REXT	MIPI DSI PHY reference resistor. Use 6.04 KΩ 1% resistor connected between this pad and GND

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
CCM	CLK1_N, CLK1_P, CLK2_N, CLK2_P	Float
CSI	CSI_CLK0M, CSI_CLK0P, CSI_D0M, CSI_D0P, CSI_D1M, CSI_D1P, CSI_REXT	Float
DSI	DSI_CLK0M, DSI_CLK0P, DSI_D0M, DSI_D0P, DSI_D1M, DSI_D1P, DSI_REXT	Float
HDMI	HDMI_CLKM, HDMI_CLKP, HDMI_D0M, HDMI_D0P, HDMI_D1M, HDMI_D1P, HDMI_D2M, HDMI_D2P, HDMI_DDCEC, HDMI_HPD, HDMI_REF	Float
	HDMI_VP, HDMI_VPH	Ground
LDB	LVDS0_CLK_N, LVDS0_CLK_P, LVDS0_TX0_N, LVDS0_TX0_P, LVDS0_TX1_N, LVDS0_TX1_P, LVDS0_TX2_N, LVDS0_TX2_P, LVDS0_TX3_N, LVDS0_TX3_P, LVDS1_CLK_N, LVDS1_CLK_P, LVDS1_TX0_N, LVDS1_TX0_P, LVDS1_TX1_N, LVDS1_TX1_P, LVDS1_TX2_N, LVDS1_TX2_P, LVDS1_TX3_N, LVDS1_TX3_P	Float
PCIe	PCIE_REXT, PCIE_RXM, PCIE_RXP, PCIE_TXM, PCIE_TXP	Float
	PCIE_VP, PCIE_VPH, PCIE_VPTX	Ground[1]
RGMII	RGMII_RD0, RGMII_RD1, RGMII_RD2, RGMII_RD3, RGMII_RX_CTL, RGMII_RXC, RGMII_TD0, RGMII_TD1, RGMII_TD2, RGMII_TD3, RGMII_TX_CTL, RGMII_TXC	Float
USB	USB_H1_DN, USB_H1_DP, USB_H1_VBUS, USB_OTG_CHD_B, USB_OTG_DN, USB_OTG_DP, USB_OTG_VBUS	Float

[1] In this case, the BSR chain will not work.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 11 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available.

On-chip 40 kHz ring oscillator—this clock source has the following characteristics:

- Approximately 25 µA more Idd than crystal oscillator
- Approximately ±50% tolerance
- No external component required
- Starts up quicker than 32 kHz crystal oscillator

External crystal oscillator with on-chip support circuit:

- At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- Higher accuracy than ring oscillator
- If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 12. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN	996 MHz ARM clock based on Power Virus operation	2200	mA
VDDSOC_IN	996 MHz ARM clock	1260	mA
VDDHIGH_IN		125[1]	mA
VDD_SNVS_IN		275[2]	µA
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)		25[3]	mA
Primary Interface (IO) Supplies			

Table 12. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_DRAM	—	—[4]	
NVCC_ENET	N=10	Use maximal IO equation[5]	
NVCC_LCD	N=29	Use maximal IO equation[5]	
NVCC_GPIO	N=24	Use maximal IO equation[5]	
NVCC_CSI	N=20	Use maximal IO equation[5]	
NVCC_EIM	N=53	Use maximal IO equation[5]	
NVCC_JTAG	N=6	Use maximal IO equation[5]	
NVCC_RGMII	N=12	Use maximal IO equation[5]	
NVCC_SD1	N=6	Use maximal IO equation[5]	
NVCC_SD2	N=6	Use maximal IO equation[5]	
NVCC_SD3	N=11	Use maximal IO equation[5]	
NVCC_NANDF	N=26	Use maximal IO equation[5]	
MISC			
DDR_VREF	—	1	mA

1 The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS2P5, NVCC_MIPI, or HDMI and PCIe VPH supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Solo/DualLite Power Consumption Measurement Application Note (AN4576) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximal power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.9 HDMI Power Consumption

Table 16 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data and power-down modes.

Table 16. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down		HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDDHIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDDARM_IN and VDDSOC_IN are connected to different external supply sources, then the following restrictions apply:

4.4.3 Ethernet PLL

Table 19. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 20. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 ARM PLL

Table 21. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~ 1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDDHIGH_IN such as the oscillator consumes

Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

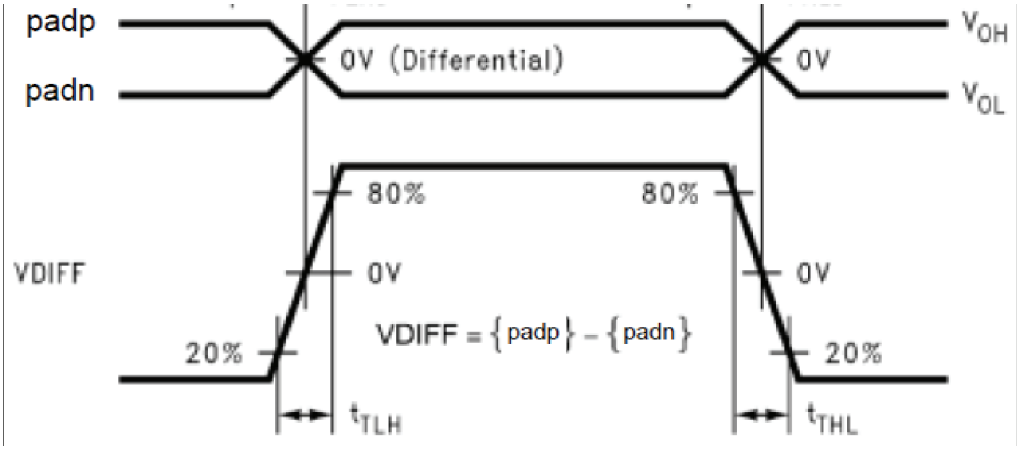
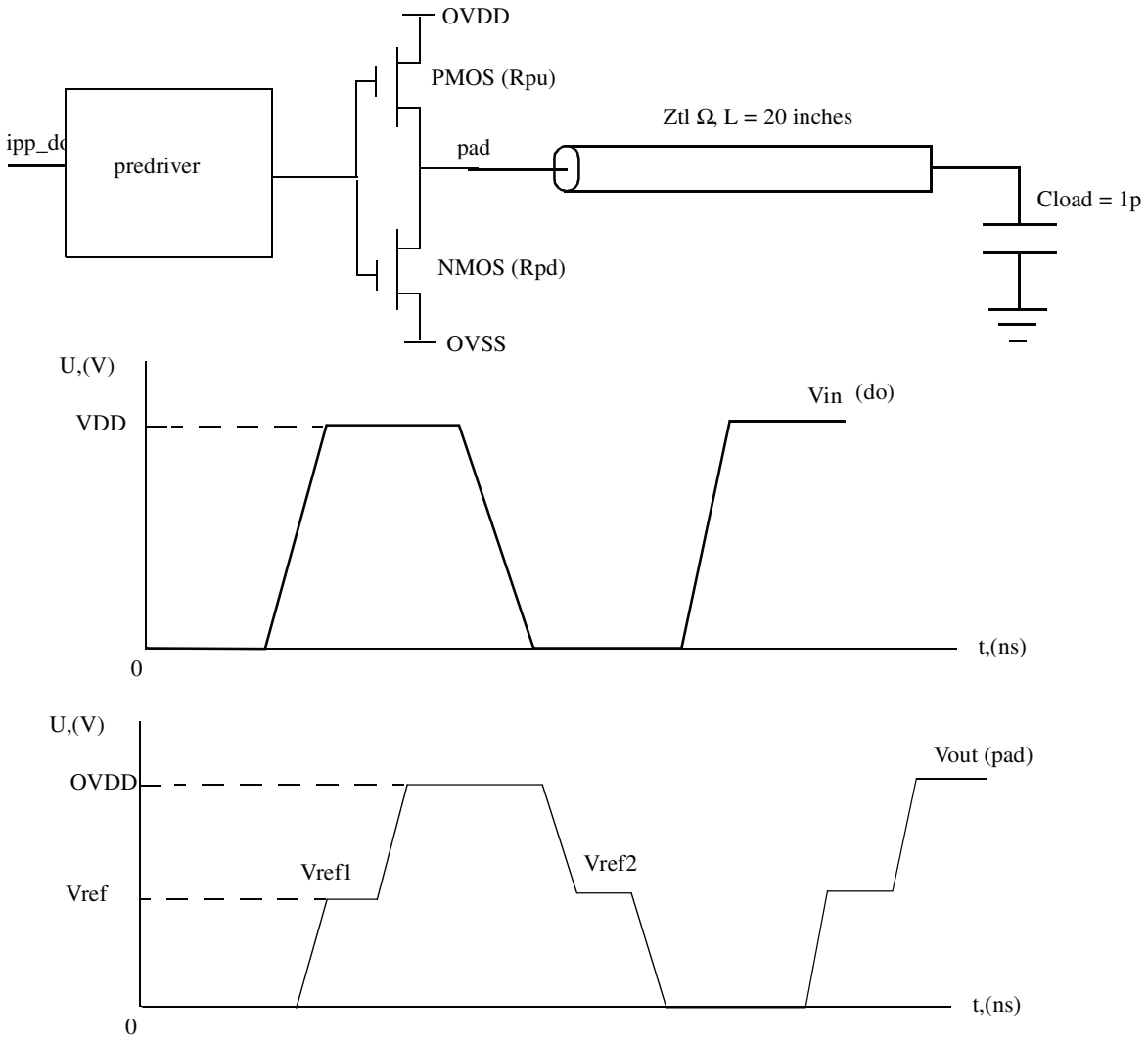


Figure 6. Differential LVDS Driver Transition Time Waveform

Table 31 shows the AC parameters for LVDS I/O.

Table 31. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 7. Impedance Matching Load for Measurement

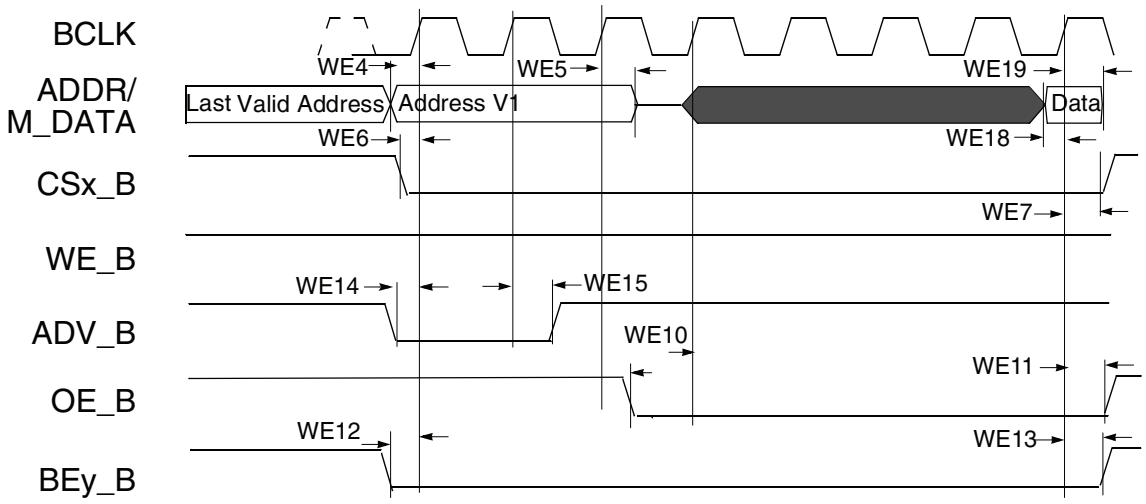


Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20, and Table 40 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

Table 47. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS x T		10		ns
NF6	ALE setup time	tALS	(AS+1) x T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1) x T	—	20	—	ns
NF8	Data setup time	tDS	DS x T	—	10	—	ns
NF9	Data hold time	tDH	DH x T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH) x T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH x T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1) x T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS x T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH) x T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH x T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' settings. In the above table, we use AS/DS/DH to represent each of these settings.

2) AS minimum value could be 0, while DS/DH minimum value is 1.

3) T represents for the GPMI clock period.

In EDO mode (Figure 31), NF16/NF17 are different from the definition in non-EDO mode (Figure 30). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample IO[7:0] at rising edge of delayed RE provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

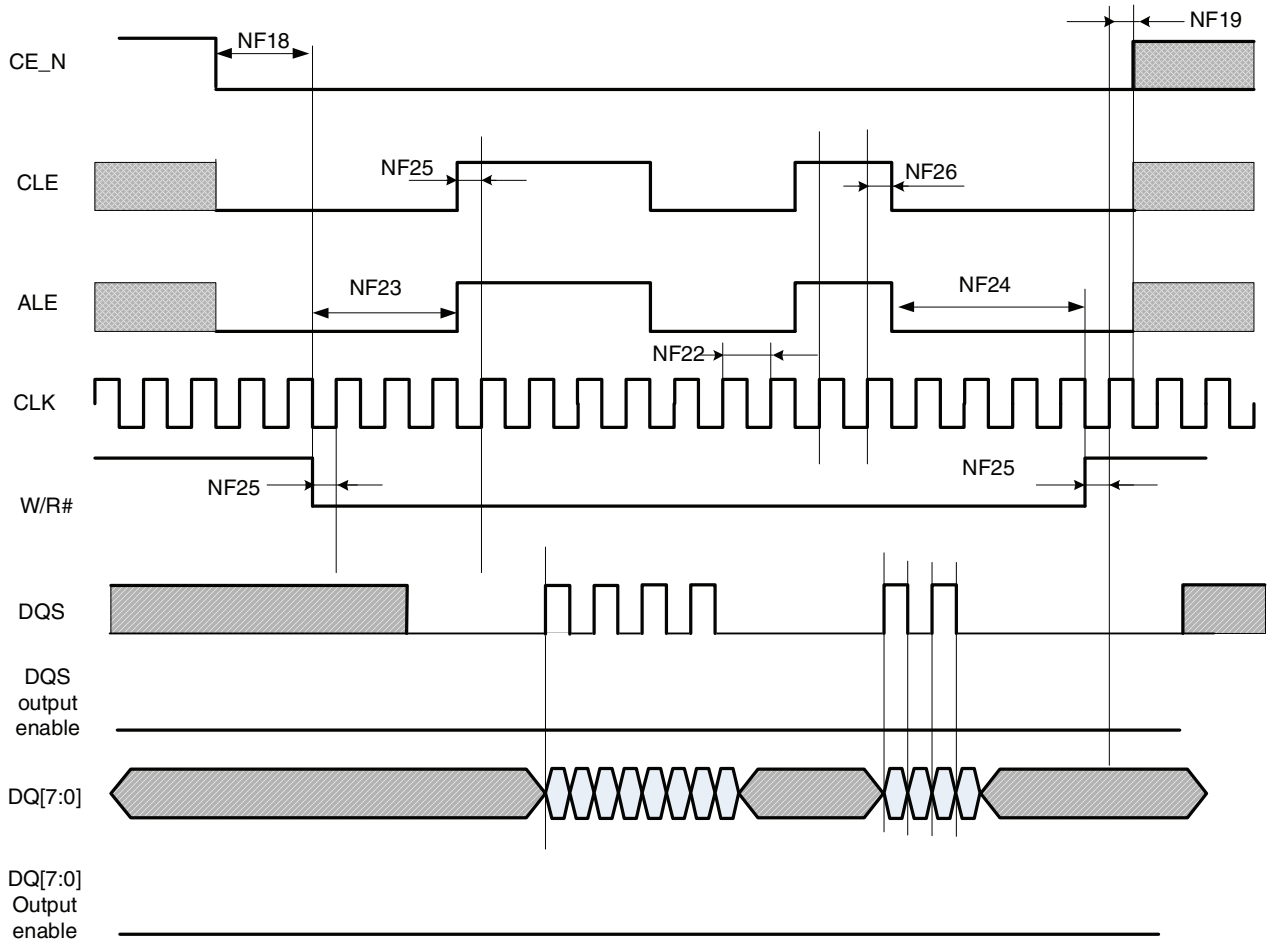


Figure 34. Source Synchronous Mode Data Read Timing Diagram

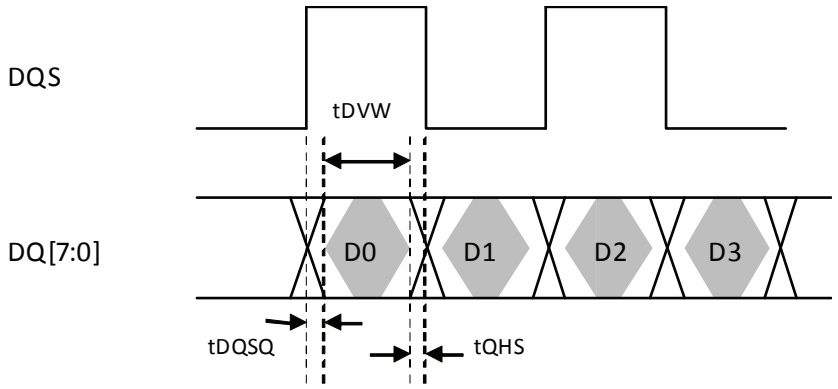


Figure 35. DQS/DQ Read Valid Window

Table 71. Electrical and Timing Information (continued)

V_{IDTL}	Differential input low voltage threshold		-70			mV
V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		920			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold		200		450	mV

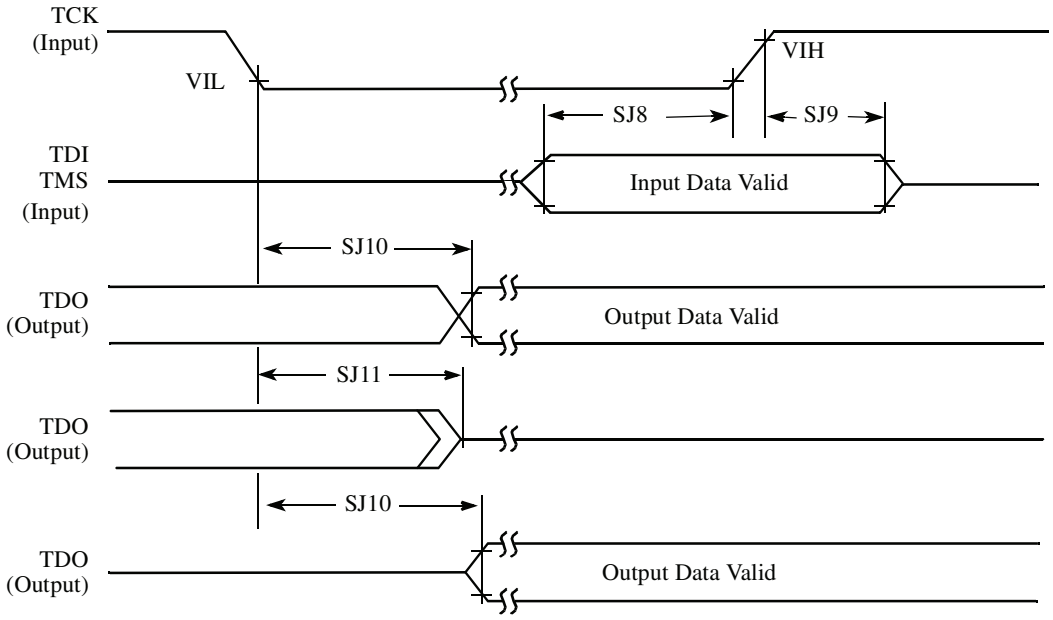


Figure 87. Test Access Port Timing Diagram

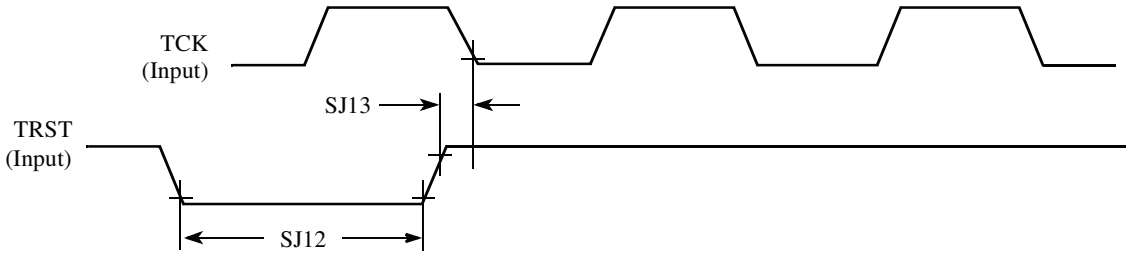


Figure 88. $\overline{\text{TRST}}$ Timing Diagram

Table 75. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns

Table 78. SSI Transmitter Timing with Internal Clock (continued)

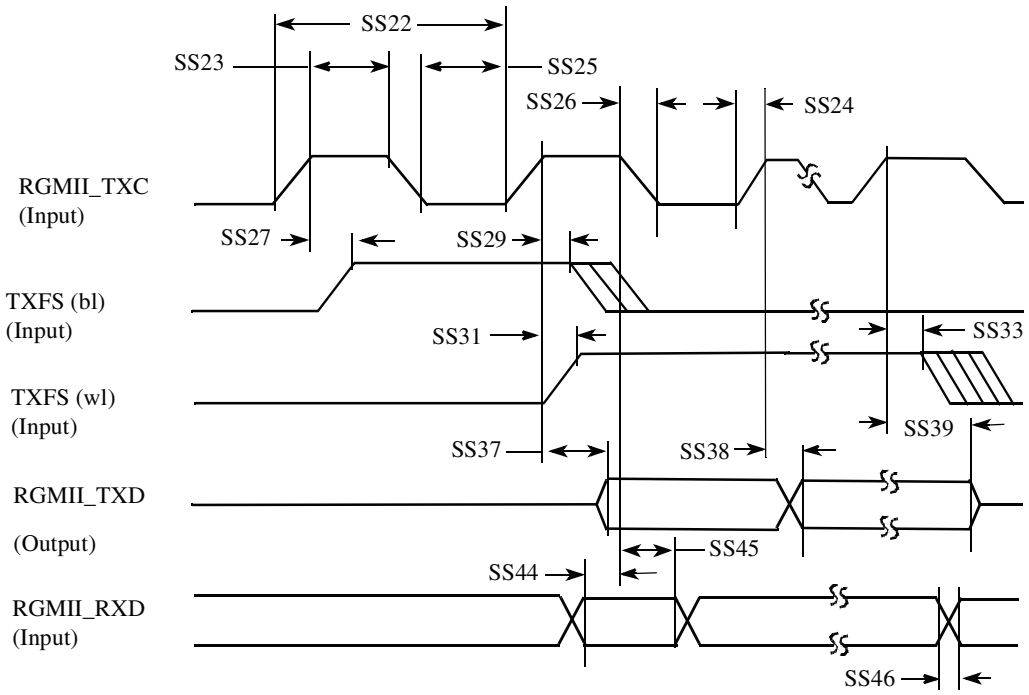
ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.18.3 SSI Transmitter Timing with External Clock

Figure 93 depicts the SSI transmitter external clock timing and Table 80 lists the timing parameters for the transmitter timing with the external clock.



Note: SRXD Input in Synchronous mode only

Figure 93. SSI Transmitter External Clock Timing Diagram

Table 80. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
	External Clock Operation			
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	-10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	-10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 91. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
PCIE_REXT	A2	
PCIE_VP	H7	
PCIE_VPH	G7	PCI PHY supply
PCIE_VPTX	G8	PCI PHY supply
VDD_SNVS_CAP	G9	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G11	Primary supply for the SNVS regulator
VDDARM_CAP	H11, H13, J11, J13, K11, K13, L11, L13, M11, M13, N11, N13, P11, P13, R11, R13	Secondary supply for core (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	H14, J14, K9, K14, L9, L14, M9, M14, N9, N14, P9, P14, R9, R14, T9, U9	Primary supply for the ARM core's regulator
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for VPU and GPUs (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for SoC and PU regulators (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V Domain (internal regulator output—requires capacitor if internal regulator is used)
USB_H1_VBUS	D10	Primary supply for the 3 V regulator
USB_OTG_VBUS	E9	Primary supply for the 3 V regulator
HDMI_DDCCEC	K2	Analog Ground(Ground reference for the Hot Plug Detect signal)
FA_ANA	A5	
GPANAIO	C8	
VDD_FA	B5	
ZQPAD	AE17	
NC	C14	
NC	G12	

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[4]	Input	100 kΩ pull-up
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[40]	Input	100 kΩ pull-up
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[41]	Input	100 kΩ pull-up
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[42]	Input	100 kΩ pull-up
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[43]	Input	100 kΩ pull-up
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[44]	Input	100 kΩ pull-up
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[45]	Input	100 kΩ pull-up
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[46]	Input	100 kΩ pull-up
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[47]	Input	100 kΩ pull-up
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[48]	Input	100 kΩ pull-up
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[49]	Input	100 kΩ pull-up
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[5]	Input	100 kΩ pull-up
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[50]	Input	100 kΩ pull-up
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[51]	Input	100 kΩ pull-up
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[52]	Input	100 kΩ pull-up
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[53]	Input	100 kΩ pull-up
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[54]	Input	100 kΩ pull-up
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[55]	Input	100 kΩ pull-up
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[56]	Input	100 kΩ pull-up
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[57]	Input	100 kΩ pull-up
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[58]	Input	100 kΩ pull-up
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[59]	Input	100 kΩ pull-up
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[6]	Input	100 kΩ pull-up
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[60]	Input	100 kΩ pull-up
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[61]	Input	100 kΩ pull-up
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[62]	Input	100 kΩ pull-up
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[63]	Input	100 kΩ pull-up
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[7]	Input	100 kΩ pull-up
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[8]	Input	100 kΩ pull-up
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[9]	Input	100 kΩ pull-up

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