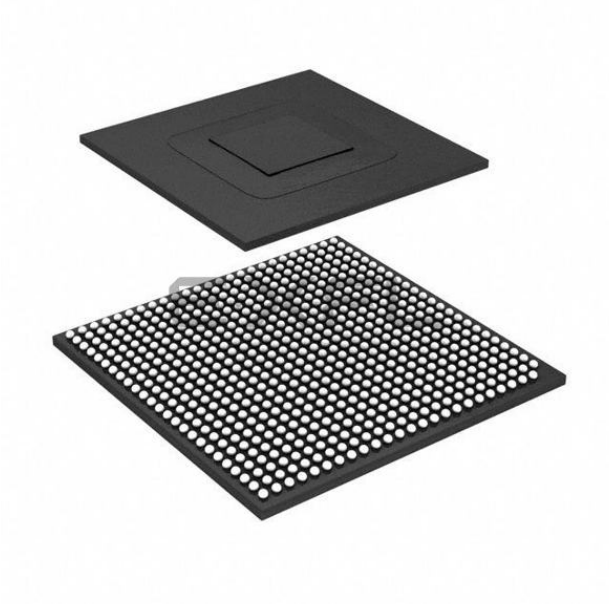

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u5dvm10ab

- — Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- — Two Controller Area Network (FlexCAN), 1 Mbps each
- — Two Watchdog timers (WDOG)
- — Audio MUX (AUDMUX)

The i.MX 6Solo/6DualLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Solo/6DualLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Solo/6DualLite processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H
- GPU3Dv5—3D Graphics Processing Unit (OpenGL ES 2.0) version 5
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 16 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

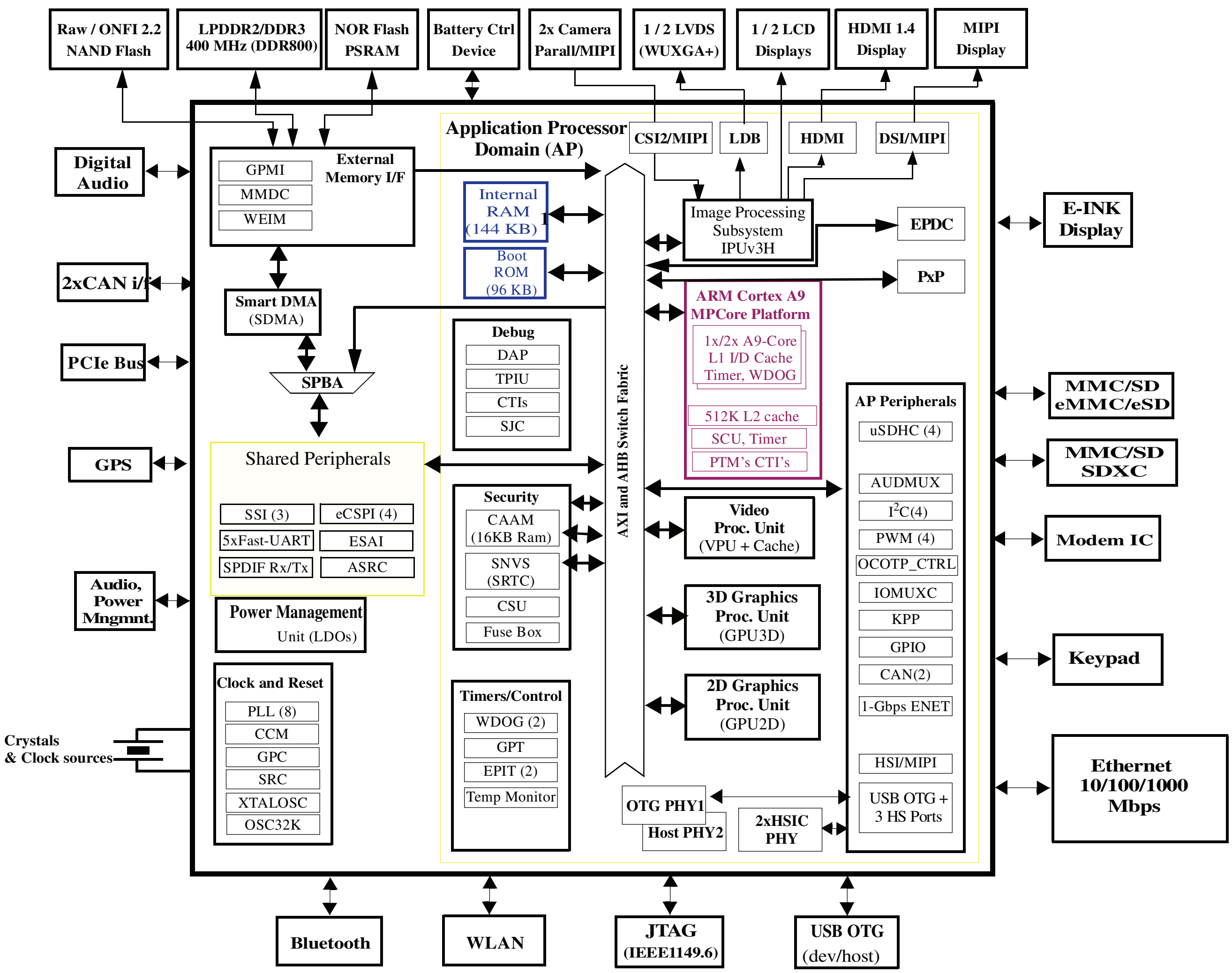
The actual feature set depends on the part numbers as described in Table 1, "Orderable Part Numbers," on page 3. Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Solo/6DualLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Solo/6DualLite processor system.



[1] 144 KB RAM including 16 KB RAM inside the CAAM.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details. **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes. It is available in both i.MX 6DualLite and i.MX 6Solo.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	-40	150	^oC

[1] OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 8 displays the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	38 23	$^oC/W$ $^oC/W$
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	30 20	$^oC/W$ $^oC/W$
Junction to Board[1,4]		$R_{\theta JB}$	14	$^oC/W$
Junction to Case[1,5]		$R_{\theta JC}$	6	$^oC/W$
Junction to Package Top[1,6]	Natural Convection	Ψ_{JT}	2	$^oC/W$

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2] Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

[3] Per JEDEC JESD51-6 with the board horizontal.

[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Table 9 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDDARM_IN	1.350[2]	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.225 V minimum for operation up to 996 MHz.
		1.275[2]	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.150 V minimum for operation up to 792 MHz.
		1.175[2]	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.05 V minimum for operation up to 396 MHz.
	VDDSOC_IN[3]	1.275[2,4]	—	1.5	V	VPU </= 328 MHz, VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) = 1.225 V maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDDARM_IN	1.250	—	1.3	V	LDO bypassed for operation up to 996 MHz
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.05	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDDSOC_IN	1.15[4]	—	1.225	V	LDO bypassed for operation VPU </= 328 MHz
Standby/DSM mode	VDDARM_IN	0.9	—	1.3	V	Refer to Table 13, "Stop Mode Current and Power Consumption," on page 29.
	VDDSOC_IN	0.9	—	1.225	V	
VDDHIGH internal regulator	VDDHIGH_IN	2.8	—	3.3	V	Must match the range of voltges that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.9	—	3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	
	USB_H1_VBUS	4.4	—	5.25	V	
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2, DDR3-U
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3_L
Supply for RGMII I/O power group[6]	NVCC_RGMII	1.15	—	2.625	V	1.15 V – 1.30 V in HSIC 1.2 V mode 1.43 V – 1.58 V in RMGII 1.5 V mode 1.70 V – 1.90 V in RMGII 1.8 V mode 2.25 V – 2.625 V in RMGII 2.5 V mode

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors in typical condition. Table 14 shows the USB interface current consumption in power down mode..

Table 14. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 PCIe 2.0 Power Consumption

Table 15 provides PCIe PHY currents under certain Tx operating modes.

Table 15. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
PO: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
POs: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Reocvery Time Latency, Lower Power State		PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down		PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 29 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 29. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω ± 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω ± 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 30 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V

Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.
2 Vid(ac) specifies the input differential voltage I Vtr-Vcp I required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).
3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

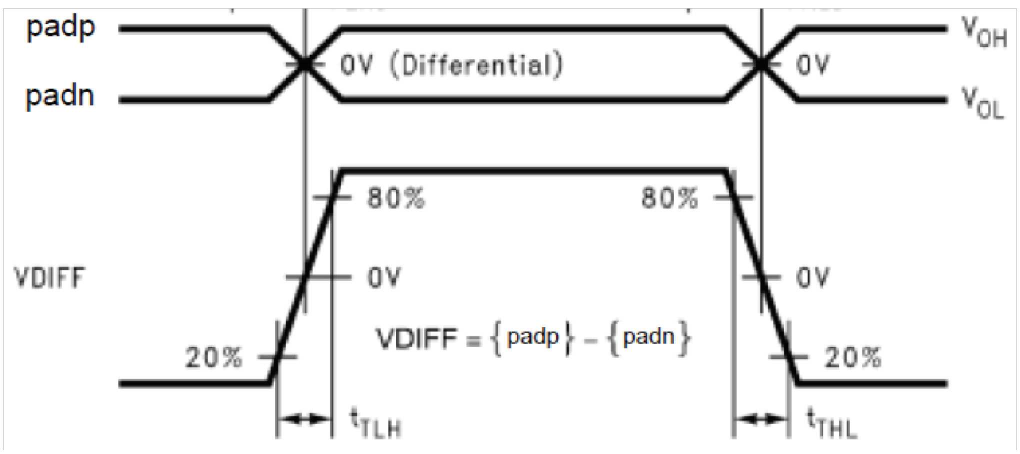


Figure 6. Differential LVDS Driver Transition Time Waveform

Table 31 shows the AC parameters for LVDS I/O.

Table 31. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+AD H+1-RCSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCS O	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

Table 49. Samsung Toggle Mode Timing Parameters (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF23	preamble delay	tPRE	(PRE_DELAY+1) x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns

For DDR Toggle mode, Figure 35 shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 1.4 ns(max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.11.2.1 ECSPI Master Mode Timing

Figure 38 depicts the timing of ECSPI in master mode. Table 50 lists the ECSPI master mode timing characteristics.

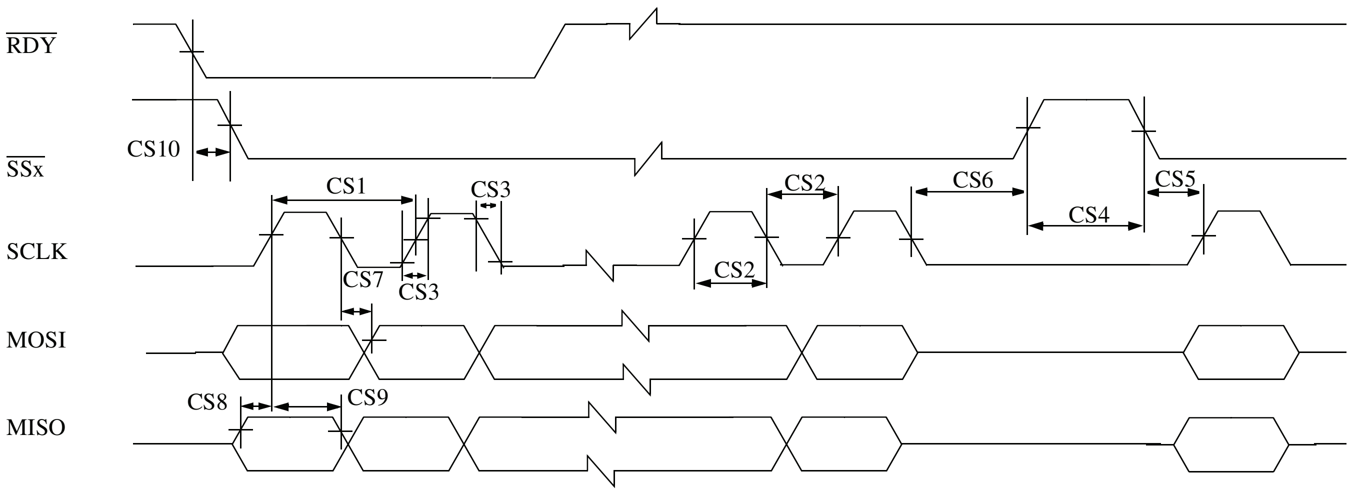


Figure 38. ECSPI Master Mode Timing Diagram

Table 50. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	Half SCLK period - 4	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	Half SCLK period - 2	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	MISO Setup Time	t_{Smiso}	18	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

[1] See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

[2] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

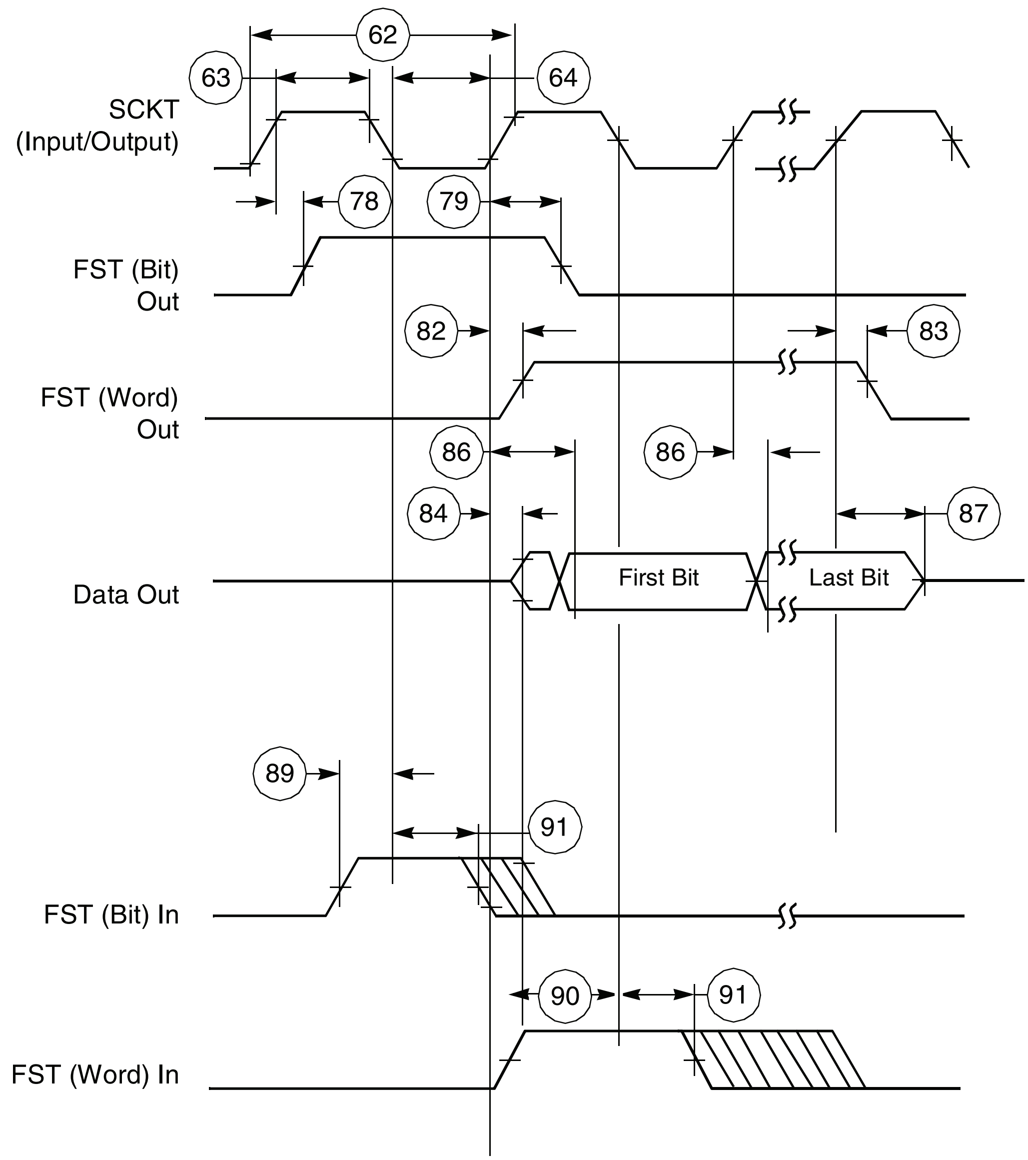


Figure 40. ESAI Transmitter Timing

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 48 shows MII asynchronous input timings. Table 59 describes the timing parameters (M10–M15) shown in the figure.

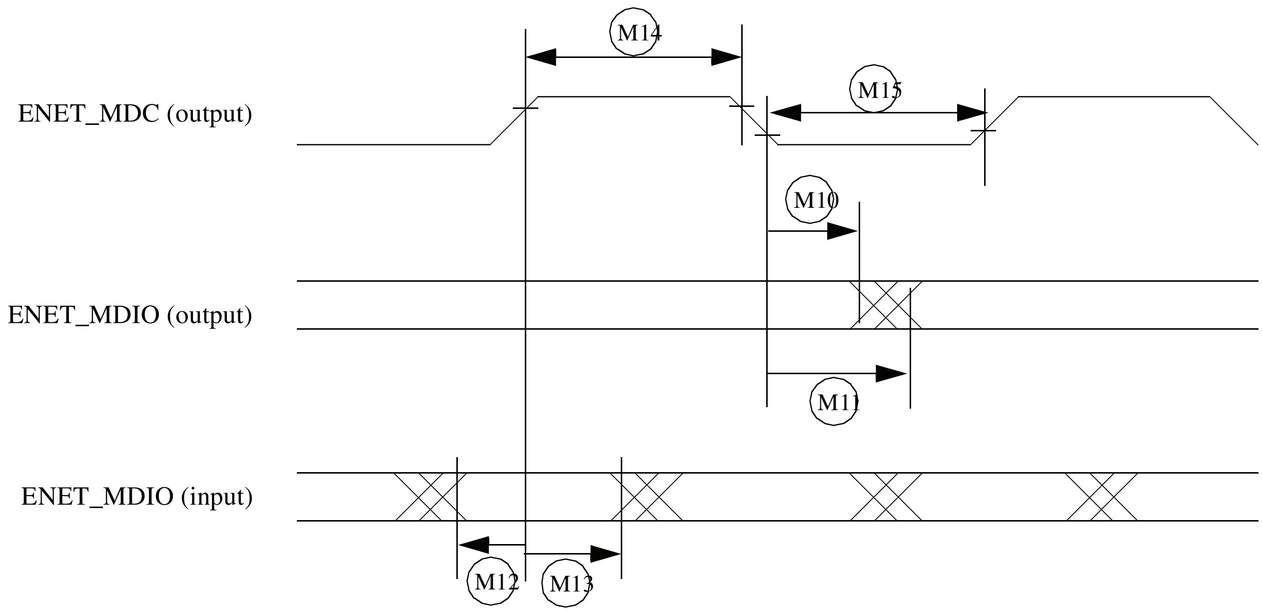


Figure 48. MII Serial Management Channel Timing Diagram

Table 59. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 65 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 65. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 2 cycles	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

1 CSIx stands for CSI1 or CSI2
2 The MSB bits are duplicated on LSB bits implementing color extension
3 The two MSB bits are duplicated on LSB bits implementing color extension
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB 16 bits— Supported in two ways: (1) As a “generic data” input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr 16 bits— Supported as a “generic-data” input, with no on-the-fly processing.
7 YCbCr 16 bits— Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 66 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

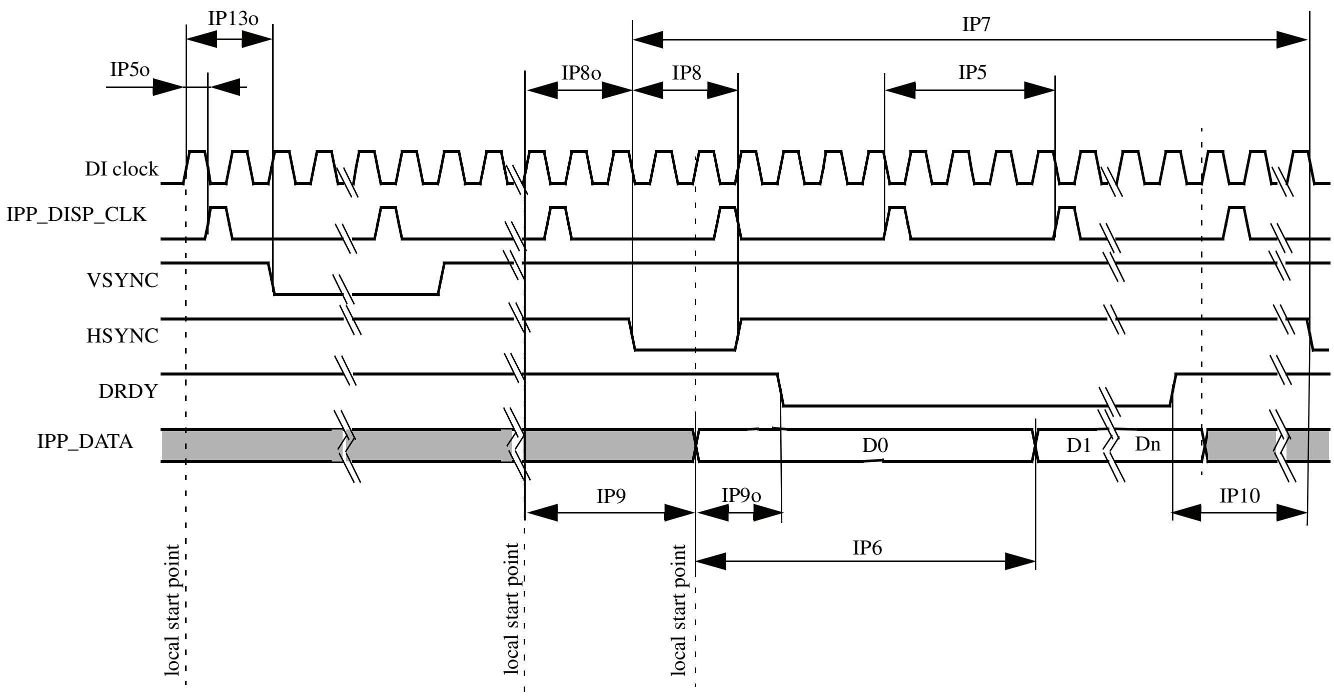


Figure 66. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 67 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

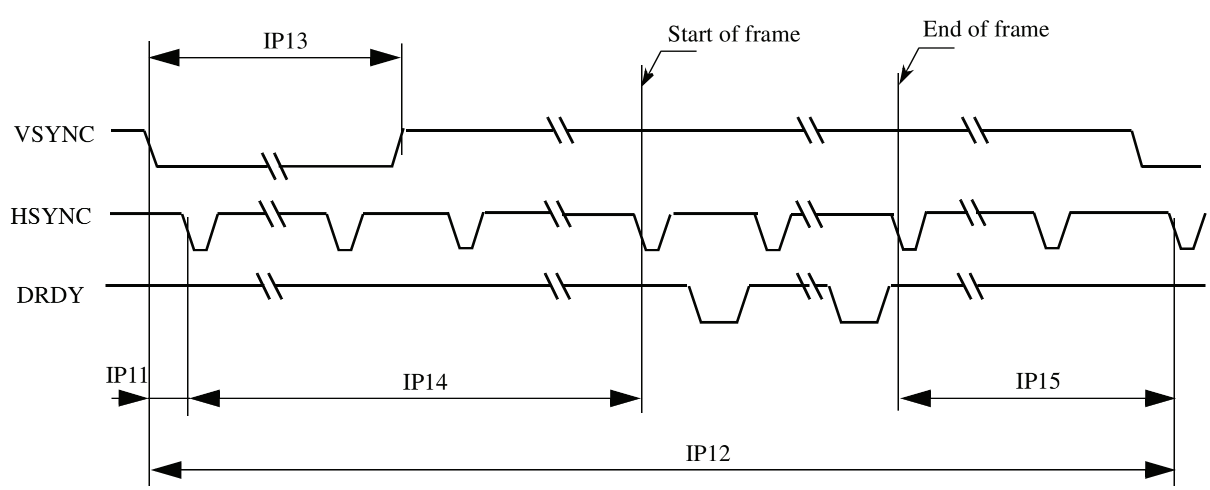


Figure 67. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 75. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.11.17 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 76 and Figure 89 and Figure 90 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 76. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, LOW PROFILE, FINE PITCH, 624 I/O, 21 X 21 PKG, 0.8 MM PITCH (MAP)		DOCUMENT NO: 98ASA00404D	REV: 0
		CASE NUMBER: 2240–01	27 SEP 2011
		STANDARD: NON–JEDEC	

Figure 101. 21 x 21 mm BGA, Case 2240 Package Top, Bottom, and Side Views

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DRAM_SDQS4_B	AE18	NVCC_DRAM			DRAM_SDQS4_B	-	-
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[5]	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM			DRAM_SDQS5_B	-	-
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[6]	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM			DRAM_SDQS6_B	-	-
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[7]	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM			DRAM_SDQS7_B	-	-
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDWE	Output	Low
DSI_CLK0M	H3	NVCC_MIPI	ANALOG				
DSI_CLK0P	H4	NVCC_MIPI	ANALOG				
DSI_D0M	G2	NVCC_MIPI	ANALOG				
DSI_D0P	G1	NVCC_MIPI	ANALOG				
DSI_D1M	H2	NVCC_MIPI	ANALOG				
DSI_D1P	H1	NVCC_MIPI	ANALOG				
EIM_A16	H25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[16]	Output	Low
EIM_A17	G24	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[17]	Output	Low
EIM_A18	J22	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[18]	Output	Low
EIM_A19	G25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[19]	Output	Low
EIM_A20	H22	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[20]	Output	Low
EIM_A21	H23	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[21]	Output	Low
EIM_A22	F24	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[22]	Output	Low
EIM_A23	J21	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[23]	Output	Low
EIM_A24	F25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[24]	Output	Low
EIM_A25	H19	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[25]	Output	Low
EIM_BCLK	N22	NVCC_EIM	GPIO	ALT0	weim.WEIM_BCLK	Output	Low
EIM_CS0	H24	NVCC_EIM	GPIO	ALT0	weim.WEIM_CS[0]	Output	High
EIM_CS1	J23	NVCC_EIM	GPIO	ALT0	weim.WEIM_CS[1]	Output	High
EIM_D16	C25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[16]	Input	100 kΩ pull-up
EIM_D17	F21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[17]	Input	100 kΩ pull-up
EIM_D18	D24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[18]	Input	100 kΩ pull-up

Table 93. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AD	AE
1	DRAM_D5	GND
2	DRAM_D0	DRAM_D1
3	DRAM_SDQS0_B	DRAM_SDQS0
4	GND	DRAM_D7
5	DRAM_D8	DRAM_D9
6	DRAM_SDQS1	DRAM_SDQS1_B
7	GND	DRAM_D11
8	DRAM_SDQS2	DRAM_SDQS2_B
9	DRAM_D29	DRAM_D24
10	GND	DRAM_DQM3
11	DRAM_D30	DRAM_D26
12	DRAM_A12	DRAM_A9
13	GND	DRAM_A5
14	DRAM_SDCLK_1	DRAM_SDCLK_1_B
15	DRAM_SDCLK_0	DRAM_SDCLK_0_B
16	GND	DRAM_CAS
17	DRAM_CS1	ZQPAD
18	NC	NC
19	GND	NC
20	NC	NC
21	NC	NC
22	GND	NC
23	NC	NC
24	NC	NC
25	NC	GND
	AD	AE

Table 94 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 94. 21 x 21 mm, 0.8 mm Pitch Ball Map

	A	B	C	D
1	NC	PCIE_RXM	GND	CSI_D1M
2	PCIE_REXT	PCIE_RXP	JTAG_TRSTB	CSI_D1P
3	PCIE_TXM	PCIE_TXP	JTAG_TMS	GND
4	GND	GND	GND	CSI_REXT
5	FA_ANA	VDD_FA	CLK2_N	CLK2_P
6	USB_OTG_DP	USB_OTG_DN	GND	GND
7	XTALI	XTALO	CLK1_N	CLK1_P
8	GND	USB_OTG_CHD_B	GPANAIO	GND
9	NC	NC	RTC_XTALO	RTC_XTALI
10	NC	NC	GND	USB_H1_VBUS
11	NC	NC	POR_B	PMIC_ON_REQ
12	NC	NC	BOOT_MODE0	ONOFF
13	GND	SD3_CMD	SD3_DAT5	SD3_DAT4
14	NC	NC	NC	SD3_CLK
15	SD3_DAT2	SD3_DAT3	NANDF_CLE	SD3_RST
16	NANDF_ALE	NANDF_RB0	NANDF_CS1	NANDF_CS3
17	NANDF_CS2	SD4_CMD	NANDF_D1	NANDF_D3
18	NANDF_D0	NANDF_D5	NANDF_D7	SD4_DAT0
19	NANDF_D4	SD4_DAT1	SD4_DAT5	SD4_DAT7
20	SD4_DAT3	SD4_DAT6	SD1_DAT1	SD1_CLK
21	SD1_DAT0	SD1_CMD	SD2_CLK	RGMII_TXC
22	SD2_DAT0	SD2_DAT3	RGMII_TD0	RGMII_RX_CTL
23	SD2_DAT2	RGMII_RD1	RGMII_TX_CTL	RGMII_RD3
24	RGMII_TD3	RGMII_RD2	RGMII_RD0	EIM_D18
25	GND	RGMII_RXC	EIM_D16	EIM_D23
	A	B	C	D

Table 94. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

M	L	K	J	H	G	F	E
CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	DSI_D0P	NC	NC
CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	DSI_D0M	NC	NC
CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P
CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M
CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	JTAG_TDI	GND	GND
CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	JTAG_TDO	GND	GND
HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	PCIE_VPH	GND	GND
GND	GND	GND	GND	GND	PCIE_VPTX	GND	NVCC_PLL_OUT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	VDD_SNVS_CAP	VDDUSB_CAP	USB_OTG_VBUS
GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDD_SNVS_IN	PMIC_STBY_REQ	TAMPER
GND	GND	GND	GND	GND	NC	BOOT_MODE1	TEST_MODE
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	NC	SD3_DAT7	SD3_DAT6
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0
GND	GND	GND	GND	GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK
VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6
GND	GND	GND	GND	GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4
NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	GND	SD2_CMD	SD1_DAT2
EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1
EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	EIM_D19	EIM_D17	RGMII_TD2
EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	EIM_D25	EIM_D24	EIM_EB2
EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	EIM_D28	EIM_EB3	EIM_D22
EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	EIM_A17	EIM_A22	EIM_D26
EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	EIM_A19	EIM_A24	EIM_D27
M	L	K	J	H	G	F	E