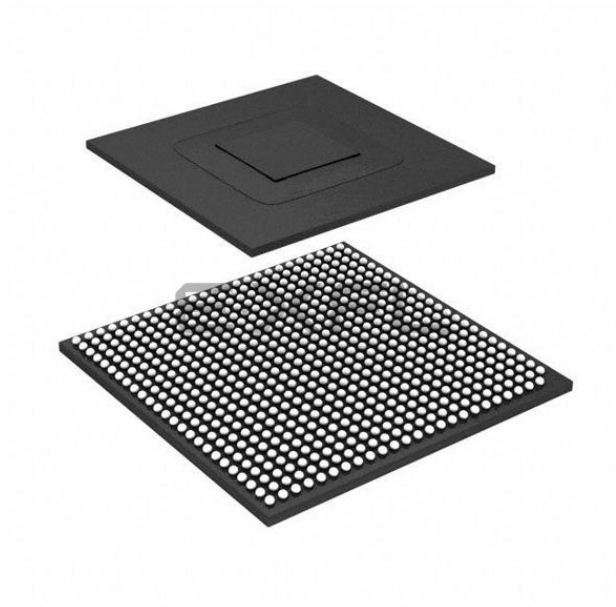

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

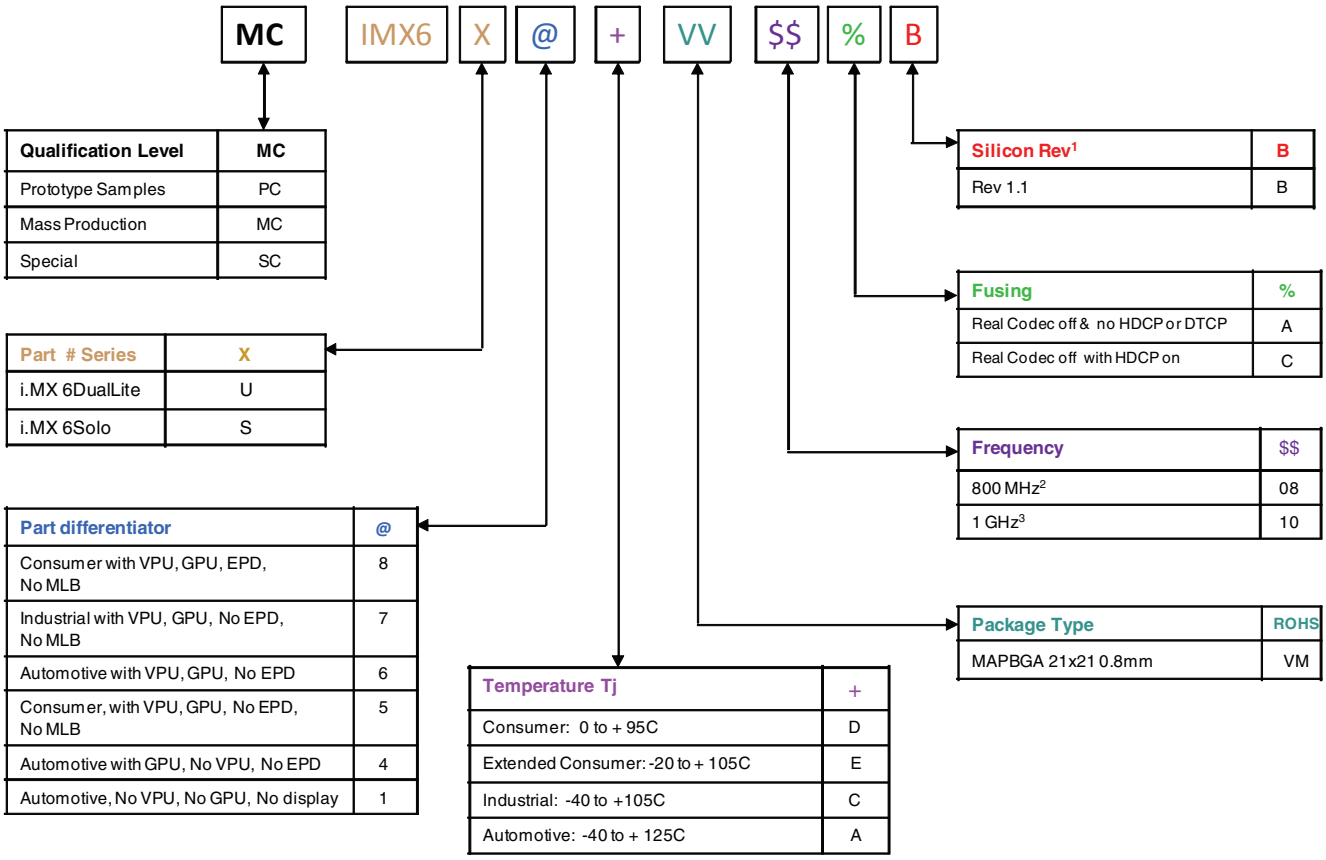
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u5evm10abr

- Color eReaders
- IPTV
- Human Machine Interfaces (HMI)
- Portable medical
- IP phones
- Home energy management systems

The i.MX 6Solo/6DualLite processors have some very exciting features, for example:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4.
- Smart speed technology—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, an image processing unit (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with a shader and a 2D graphics accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to two displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, and PCIe-II).
- Eink Panel Display Controller—The processors integrate EPD controller that supports E-INK color and monochrome with up to 1650x2332 resolution and 5-bit grayscale (32-levels per color channel).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure



1. See the freescale.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
3. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6DualLite and 6Solo

1.2 Features

The i.MX 6Solo/6DualLite processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- The i.MX 6Solo supports single ARM Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual ARM Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer

NOTE

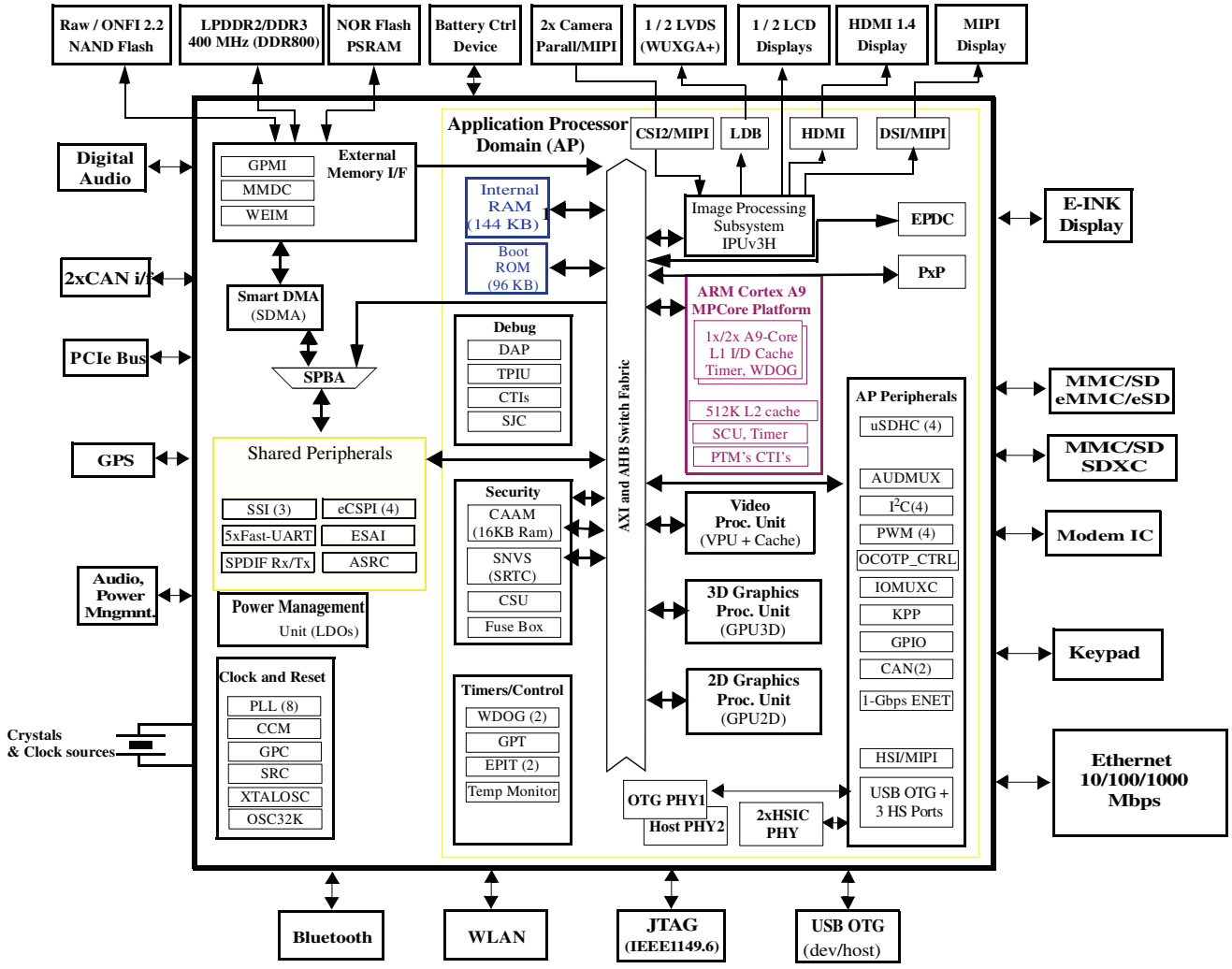
The actual feature set depends on the part numbers as described in Table 1, "Orderable Part Numbers," on page 3. Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Solo/6DualLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Solo/6DualLite processor system.



1 144 KB RAM including 16 KB RAM inside the CAAM.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Solo/6DualLite processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6Solo/6DualLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 22
BGA Case 2240 Package Thermal Resistance	on page 23
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximal Supply Currents	on page 27
Low Power Mode Supply Currents	on page 29
USB PHY Current Consumption	on page 30
PCIe 2.0 Power Consumption	on page 30

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDDARM_IN VDDSOC_IN	-0.3	1.5	V
Internal supply voltages	VDDARM_CAP VDDSOC_CAP VDDPU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
LVDS I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	-0.3	3.3	V
VDDHIGH_IN supply voltage	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD[1]+0.3	V

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 11 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available.

On-chip 40 kHz ring oscillator—this clock source has the following characteristics:

- Approximately 25 µA more Idd than crystal oscillator
- Approximately ±50% tolerance
- No external component required
- Starts up quicker than 32 kHz crystal oscillator

External crystal oscillator with on-chip support circuit:

- At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- Higher accuracy than ring oscillator
- If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 12. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN	996 MHz ARM clock based on Power Virus operation	2200	mA
VDDSOC_IN	996 MHz ARM clock	1260	mA
VDDHIGH_IN		125[1]	mA
VDD_SNVS_IN		275[2]	µA
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)		25[3]	mA
Primary Interface (IO) Supplies			

their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logics.

These regulators have three basic modes:

- Bypass. The regulation FET is switched fully on passing the external voltage, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since the accuracy or the % regulation is not tested, and only tested with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value for component selection), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDDHIGH_IN (see Table 9 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. Since the accuracy or the % regulation is not tested, and only tested with the LDO set to either 2.25V or 2.75V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value for component selection), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 29 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 29. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω ± 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω ± 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 30 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 30. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 39 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

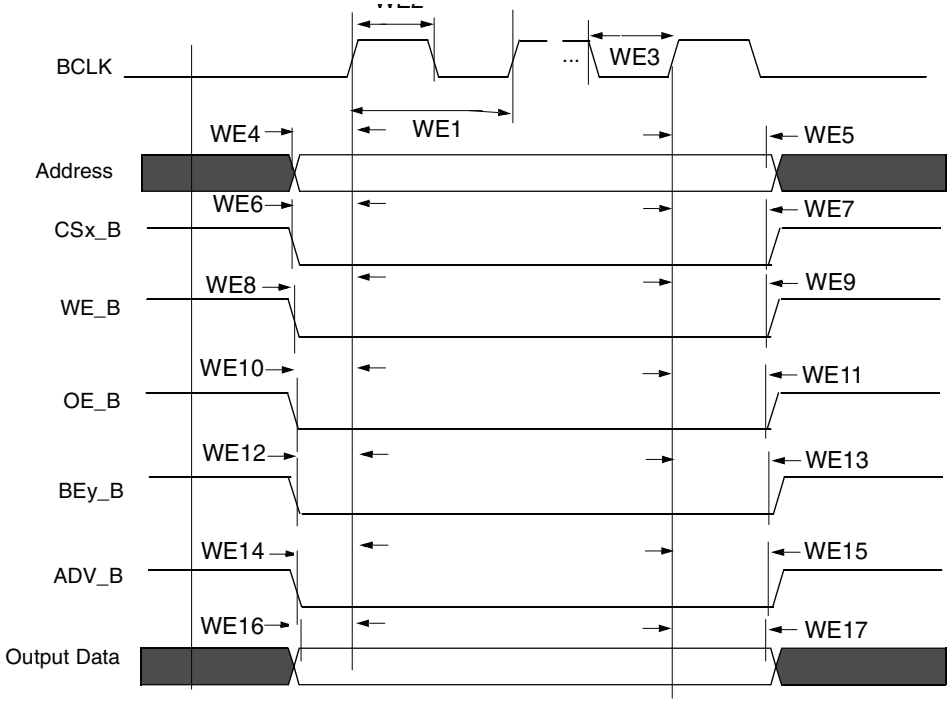


Figure 10. EIM Outputs Timing Diagram

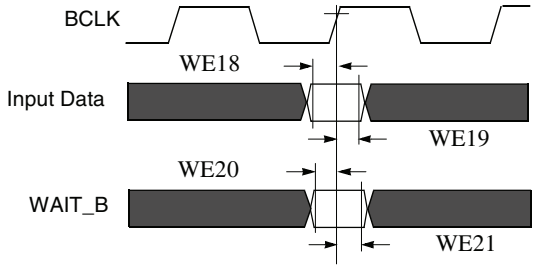


Figure 11. EIM Inputs Timing Diagram

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 32 to Figure 34 show the write and read timing of Source Synchronous Mode.

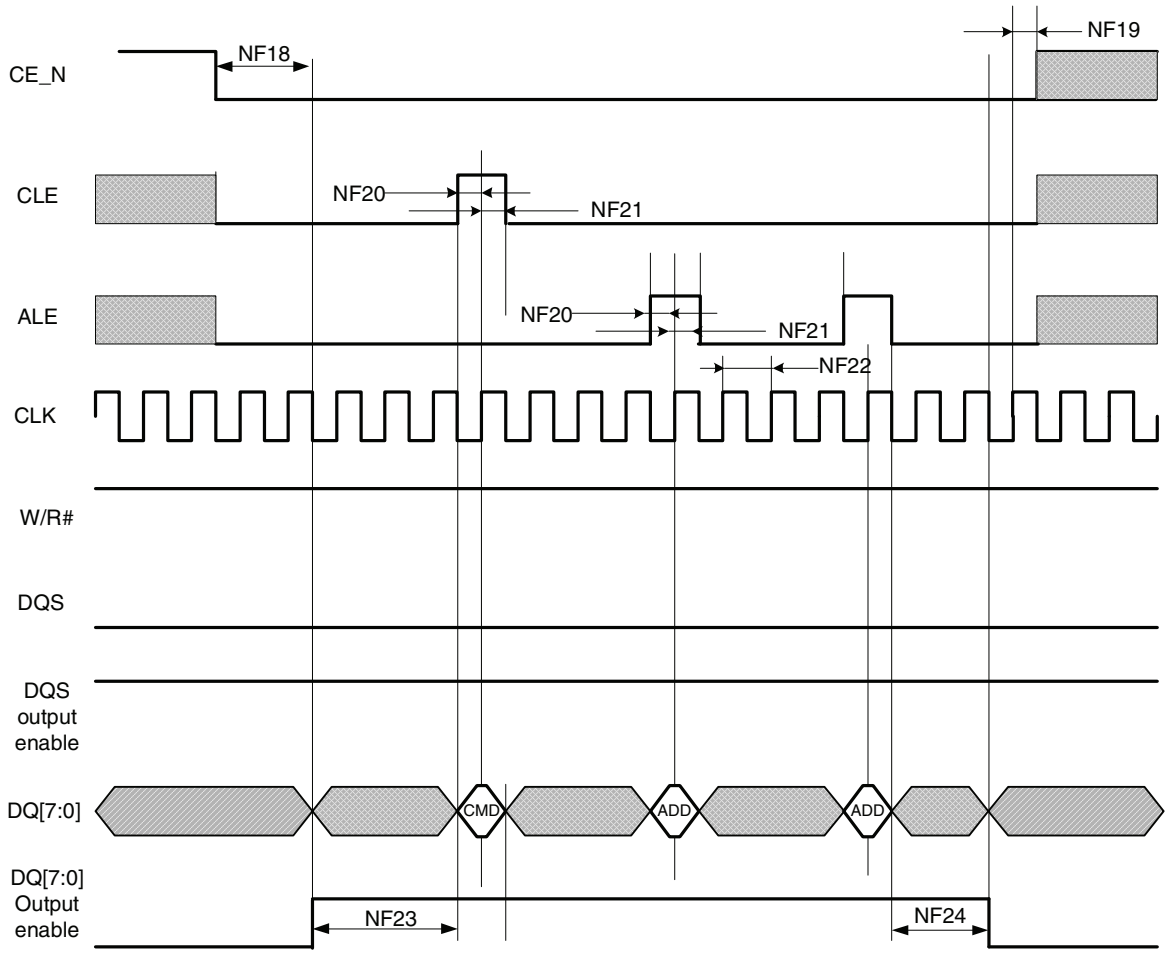


Figure 32. Source Synchronous Mode Command and Address Timing Diagram

Table 52. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	SCKT rising edge to FST out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

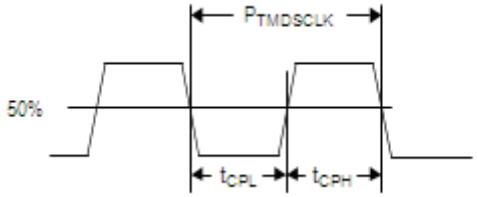


Figure 56. TMDS Clock Signal Definitions

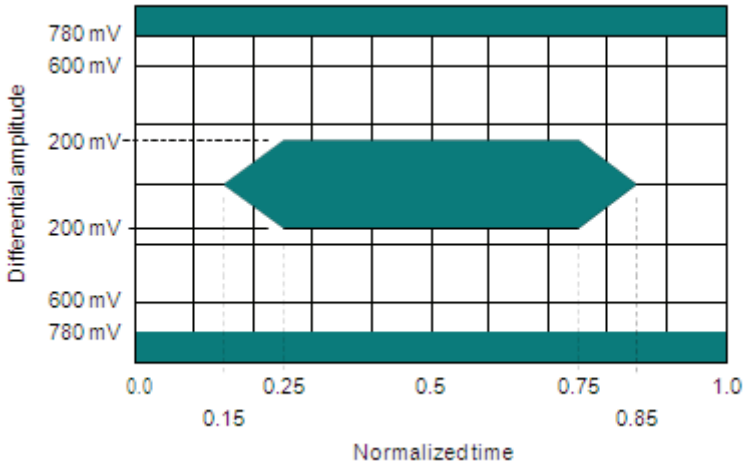


Figure 57. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

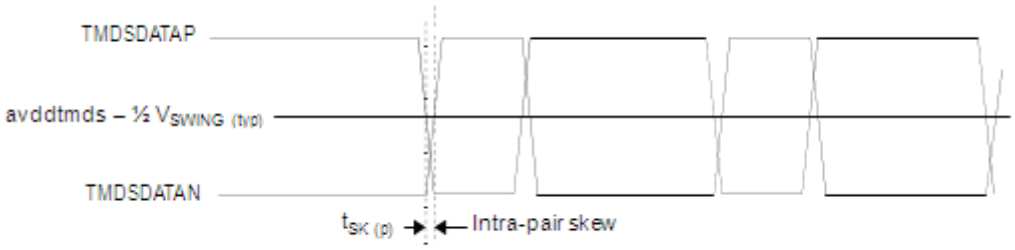


Figure 58. Intra-Pair Skew Definition

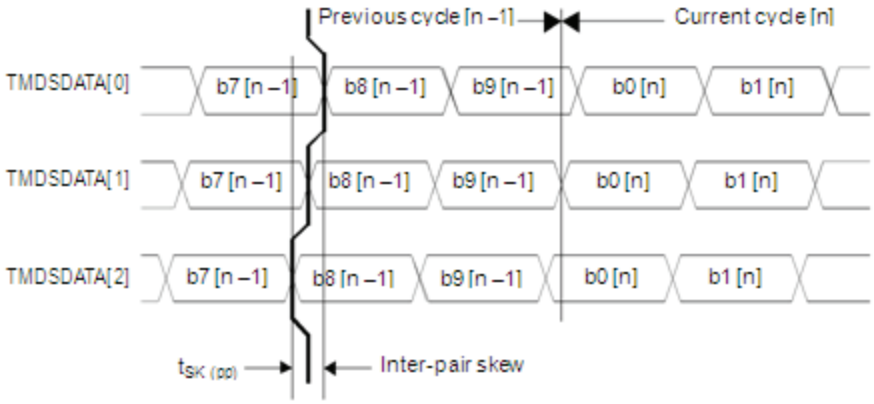


Figure 59. Inter-Pair Skew Definition

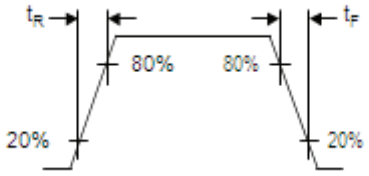


Figure 60. TMDS Output Signals Rise and Fall Time Definition

Table 63. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 56.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 56.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 56.	4	5	6	UI[1]
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 56.	4	5	6	UI[1]
—	TMDSCLK jitter[2]	RL = 50 Ω	—	—	0.25	UI[1]
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 58.	—	—	0.15	UI[1]

Table 64. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 65 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 65. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 2 cycles	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

1 CSIx stands for CSI1 or CSI2

2 The MSB bits are duplicated on LSB bits implementing color extension

3 The two MSB bits are duplicated on LSB bits implementing color extension

4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).

5 RGB 16 bits— Supported in two ways: (1) As a “generic data” input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

6 YCbCr 16 bits— Supported as a “generic-data” input, with no on-the-fly processing.

7 YCbCr 16 bits— Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

8 YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.13.4 Synchronized Data Flow Transmission with Wake

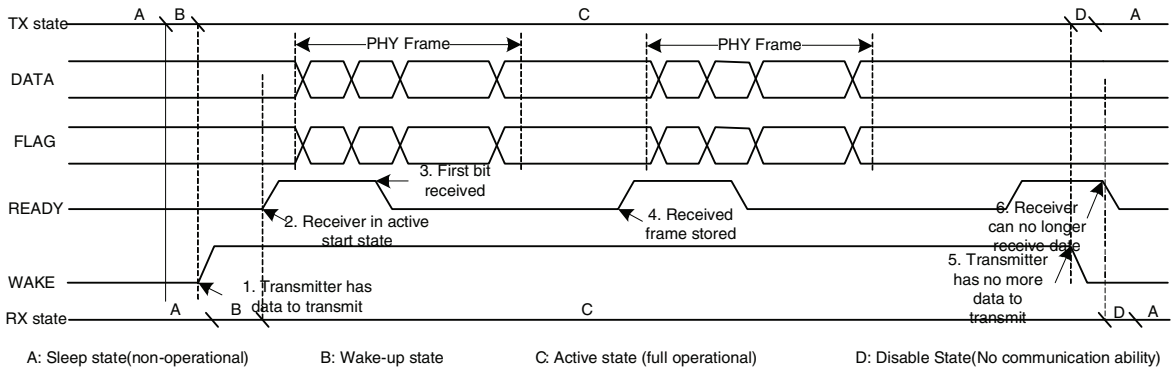


Figure 79. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

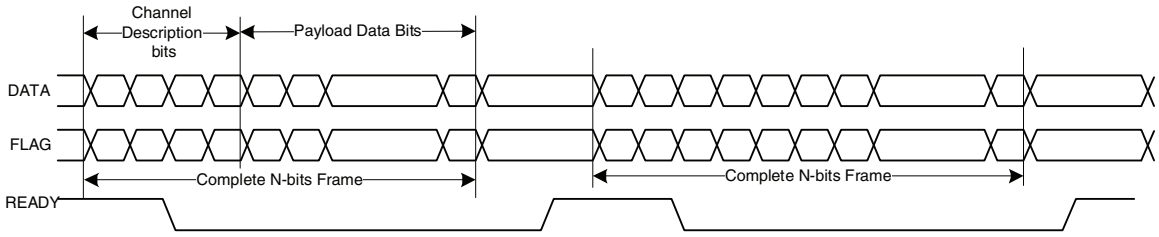


Figure 80. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

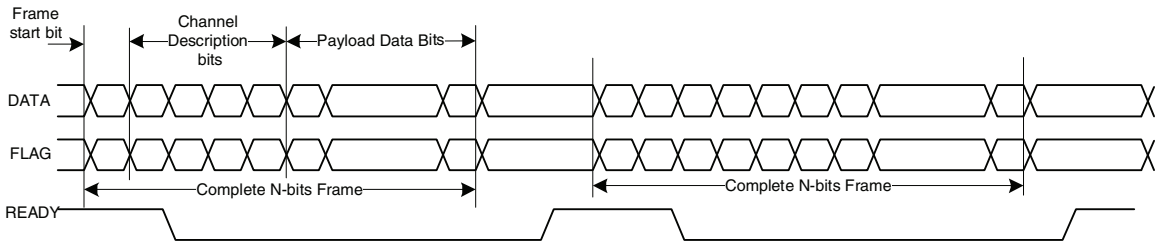


Figure 81. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

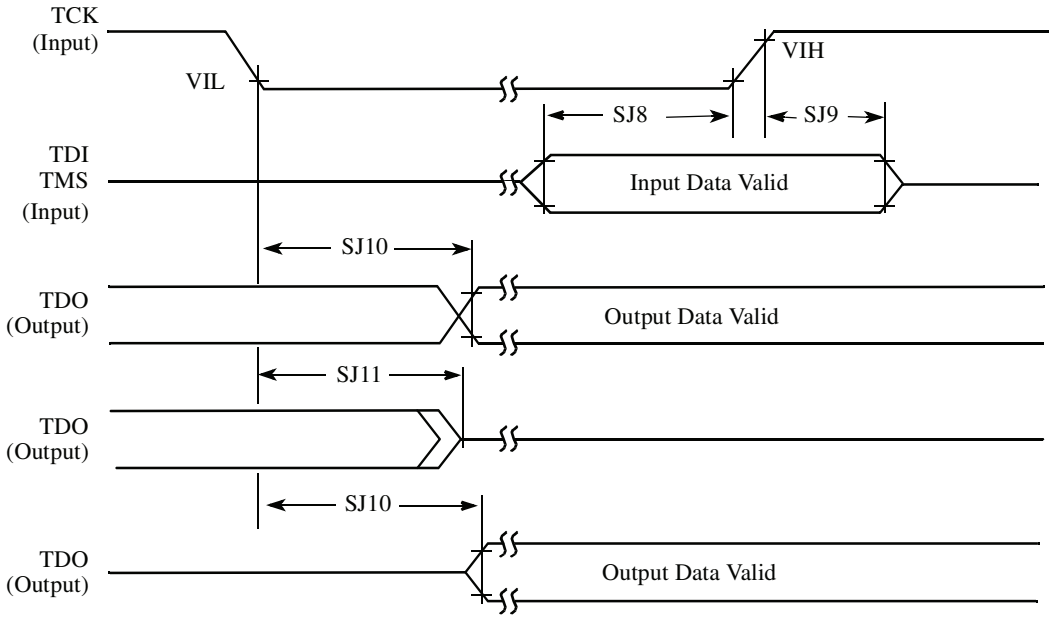


Figure 87. Test Access Port Timing Diagram

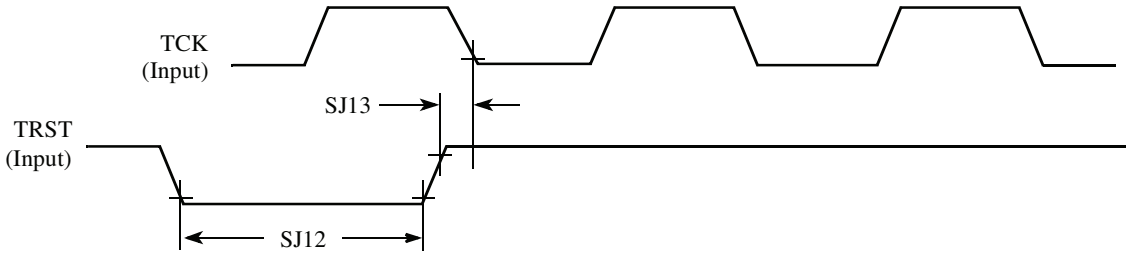


Figure 88. $\overline{\text{TRST}}$ Timing Diagram

Table 75. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns

Table 75. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.11.17 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 76 and Figure 89 and Figure 90 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 76. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

6.1.2 21 x 21 mm Supplies Contact Assignments and Functional Contact Assignments

Table 91 shows supplies contact assignments for the 21 x 21 mm package.

Table 91. 21 x 21 mm Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of the DDR interface
NVCC_EIM	K19, L19, M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the raw NAND Flash memories interface
NVCC_PLL_OUT	E8	
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[24]	Input	100 kΩ pull-up
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[25]	Input	100 kΩ pull-up
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[26]	Input	100 kΩ pull-up
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[27]	Input	100 kΩ pull-up
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[28]	Input	100 kΩ pull-up
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[29]	Input	100 kΩ pull-up
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[30]	Input	100 kΩ pull-up
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[0]	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[1]	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[10]	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[11]	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[12]	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[13]	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[14]	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[15]	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[2]	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[3]	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[4]	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[5]	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[6]	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[7]	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[8]	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[9]	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CAS	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[0]	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[1]	Output	Low
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[0]	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[1]	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[10]	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[11]	Input	100 kΩ pull-up

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[9]	Input	100 kΩ pull-up
HDMI_CLKM	J5	HDMI_VPH					
HDMI_CLKP	J6	HDMI_VPH					
HDMI_D0M	K5	HDMI_VPH					
HDMI_D0P	K6	HDMI_VPH					
HDMI_D1M	J3	HDMI_VPH					
HDMI_D1P	J4	HDMI_VPH					
HDMI_D2M	K3	HDMI_VPH					
HDMI_D2P	K4	HDMI_VPH					
HDMI_HPD	K1	HDMI_VPH					
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	sjc.MOD	Input	100 kΩ pull-up
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	sjc.TCK	Input	47 kΩ pull-up
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	sjc.TDI	Input	47 kΩ pull-up
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	sjc.TDO	Output	Low
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	sjc.TMS	Input	47 kΩ pull-up
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	sjc.TRSTB	Input	47 kΩ pull-up
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[6]	Input	100 kΩ pull-up
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[8]	Input	100 kΩ pull-up
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[10]	Input	100 kΩ pull-up
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[12]	Input	100 kΩ pull-up
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[14]	Input	100 kΩ pull-up
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[7]	Input	100 kΩ pull-up
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[9]	Input	100 kΩ pull-up
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[11]	Input	100 kΩ pull-up
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[13]	Input	100 kΩ pull-up
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[15]	Input	100 kΩ pull-down
LVDS0_CLK_N	V4	NVCC_LVDS2P5					
LVDS0_CLK_P	V3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_CLK	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS2P5					
LVDS0_TX0_P	U1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX0	Input	Keeper