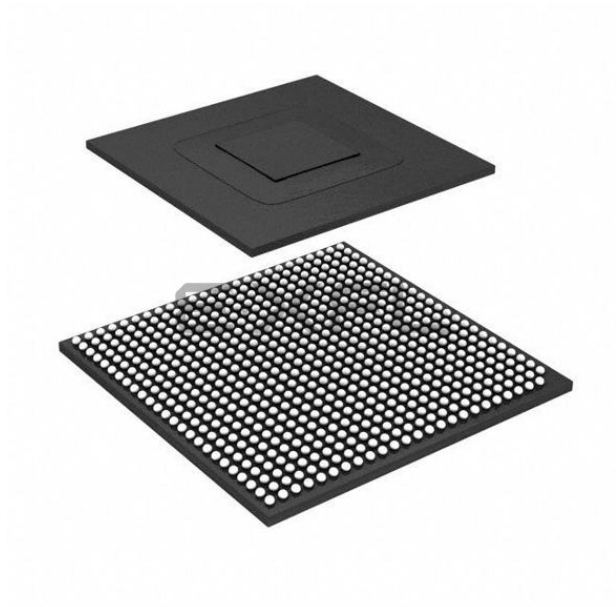

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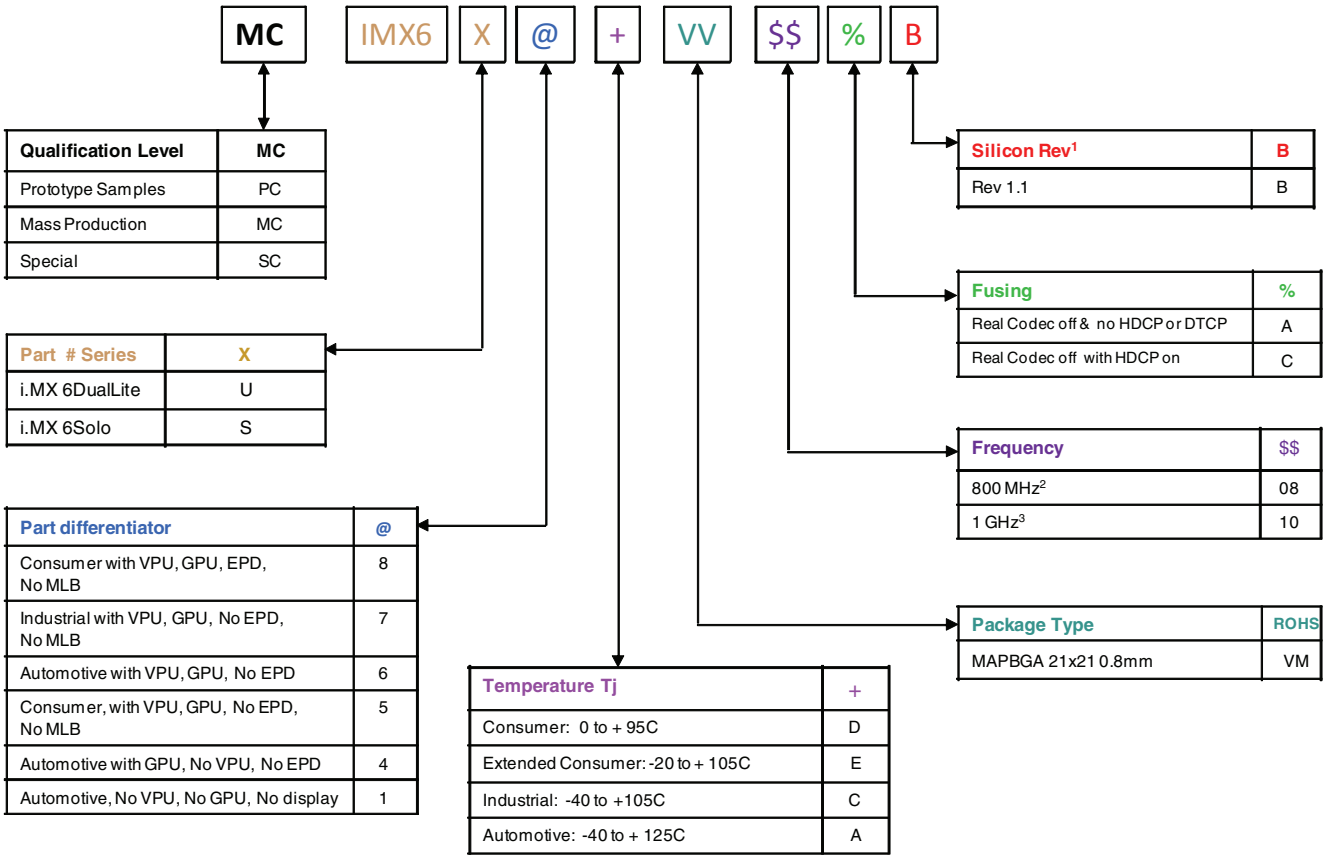
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u5evm10ac



1. See the freescale.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
3. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6DualLite and 6Solo

1.2 Features

The i.MX 6Solo/6DualLite processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- The i.MX 6Solo supports single ARM Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual ARM Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer

[2] For i.MX 6Solo, there is only one A9-core platform in the chip; for i.MX 6DualLite, there are two A9-core platforms.

Figure 2. i.MX 6Solo/6DualLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6Solo/6DualLite processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Solo/6DualLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Core Platform includes 1x (Solo) Cortex-A9 core for i.MX 6Solo and 2x (Dual) Cortex-A9 cores for i.MX 6DualLite. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
APBH-DMA	NAND Flash and BCH ECC DMA controller	System Control Peripherals	DMA controller used for GPMI2 operation
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse fox accessible through OCOTP_CTRL interface.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3Dv5	Graphics Processing Unit, ver.5	Multimedia Peripherals	The GPU3Dv5 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
HDMI Tx	HDMI Tx i/f	Multimedia Peripherals	The HDMI module provides HDMI standard i/f port to an HDMI 1.4 compliant display.
HSI	MIPI HSI i/f	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3 I^2C-4	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Solo/6DualLite processors, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OSC32KHz	OSC32KHz	Clocking	Generates 32.768 KHz clock from external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supply voltages[6]	NVCC_CSI, NVCC_EIM, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	
	NVCC_LVDS2P5[7] NVCC_MIPI	2.25	2.5	2.75	V	
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	
	HDMI_VPH	2.25	2.5	2.75	V	
PCIe supply voltages	PCIE_VP	1.023	1.1	1.225	V	
	PCIE_VPH	2.325	2.5	2.75	V	
	PCIE_VPTX	1.023	1.1	1.225	V	
Junction temperature Extended consumer	T_J	-20	—	105	°C	Refer to Consumer qualification report for details.
Junction temperature Standard consumer	T_J	0	—	95	°C	Refer to Consumer qualification report for details.

1 Applying the maximum voltage results in maximum power consumption and heat generation. Freescale recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDDARM_IN and VDDSOC_IN must be 125 mV higher than the LDO Output Set Point for correct regulator supply voltage.

3 VDDSOC_CAP and VDDPU_CAP must be equal.

4 VDDSOC and VDDPU output voltage must be set to this rule: VDDARM - VDDSOC/PU < 100 mV.

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not and associated IO pins need to have a Pullup or Pulldown resistor applied to limit any floating gate current.

7 This supply also powers the pre-drivers of the DDR IO pins, hence, it must be always provided, even when LVDS is not used

Table 10 shows on-chip LDO regulators that can supply on-chip loads.

Table 10. On-Chip LDOs[1] and their On-Chip Loads

Voltage Source	Load	Comment
VDDHIGH_CAP	NVCC_LVDS2P5	Board-level connection to VDDHIGH_CAP
	NVCC_MIPI	
	HDMI_VPH	
	PCIE_VPH	

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 39 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

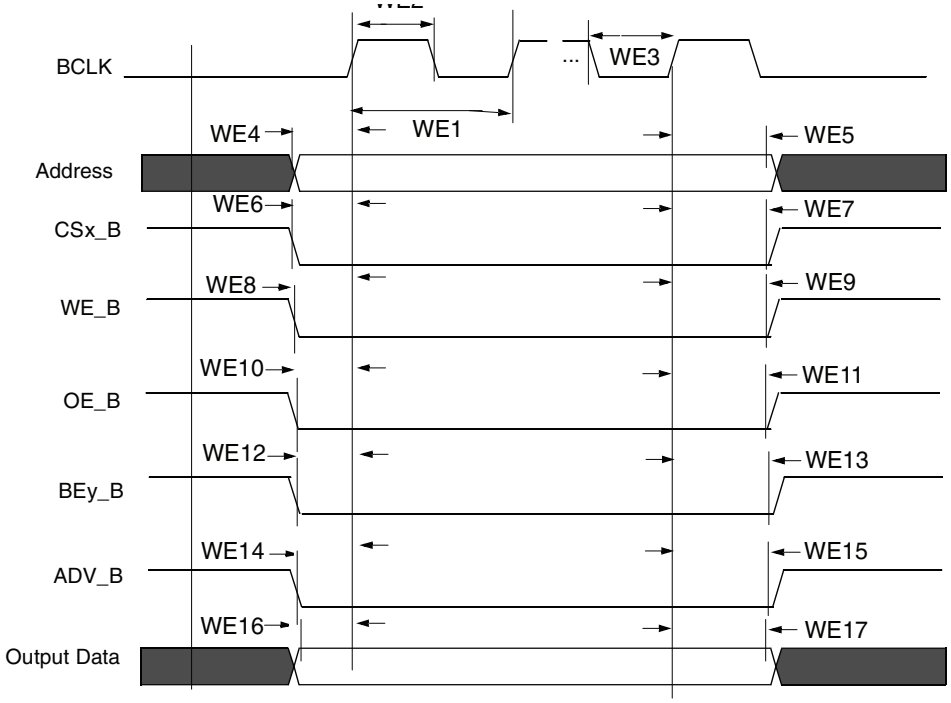


Figure 10. EIM Outputs Timing Diagram

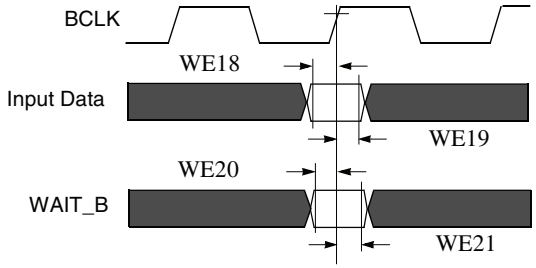


Figure 11. EIM Inputs Timing Diagram

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

2 In this table, CSA means WCSA when write operation or RCSA when read operation.

3 In this table, CSN means WCSN when write operation or RCSN when read operation.

4 t is axi_clk cycle time.

5 In this table, ADVN means WADVN when write operation or RADVN when read operation.

6 In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the basic timing parameters. The timing parameters for this diagram appear in Table 44.

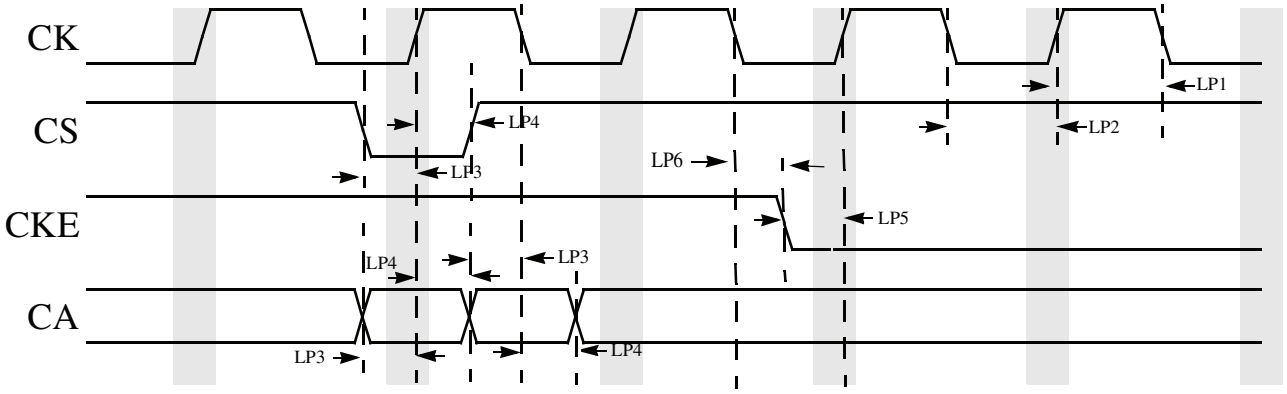


Figure 25. LPDDR2 Command and Address Timing Parameters

Table 44. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	CA, CS setup time	t_{IS}	380	—	ps
LP4	CA, CS hold time	t_{IH}	380	—	ps
LP5	CKE setup time	t_{ISCKE}	770	—	tck
LP6	CKE hold time	t_{IHCKE}	770	—	tck

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Table 48. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY x tCK	—	ns
NF19	CE# hold time	tCH	0.5 x tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5 x tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5 x tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

1 GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

For DDR Source sync mode, Figure 35 shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET(see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

Figure 45 shows MII receive signal timings. Table 56 describes the timing parameters (M1–M4) shown in the figure.

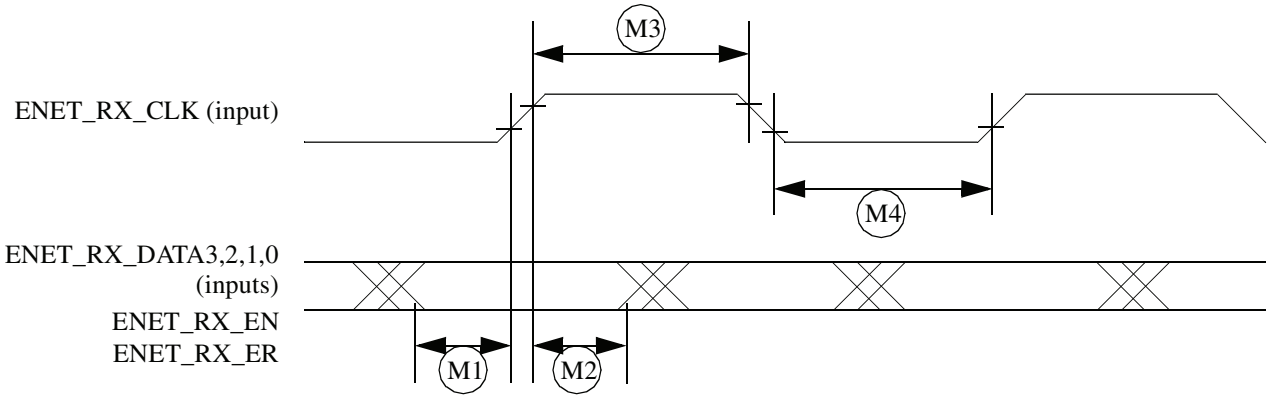


Figure 45. MII Receive Signal Timing Diagram

Table 56. MII Receive Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 48 shows MII asynchronous input timings. Table 59 describes the timing parameters (M10–M15) shown in the figure.

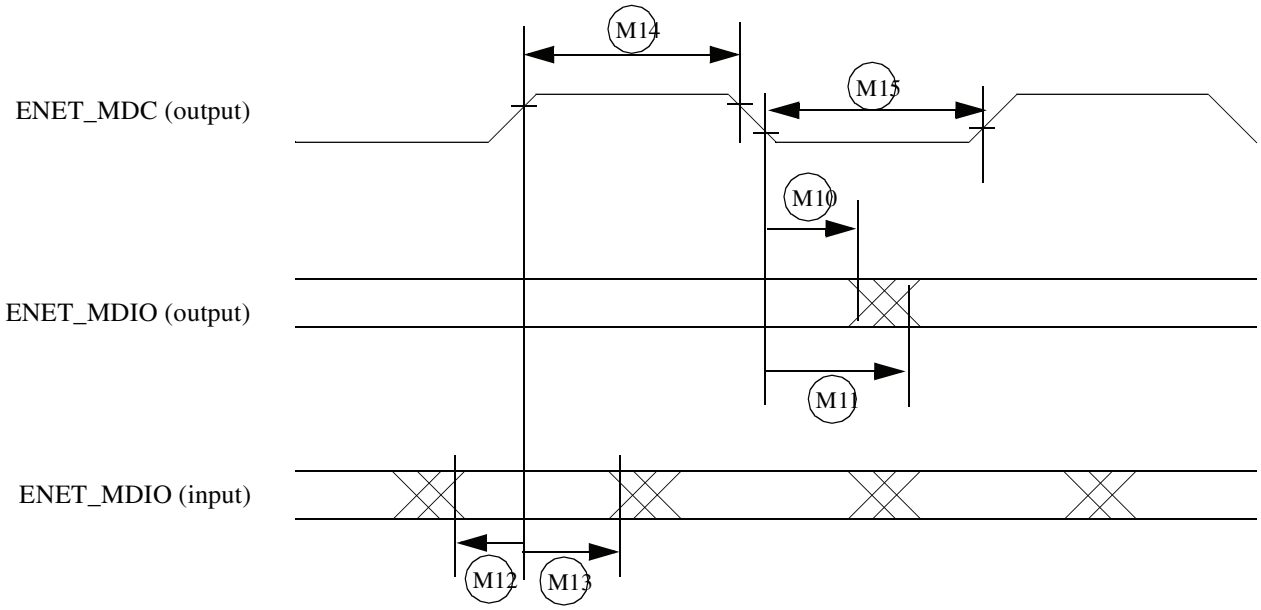


Figure 48. MII Serial Management Channel Timing Diagram

Table 59. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

Table 63. Switching Characteristics (continued)

$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 59.	—	—	1	UI[1]
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 60.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 60.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%

1 UI means TMDS clock unit.

2 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 61 depicts the timing of I²C module, and Table 64 lists the I²C module timing characteristics.

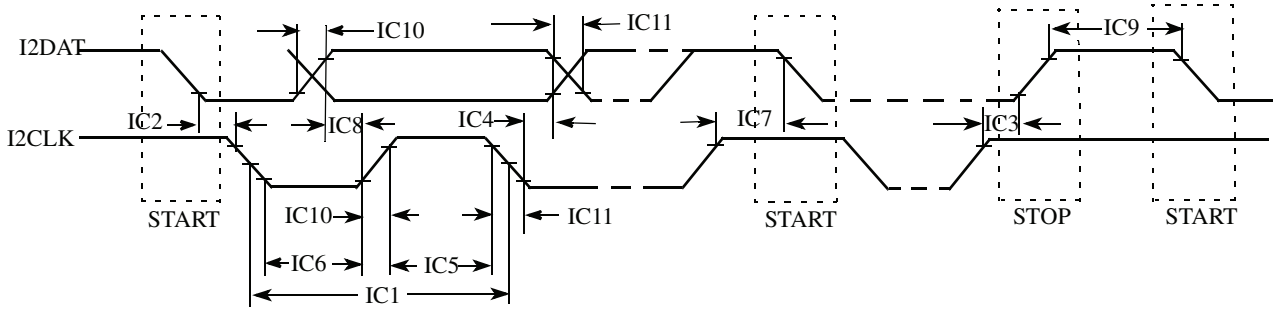


Figure 61. I²C Bus Timing

Table 64. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, "Gated Clock Mode,") except for the SENSB_HSYNC signal, which is not used (see Figure 63). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

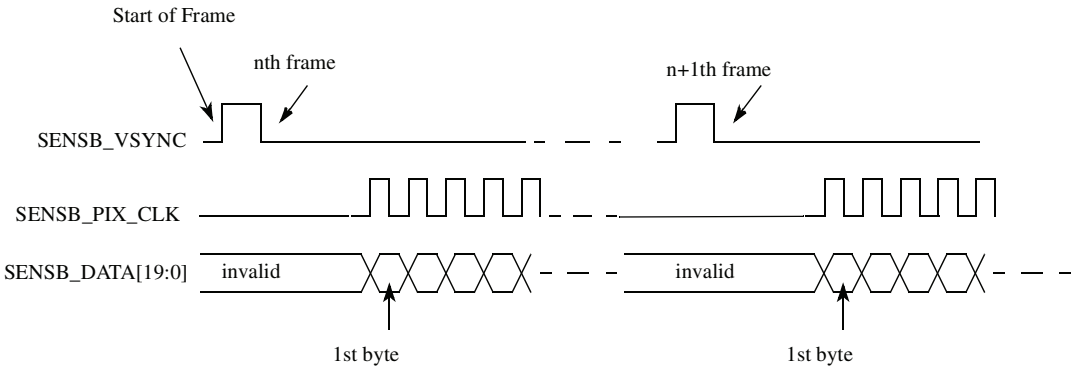


Figure 63. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 63 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.11.12.4 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

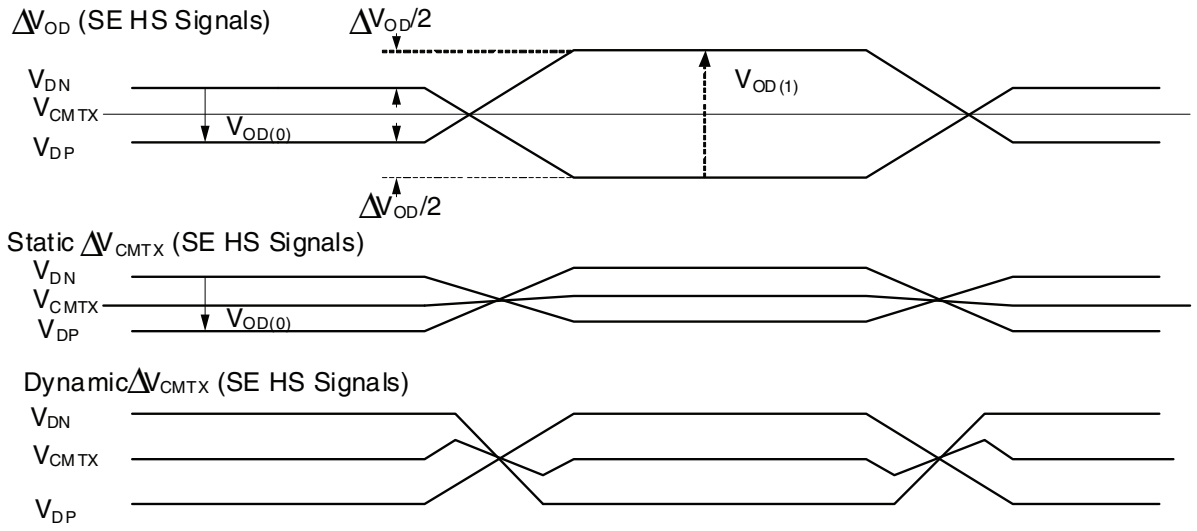


Figure 71. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.11.12.5 MIPI D-PHY Switching Characteristics

Table 72. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω<= RL< = 125 Ω	2	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time		—	1	—	UI
t_{CPL}	DDR CLK low time		—	1	—	UI
—	DDR CLK / DATA Jitter		—	75	—	ps pk–pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew		0.350		0.650	UI
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time		0.15			UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time		0.15			UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω			15	mV_{rms}

4.11.14 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.14.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.15 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 84 depicts the timing of the PWM, and Table 74 lists the PWM timing parameters.

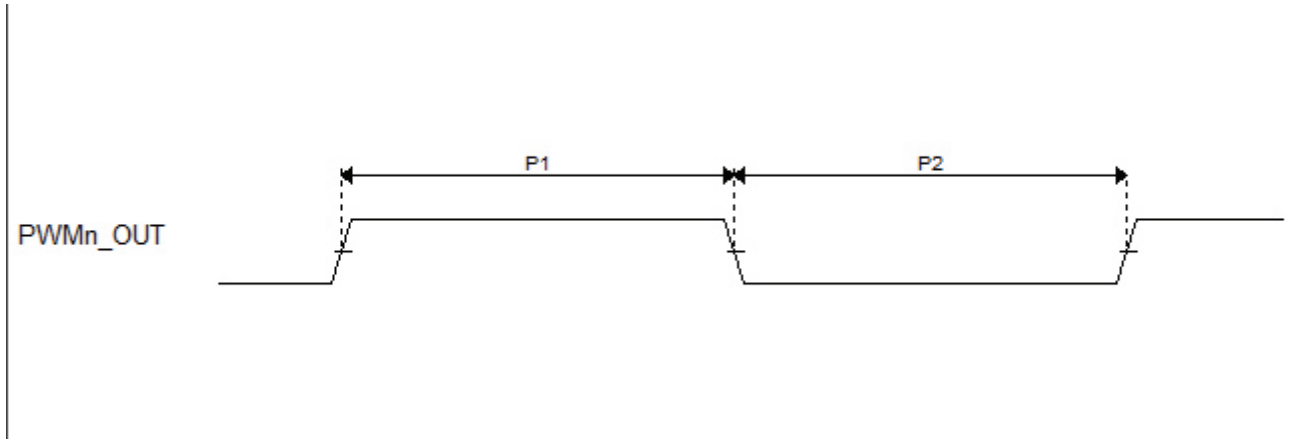


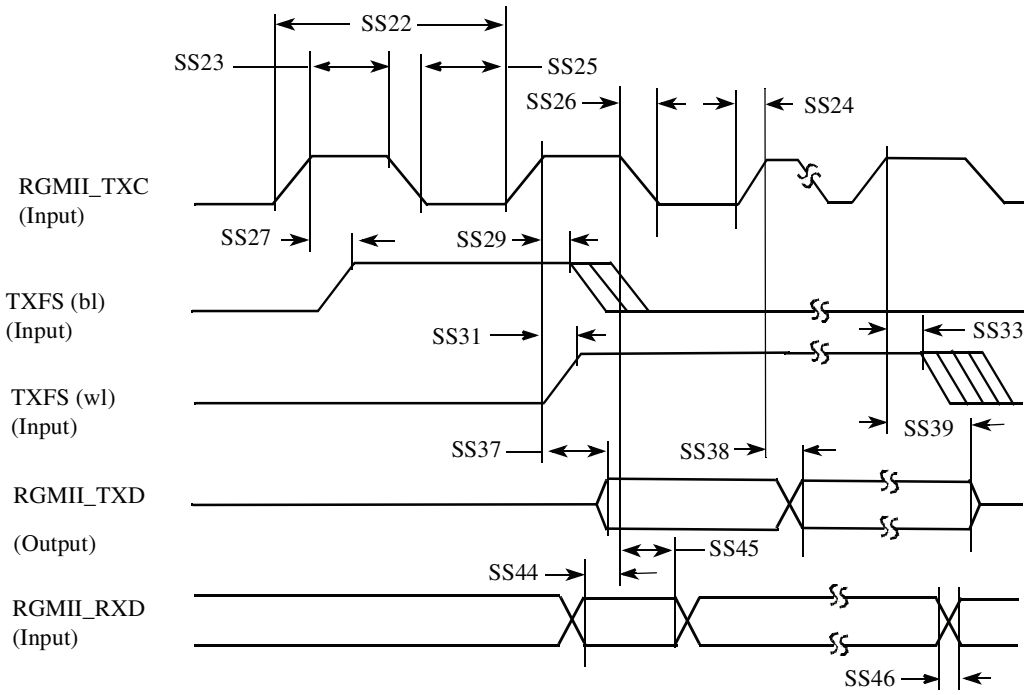
Figure 84. PWM Timing

Table 74. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15		ns
P2	PWM output pulse width low	15		ns

4.11.18.3 SSI Transmitter Timing with External Clock

Figure 93 depicts the SSI transmitter external clock timing and Table 80 lists the timing parameters for the transmitter timing with the external clock.



Note: SRXD Input in Synchronous mode only

Figure 93. SSI Transmitter External Clock Timing Diagram

Table 80. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
	External Clock Operation			
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	-10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	-10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

[1] The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.20 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.11.20.1 Transmit Timing

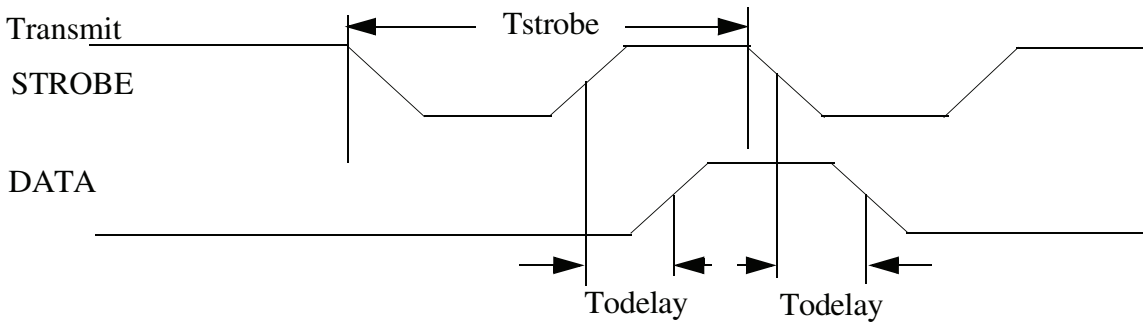


Figure 99. USB HSIC Transmit Waveform

Table 87. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[19]	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[20]	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[21]	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[22]	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[23]	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[24]	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[25]	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[26]	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[27]	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[28]	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[29]	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[30]	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[31]	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[0]	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[1]	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[10]	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[11]	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[12]	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[13]	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[14]	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[15]	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[2]	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[3]	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[4]	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[5]	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[6]	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[7]	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[8]	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[9]	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[0]	Output	High

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
EIM_EB1	K23	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[1]	Output	High
EIM_EB2	E22	NVCC_EIM	GPIO	ALT5	gpio2.GPIO[30]	Input	100 kΩ pull-up
EIM_EB3	F23	NVCC_EIM	GPIO	ALT5	gpio2.GPIO[31]	Input	100 kΩ pull-up
EIM_LBA	K22	NVCC_EIM	GPIO	ALT0	weim.WEIM_LBA	Output	High
EIM_OE	J24	NVCC_EIM	GPIO	ALT0	weim.WEIM_OE	Output	High
EIM_RW	K20	NVCC_EIM	GPIO	ALT0	weim.WEIM_RW	Output	High
EIM_WAIT	M25	NVCC_EIM	GPIO	ALT0	weim.WEIM_WAIT	Input	100 kΩ pull-up
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[25]	Input	100 kΩ pull-up
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[31]	Input	100 kΩ pull-up
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[22]	Input	100 kΩ pull-up
ENET_REF_CLK	V22	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[23]	Input	100 kΩ pull-up
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[24]	Input	100 kΩ pull-up
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[27]	Input	100 kΩ pull-up
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[26]	Input	100 kΩ pull-up
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[28]	Input	100 kΩ pull-up
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[30]	Input	100 kΩ pull-up
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[29]	Input	100 kΩ pull-up
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[0]	Input	100 kΩ pull-down
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[1]	Input	100 kΩ pull-up
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	gpio7.GPIO[11]	Input	100 kΩ pull-up
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	gpio7.GPIO[12]	Input	100 kΩ pull-up
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	gpio7.GPIO[13]	Input	100 kΩ pull-up
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[5]	Input	100 kΩ pull-up
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[2]	Input	100 kΩ pull-up
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[3]	Input	100 kΩ pull-up
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[4]	Input	100 kΩ pull-up
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[5]	Input	100 kΩ pull-up
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[6]	Input	100 kΩ pull-up
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[7]	Input	100 kΩ pull-up
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[8]	Input	100 kΩ pull-up

Table 92. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[2]	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[3]	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[4]	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[5]	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[6]	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[7]	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[10]	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[9]	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	src.RESET_B	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH					
PCIE_RXP	B2	PCIE_VPH					
PCIE_TXM	A3	PCIE_VPH					
PCIE_TXP	B3	PCIE_VPH					
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	Output	Low
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm.PMIC_VSTBY_REQ	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src.POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[25]	Input	100 kΩ pull-up
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[27]	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[28]	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[29]	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[24]	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[30]	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[20]	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[21]	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[22]	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[23]	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[26]	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[19]	Input	100 kΩ pull-down