Welcome to E-XFL.COM

Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7014S)
Speed	766MHz
Flash Size	32MB
RAM Size	1GB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0720-03-14s-1c

1 Table of Contents

1 Table of Contents 2
2 Overview 4
2.1 Key Features 4
2.2 Block Diagram 5
2.3 Main Components 6
2.4 Initial Delivery State 7
3 Boot Process 8
4 Signals, Interfaces and Pins 9
4.1 Board to Board (B2B) I/Os 9
4.2 JTAG Interface 10
4.3 System Controller CPLD I/O Pins 10
4.4 Quad SPI Interface 11
4.5 eMMC Interface 11
4.6 Ethernet Interface 12
4.7 USB Interface 13
4.8 I2C Interface 14
5 On-board Peripherals 16
5.1 System Controller CPLD 16
5.2 DDR Memory 16
5.3 Quad SPI Flash Memory 16
5.4 eMMC Flash Memory 16
5.5 Gigabit Ethernet PHY 17
5.6 High-speed USB ULPI PHY 17
5.7 RTC - Real Time Clock 17
5.8 MAC-Address EEPROM 18
5.9 Atmel CryptoAuthentication Chip 18
5.10 eCompass module 18
5.11 Oscillators 18
5.12 On-board LEDs 19
6 Power and Power-On Sequence 20

6.1 Power Supply 20
6.2 Power-On Sequence 20
6.3 Power Rails 21
6.4 Bank Voltages 22
7 Board to Board Connectors 24
7.1 Connector Mating height 24
7.2 Connector Speed Ratings 24
7.3 Current Rating 25
7.4 Connector Mechanical Ratings 25
7.5 Manufacturer Documentation 25
8 Variants Currently in Production 26
9 Technical Specifications 27
9.1 Absolute Maximum Ratings 27
9.2 Recommended Operating Conditions 28
9.3 Operating Temperature Ranges 28
9.4 Physical Dimensions 28
10 Revision History 30
10.1 Hardware Revision History 30
10.2 Document Change History 30
11 Disclaimer 31
11.1 Document Warranty 31
11.2 Limitation of Liability 31
11.3 Copyright Notice 31
11.4 Technology Licenses 31
11.5 Environmental Protection 31
11.6 REACH, RoHS and WEEE 32

- Evenly spread supply pins for good signal integrity
- Rugged for shock and high vibration

Additional assembly options are available for cost or performance optimization upon request.

2.2 Block Diagram

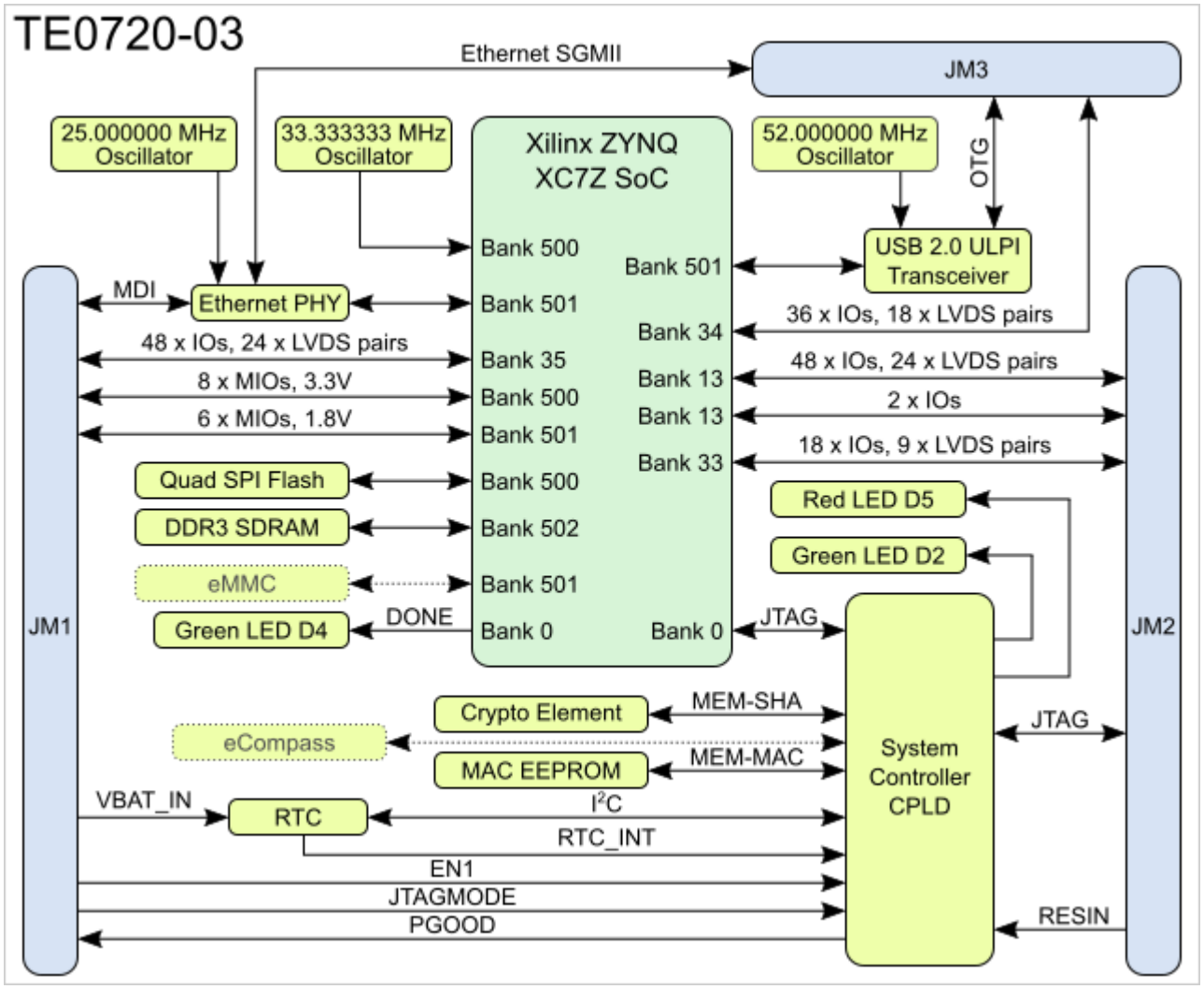


Figure 1: TE0720-03 block diagram.

Components and connections marked with dashed lines are optional or may be missing on some module variants, please contact us for additional information.

2.3 Main Components

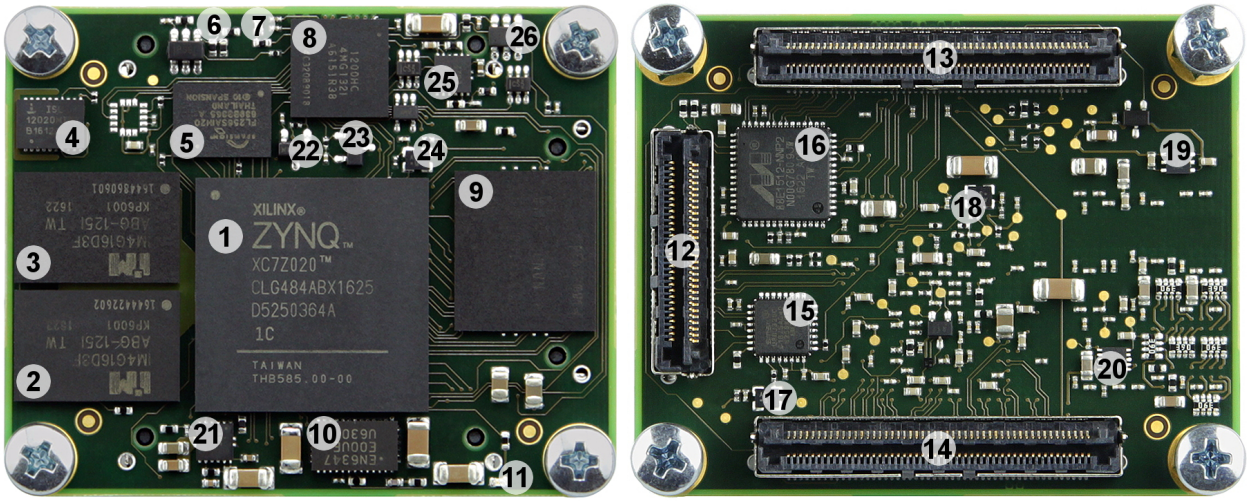


Figure 2: Main components of the module.

1. Xilinx Zynq XC7Z SoC, U5
2. 4 Gbit DDR3/L SDRAM, U13
3. 4 Gbit DDR3/L SDRAM, U12
4. Low-power RTC with battery backed SRAM, U20
5. 32 MByte Quad SPI Flash memory, U7
6. Red LED (LED1), D5
7. Green LED (LED2), D2
8. System Controller CPLD, U19
9. eMMC NAND Flash, U15
10. 4A high-efficiency PowerSoC DC-DC step-down converter (1V), U1
11. Green LED (DONE), D4
12. B2B connector Samtec Razor Beam™ LSHM-130, JM3
13. B2B connector Samtec Razor Beam™ LSHM-150, JM1
14. B2B connector Samtec Razor Beam™ LSHM-150, JM2
15. Hi-speed USB 2.0 ULPI transceiver, U18
16. Gigabit Ethernet (GbE) transceiver, U8
17. Low-power programmable oscillator @ 52.000000 MHz (OTG-RCLK), U14
18. Low-power programmable oscillator @ 33.333333 MHz (PS-CLK), U6
19. Low-dropout regulator (VBATT), U24
20. DDR termination regulator, U4
21. 1.5A PowerSoC DC-DC step-down converter with integrated inductor (1.5V), U2
22. Atmel CryptoAuthentication chip, U10
23. 2Kbit UNI/O® serial EEPROM with EUI-48™ node identity, U17
24. Low-power programmable oscillator @ 25.000000 MHz (ETH-CLK), U9
25. 1.5A PowerSoC DC-DC step-down converter with integrated inductor (1.8V), U3
26. 3A PFET load switch with configurable slew rate (3.3V), Q1

2.4 Initial Delivery State

Storage device name	IC	Content	Notes
Quad SPI Flash	U 7	Empty	-
eMMC NAND Flash	U 15	Empty	-
11AA02E48T EEPROM	U 17	Pre-programmed globally unique, 48-bit node address (MAC)	-
System Controller CPLD	U 19	Standard firmware.	Download firmware

Table 1: Initial state of programmable devices on delivery of the module.

4 Signals, Interfaces and Pins

4.1 Board to Board (B2B) I/Os

PL I/O signal connections between Zynq SoC's I/O banks and B2B connectors, 152 HR GPIOs total.

Bank	Type	Voltage	B2B	I/O Count	Notes
13	HR GPIO	VCCIO13	JM2	48	24 LVDS pairs
13	HR GPIO	VCCIO13	JM2	2	B13_IO0 and B13_IO25
33	HR GPIO	VCCIO33	JM2	18	9 LVDS pairs
34	HR GPIO	VCCIO34	JM3	36	18 LVDS pairs
35	HR GPIO	VCCIO35	JM1	48	24 LVDS pairs

Table 2: General PL I/O to B2B connectors information.

PS MIO bank 500 and 501 signal connections to B2B JM1 connector, 14 PS MIOs total.

MIO	B2B Pin	Bank	Voltage	Notes
0	JM1-87	500	3.3V	
9	JM1-91	500	3.3V	
10	JM1-95	500	3.3V	
11	JM1-93	500	3.3V	
12	JM1-99	500	3.3V	
13	JM1-97	500	3.3V	
14	JM1-92	500	3.3V	Also wired to U19-M4
15	JM1-85	500	3.3V	Also wired to U19-N4
40	JM1-27	501	1.8V	Zynq SoC SD0
41	JM1-25	501	1.8V	Zynq SoC SD0
42	JM1-23	501	1.8V	Zynq SoC SD0
43	JM1-21	501	1.8V	Zynq SoC SD0

44	JM1-19	501	1.8V	Zynq SoC SD0
45	JM1-17	501	1.8V	Zynq SoC SD0

Table 3: General PS MIO connections information.

For detailed information about the pin-out, please refer to the Pin-out tables.

4.2 JTAG Interface

JTAG access to the Zynq SoC and System Controller CPLD is provided through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

Table 4: JTAG pins connection.

⚠ JTAGMODE pin 89 in B2B connector JM1 is used to switch access between devices, low selects Zynq SoC, high selects System Controller CPLD.

4.3 System Controller CPLD I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
RESIN	Input	Reset input	Active low reset input, default mapping forces POR_B reset to Zynq PS.
PGOOD	Output	Power good	Active high when all on-module power supplies are working properly.
MODE	Input	Boot mode	Force low for boot from the SD card. Latched at power-on only, not during soft reset!

48	MMC-CLK	W6
49	MMC-D1	H4
50	MMC-D2	H5
51	MMC-D3	J2

Table 7: eMMC interface MIOs and pins.

4.6 Ethernet Interface

The Marvell Alaska 88E1512 (U8) is a physical layer device containing a single Gigabit Ethernet transceiver and three separate major electrical interfaces: MDI interface to copper cable, SERDES/SGMII interface and RGMII interface. RGMII interface is connected to the Zynq SoC PS bank 501 MIO pins, see tables below.

SGMII (SFP copper or fiber) pins are routed to the B2B connector JM3 and MDI pins are routed to the B2B connector JM1 (see table below).

Ethernet PHY to B2B connections

PHY Signal	B2B Pin		PHY Signal	B2B Pin
SOUT_N	JM3-1		PHY_MDI1_P	JM1-10
SOUT_P	JM3-3		PHY_MDI1_N	JM1-12
SIN_N	JM3-2		PHY_MDI2_P	JM1-16
SIN_P	JM3-4		PHY_MDI2_N	JM1-18
PHY_MDI0_P	JM1-4		PHY_MDI3_P	JM1-22
PHY_MDI0_N	JM1-6		PHY_MDI3_N	JM1-24

Table 8: Ethernet PHY to B2B connections.

Ethernet PHY to Zynq SoC PS MIO ETH0 connections

PHY Signal	SoC MIO		PHY Signal	SoC MIO
ETH-TXCK	16		ETH-RXCK	22
ETH-TXD0	17		ETH-RXD0	23
ETH-TXD1	18		ETH-RXD1	24
ETH-TXD2	19		ETH-RXD2	25

ETH-TXD3	20		ETH-RXD3	26
ETH-TXCTL	21		ETH-RXCTL	27
ETH-MDC	52		ETH-MDIO	53

Table 9: Ethernet PHY to Zynq SoC connections.

4.7 USB Interface

Hi-speed USB ULPI PHY is provided by USB3320 from Microchip (U18). The ULPI interface is connected to the Zynq SoC PS USB0 via MIO28..39, bank 501.

USB PHY Signal	Wired to	SoC MIO
OTG-DATA4	U18-7	28
OTG-DIR	U18-31	29
OTG-STP	U18-29	30
OTG-NXT	U18-2	31
OTG-DATA0	U18-3	32
OTG-DATA1	U18-4	33
OTG-DATA2	U18-5	34
OTG-DATA3	U18-6	35
OTG-CLK	U18-1	36
OTG-DATA5	U18-9	37
OTG-DATA6	U18-10	38
OTG-DATA7	U18-13	39

Table 10: USB ULPI PHY to Zynq SoC connections.

USB PHY connection

USB PHY Pin	SC CPLD Pin	B2B Name	Notes
REFSEL0..2	-	-	Reference clock frequency select, all set to GND = 52.000000 MHz.
RESETB	B14, bank 1	-	Active low reset.
CLKOUT	-	-	ULPI output clock connected to Zynq PS MIO36.
DP, DM		OTG-D_P, OTG-D_N	USB data lines.
CPEN		VBUS_V_EN	External USB power switch active high enable signal.
VBUS	-	USB-VBUS	Connect to USB VBUS via a series of resistors, see reference schematic.
ID	-	OTG-ID	For A-device connect to the ground, for B-device leave floating.
SPK_L	M5, bank 2	-	In USB audio mode a switch connects the DM pin to the SPK_L.
SPK_R	M8, bank 2	-	In USB audio mode a switch connects the DP pin to the SPK_R.

Table 11: USB ULPI PHY connections.

4.8 I2C Interface

On-board I^2C devices are connected to the System Controller CPLD which acts as a I^2C bus repeater for the Zynq SoC. System Controller CPLD signals X1, X3 and X7 are routed to Zynq SoC bank 34. Exact functionality depends on the System Controller CPLD firmware.

Signal Name	SC CPLD Pin	SoC Pin	Notes
X1	F1	L16	SCL, I2C clock.
X5	J1	P22	SDA, I2C data out.
X7	M1	N22	SDA, I2C data in.

Table 12: Zynq SoC to System Controller CPLD I^2C bus.

5.8 MAC-Address EEPROM

A Microchip 2Kbit 11AA02E48 serial EEPROM (U17) is connected to the System Controller CPLD pin M14 via single-I/O UNI/O serial interface and contains pre-programmed globally unique 48-bit node address compatible with EUI-48™ specification. Chip is programmed at the factory with a globally unique node address stored in the upper 1/4 of the memory array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

5.9 Atmel CryptoAuthentication Chip

The ATSHA204A Atmel CryptoAuthentication™ chip (U10) is connected to the System Controller CPLD pin N14 via single-wire interface providing various security functions and features such as anti-counterfeiting, firmware/media protection, password validation, secure session key exchanging, secure data storage and more. Refer to the product datasheet for more information.

5.10 eCompass module

Optionally TE0720 module can be fitted with ultra-compact high-performance eCompass device (LSM303D, U22) featuring 3D accelerometer and 3D magnetometer.

5.11 Oscillators

Source	Signal	Frequency	Destination	Pin Name	Notes
U6	PS-CLK	33.333333 MHz	U5	PS_CLK_500	Zynq SoC PS subsystem main clock.
U14	OTG-RCLK	52.000000 MHz	U18	REFCLK	USB3320C PHY reference clock.
U9	ETH-CLK	25.000000 MHz	U8	XTAL_IN	88E1512 PHY reference clock.

Table 16: Oscillators.

5.12 On-board LEDs

LED	Color	Connected to	Description and Notes
D2	Green	LED1	Controlled by System Controller CPLD firmware.
D4	Green	DONE	
D5	Red	LED2	Controlled by System Controller CPLD firmware.

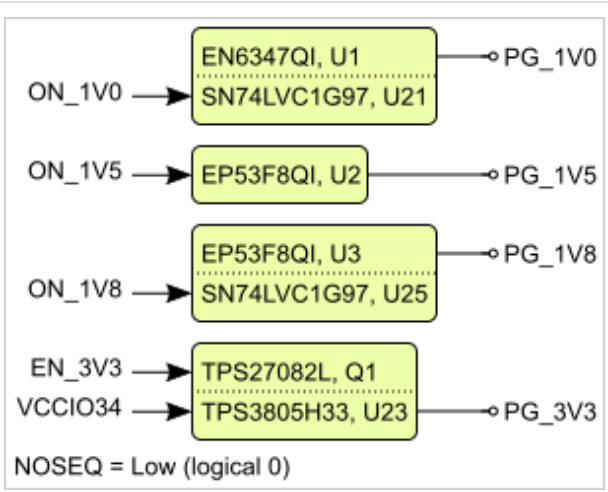
Table 17: On-board LEDs.

It is important that all carrier board I/Os are 3-stated at power-on until System Controller CPLD sets PGOOD signal high (B2B connector JM1, pin 30), or 3.3V is present on B2B connector JM2 pins 10 and 12, meaning that all on-module voltages have become stable and module is properly powered up.

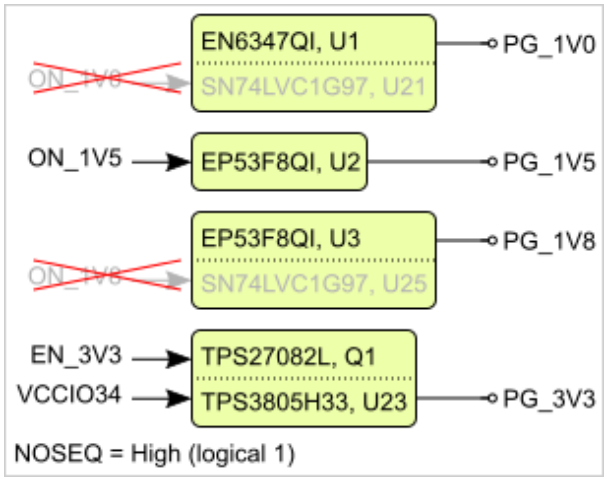
See also Xilinx datasheet DS187 for additional information. User should also check related carrier board documentation when choosing carrier board design for TE0720 module.

NOSEQ input signal

NOSEQ input signal from the carrier board can be used to control output of the two DC-DC converters U1 and U3. It works in conjunction with the System Controller CPLD firmware controlled ON_1V0 and ON_1V8 input signals of the U21 and U25 gate ICs.



If NOSEQ input signal from the carrier board is low (logical 0), signals ON_1V0 and ON_1V8 can be driven by System Controller CPLD to control outputs of the U1 and U3 DC-DC converters.



If NOSEQ input signal from the carrier board is high (logical 1), state of the ON_1V0 and ON_1V8 signals is irrelevant and DC-DC converters U1 and U3 outputs are always enabled.

Figure 4: Power sequencing.

⚠ Initial state of the ON_1V0 and ON_1V8 signals and therefore also functionality of the NOSEQ signal depend on the System Controller CPLD firmware.

6.3 Power Rails

B2B Name	B2B JM1 Pins	B2B JM2 Pins	Direction	Note
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage from carrier board.

3.3VIN	13, 15	91	Input	Supply voltage from carrier board. JM2-91 is VREF_JTAG.
VCCIO35	9, 11	-	Input	High range bank voltage from carrier board.
VCCIO33	-	5	Input	High range bank voltage from carrier board.
VCCIO13	-	7, 9	Input	High range bank voltage from carrier board.
VCCIO34	-	1, 3	Input	High range bank voltage from carrier board.
VBAT_IN	79	-	Input	RTC battery-buffer supply voltage.
3.3V	-	10, 12	Output	Internal 3.3V voltage level.
1.8V	39	-	Output	Internal 1.8V voltage level.
1.5V [1)]	-	19	Output	Internal 1.5V voltage level.

Table 19: Module power rails.

[1)] In case of module variant of TE0720-03-L1IF which uses Xilinx Zynq XC7Z020-L1CLG484I chip with lower power consumption, power rails named 1.5V and VCCO_DDR_502 voltage is actually 1.35V. To achieve this, a resistor with different value is used for R4 (see schematic of the TE0720-03-L1IF for more information).

6.4 Bank Voltages

Bank	Schematic Name	Voltage	Notes
500	3.3V, VCCO_MIO0_500	3.3V	
501	1.8V, VCCO_MIO1_501	1.8V	
502	1.5V, VCCO_DDR_502	1.5V	
0 Config	3.3V	3.3V	

7 Board to Board Connectors

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

7.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Connector on baseboard	compatible to	Mating height
REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

The module can be manufactured using other connectors upon request.

7.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps

12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

7.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

7.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

7.5 Manufacturer Documentation

Geändert
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz
07 04, 2016 by Thorsten Trenz

8 Variants Currently in Production

Module Variant	Zynq SoC	RAM	eMMC Size	Temperature Range	B2B Connector Height
TE0720-03-2IF	XC7Z020-2CLG484I	1 GByte	4 GByte	Industrial	4.0 mm
TE0720-03-2IF C3	XC7Z020-2CLG484I	1 GByte	4 GByte	Industrial	2.5 mm
TE0720-03-2IF C8	XC7Z020-2CLG484I	1 GByte	32 GByte	Industrial	4.0 mm
TE0720-03-L1IF	XC7Z020-L1CLG484I	512 MByte	4 GByte	Industrial	4.0 mm
TE0720-03-1CF	XC7Z020-1CLG484C	1 GByte	4 GByte	Commercial	4.0 mm
TE0720-03-1CR	XC7Z020-1CLG484C	256 MByte	-	Commercial	4.0 mm
TE0720-03-14S-1C	XC7Z014S-1CLG484C	1 GByte	4 GByte	Commercial	4.0 mm
TE0720-03-1QF	XA7Z020-1CLG484Q	1 GByte	4 GByte	Automotive	4.0 mm

Table 21: Module variants currently in production.

9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	-0.3	6.5	V	EP53F8QI datasheet.
3.3VIN supply voltage	-0.1	3.75	V	TPS27082L and LCMXO2-1200HC datasheets.
Supply voltage for PS MIO banks	-0.5	3.6	V	See Xilinx DS187 datasheet.
I/O input voltage for MIO banks	-0.4	VCCO_MIO + 0.55	V	See Xilinx DS187 datasheet. (VCCO_MIO0_500, VCCO_MIO1_501)
Supply voltage for HR I/Os banks	-0.5	3.6	V	See Xilinx DS187 datasheet. (VCCIO13, VCCIO33, VCCIO34, VCCIO35)
I/O input voltage for HR I/O banks	-0.4	VCCIO + 0.55	V	See Xilinx DS187 datasheet.
Storage temperature	-40	+85	°C	-
Storage temperature without the ISL12020MIRZ, eMMC Flash and 88E1512 PHY installed	-55	+100	°C	NB! Module variants using Nanya SDRAM chips, max temperature limit is +125 °C.

Table 22: Module absolute maximum ratings.

⚠ Assembly variants for higher storage temperature range are available on request.

⚠ Please check Xilinx datasheet DS187 for complete list of absolute maximum and recommended operating ratings.

9.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	2.5	5.5	V	EN6347QI and EP53F8QI datasheets.
3.3VIN supply voltage	3.135	3.465	V	3.3V +/- 5%.
Supply voltage for PS MIO banks	1.71	3.465	V	See Xilinx DS187 datasheet.
I/O input voltage for PS MIO banks	-0.20	VCCO_MIO + 0.20	V	See Xilinx DS187 datasheet.
Supply voltage for HR I/Os banks	1.14	3.465	V	See Xilinx DS187 datasheet.
I/O input voltage for HR I/O banks	-0.20	VCCIO + 0.20	V	See Xilinx DS187 datasheet.

Table 23: Recommended operating conditions.

9.3 Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial and automotive grade: -40°C to +85°C.

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.
- PCB thickness: 1.6 mm.
- Highest part on PCB: approx. 2.5 mm. Please download the step model for exact numbers.

All dimensions are given in millimeters.

11.6 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.