



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - Microcontroller, Microprocessor, FPGA Modules](#)

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

### Applications of [Embedded - Microcontroller,](#)

#### Details

Product Status	Discontinued at Digi-Key
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7020)
Speed	-
Flash Size	32MB
RAM Size	1GB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	<a href="https://www.e-xfl.com/product-detail/trenz-electronic/te0720-03-2if">https://www.e-xfl.com/product-detail/trenz-electronic/te0720-03-2if</a>

## 1 Table of Contents

1	Table of Contents.....	2
2	Overview.....	4
2.1	Key Features.....	4
2.2	Block Diagram.....	5
2.3	Main Components.....	6
2.4	Initial Delivery State.....	7
3	Boot Process.....	8
4	Signals, Interfaces and Pins.....	9
4.1	Board to Board (B2B) I/Os.....	9
4.2	JTAG Interface.....	10
4.3	System Controller CPLD I/O Pins.....	10
4.4	Quad SPI Interface.....	11
4.5	eMMC Interface.....	11
4.6	Ethernet Interface.....	12
4.7	USB Interface.....	13
4.8	I2C Interface.....	14
5	On-board Peripherals.....	16
5.1	System Controller CPLD.....	16
5.2	DDR Memory.....	16
5.3	Quad SPI Flash Memory.....	16
5.4	eMMC Flash Memory.....	16
5.5	Gigabit Ethernet PHY.....	17
5.6	High-speed USB ULPI PHY.....	17
5.7	RTC - Real Time Clock.....	17
5.8	MAC-Address EEPROM.....	18
5.9	Atmel CryptoAuthentication Chip.....	18
5.10	eCompass module.....	18
5.11	Oscillators.....	18
5.12	On-board LEDs.....	19
6	Power and Power-On Sequence.....	20

6.1	Power Supply .....	20
6.2	Power-On Sequence .....	20
6.3	Power Rails .....	21
6.4	Bank Voltages .....	22
7	Board to Board Connectors .....	24
7.1	Connector Mating height .....	24
7.2	Connector Speed Ratings .....	24
7.3	Current Rating .....	25
7.4	Connector Mechanical Ratings .....	25
7.5	Manufacturer Documentation .....	25
8	Variants Currently in Production .....	26
9	Technical Specifications .....	27
9.1	Absolute Maximum Ratings .....	27
9.2	Recommended Operating Conditions .....	28
9.3	Operating Temperature Ranges .....	28
9.4	Physical Dimensions .....	28
10	Revision History .....	30
10.1	Hardware Revision History .....	30
10.2	Document Change History .....	30
11	Disclaimer .....	31
11.1	Document Warranty .....	31
11.2	Limitation of Liability .....	31
11.3	Copyright Notice .....	31
11.4	Technology Licenses .....	31
11.5	Environmental Protection .....	31
11.6	REACH, RoHS and WEEE .....	32

## 2 Overview

Refer to <https://wiki.trenz-electronic.de/display/PD/TE0720+TRM> for online version of this manual and additional technical documentation of the product.

The Trenz Electronic TE0720 is an industrial-grade SoM (System on Module) based on [Xilinx Zynq-7000 SoC](#) (XC7Z020 or XC7Z014S) with up to 1 GB of DDR3/L SDRAM, 32MB of SPI flash memory, Gigabit Ethernet PHY transceiver, a USB PHY transceiver and powerful switching-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking strips. See also Variants Currently in Production section.

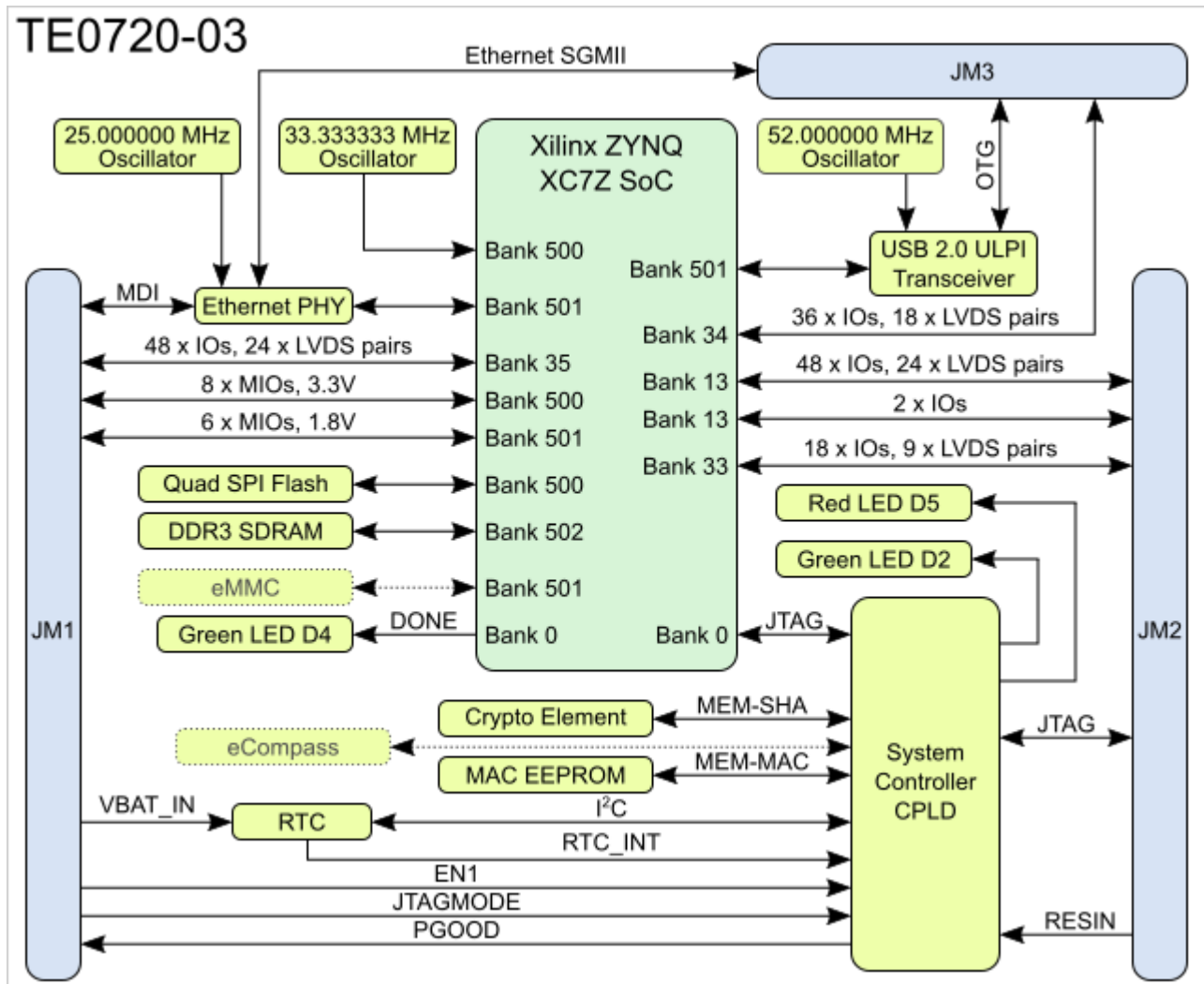
### 2.1 Key Features

- Xilinx XC7Z SoC (XC7Z020 or XC7Z014S)
  - Processing system (PS):
    - XC7Z020: Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
    - XC7Z014S: Single-core ARM Cortex-A9 MPCore™ with CoreSight™
    - L1 cache: 32 KByte instruction, 32 KByte data per processor
    - L2 cache: Unified 512 KByte
  - Programmable logic (PL): Artix-7 FPGA
    - Programmable logic cells: 85K (XC7Z020), 65K (XC7Z014S)
    - Block RAM: 4.9 MByte (XC7Z020), 3.8 MByte (XC7Z014S)
    - DSP slices: 220 (XC7Z020), 170 (XC7Z014S)
    - Peak DSP performance: 276 GMACs (XC7Z020), 187 GMACs (XC7Z014S)
    - 2x 12 bit, MSPS ADCs with up to 17 differential inputs
- 54 multiuse I/O (MIO) pins
- 152 High-Range (HR) I/O pins (SelectIO interfaces)
- System Controller CPLD ([Lattice LCMXO2-1200HC](#))
- Up to 1 GByte DDR3/L SDRAM memory (2 x 256 Mbit x 16, 32-bit wide data bus).
- 32 MByte Quad SPI Flash memory
- Gigabit Ethernet transceiver PHY ([Marvell 88E1512](#))
- MAC address serial EEPROM with EUI-48™ node identity ([11AA02E48](#))
- Highly integrated full-featured hi-speed USB 2.0 ULPI transceiver ([Microchip USB3320C-EZK](#))
- 3-axis accelerometer and 3-axis magnetometer ([ST Microelectronics LSM303DTR](#)) (Optional!)
- Real time clock with embedded crystal ([Intersil ISL12020M](#)): ±5ppm accuracy
- Atmel CryptoAuthentication element ([Atmel ATSHA204A](#))
- Up to 32 GByte eMMC, usually 4 GByte, depends on module variant and assembly option
- User LED 1 (Green), user LED 2 (Red), user LED 3 - FPGA DONE (Green)
- On-board high-efficiency DC-DC converters for all voltages used
- Trenz 4 x 5 module socket connectors (3 x [Samtec LSHM series connectors](#))

- Evenly spread supply pins for good signal integrity
- Rugged for shock and high vibration

Additional assembly options are available for cost or performance optimization upon request.

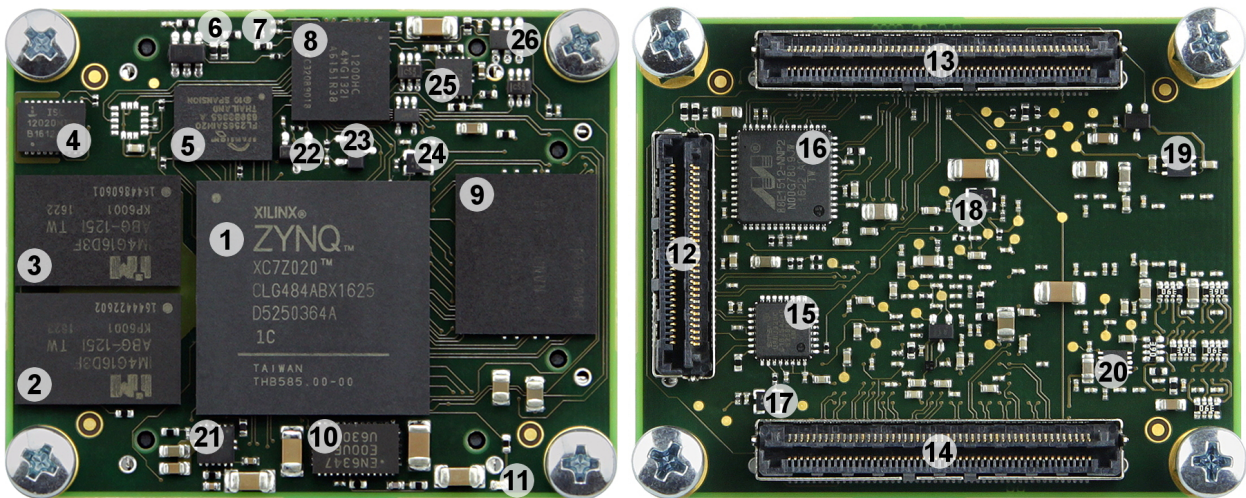
## 2.2 Block Diagram



**Figure 1:** TE0720-03 block diagram.

Components and connections marked with dashed lines are optional or may be missing on some module variants, please contact us for additional information.

## 2.3 Main Components



**Figure 2:** Main components of the module.

1. Xilinx Zynq XC7Z SoC, U5
2. 4 Gbit DDR3/L SDRAM, U13
3. 4 Gbit DDR3/L SDRAM, U12
4. Low-power RTC with battery backed SRAM, U20
5. 32 MByte Quad SPI Flash memory, U7
6. Red LED (LED1), D5
7. Green LED (LED2), D2
8. System Controller CPLD, U19
9. eMMC NAND Flash, U15
10. 4A high-efficiency PowerSoC DC-DC step-down converter (1V), U1
11. Green LED (DONE), D4
12. B2B connector Samtec Razor Beam™ LSHM-130, JM3
13. B2B connector Samtec Razor Beam™ LSHM-150, JM1
14. B2B connector Samtec Razor Beam™ LSHM-150, JM2
15. Hi-speed USB 2.0 ULPI transceiver, U18
16. Gigabit Ethernet (GbE) transceiver, U8
17. Low-power programmable oscillator @ 52.000000 MHz (OTG-RCLK), U14
18. Low-power programmable oscillator @ 33.333333 MHz (PS-CLK), U6
19. Low-dropout regulator (VBATT), U24
20. DDR termination regulator, U4
21. 1.5A PowerSoC DC-DC step-down converter with integrated inductor (1.5V), U2
22. Atmel CryptoAuthentication chip, U10
23. 2Kbit UNI/O® serial EEPROM with EUI-48™ node identity, U17
24. Low-power programmable oscillator @ 25.000000 MHz (ETH-CLK), U9
25. 1.5A PowerSoC DC-DC step-down converter with integrated inductor (1.8V), U3
26. 3A PFET load switch with configurable slew rate (3.3V), Q1

## 2.4 Initial Delivery State

Storage device name	IC	Content	Notes
Quad SPI Flash	U 7	Empty	-
eMMC NAND Flash	U 15	Empty	-
11AA02E48T EEPROM	U 17	Pre-programmed globally unique, 48-bit node address (MAC)	-
System Controller CPLD	U 19	Standard firmware.	<a href="#">Download firmware</a>

**Table 1:** Initial state of programmable devices on delivery of the module.

## 4 Signals, Interfaces and Pins

### 4.1 Board to Board (B2B) I/Os

PL I/O signal connections between Zynq SoC's I/O banks and B2B connectors, 152 HR GPIOs total.

Bank	Type	Voltage	B2B	I/O Count	Notes
13	HR GPIO	VCCIO13	JM2	48	24 LVDS pairs
13	HR GPIO	VCCIO13	JM2	2	B13_IO0 and B13_IO25
33	HR GPIO	VCCIO33	JM2	18	9 LVDS pairs
34	HR GPIO	VCCIO34	JM3	36	18 LVDS pairs
35	HR GPIO	VCCIO35	JM1	48	24 LVDS pairs

**Table 2:** General PL I/O to B2B connectors information.

PS MIO bank 500 and 501 signal connections to B2B JM1 connector, 14 PS MIOs total.

MIO	B2B Pin	Bank	Voltage	Notes
0	JM1-87	500	3.3V	
9	JM1-91	500	3.3V	
10	JM1-95	500	3.3V	
11	JM1-93	500	3.3V	
12	JM1-99	500	3.3V	
13	JM1-97	500	3.3V	
14	JM1-92	500	3.3V	Also wired to U19-M4
15	JM1-85	500	3.3V	Also wired to U19-N4
40	JM1-27	501	1.8V	Zynq SoC SD0
41	JM1-25	501	1.8V	Zynq SoC SD0
42	JM1-23	501	1.8V	Zynq SoC SD0
43	JM1-21	501	1.8V	Zynq SoC SD0



44	JM1-19	501	1.8V	Zynq SoC SD0
45	JM1-17	501	1.8V	Zynq SoC SD0

**Table 3:** General PS MIO connections information.


For detailed information about the pin-out, please refer to the [Pin-out tables](#).

## 4.2 JTAG Interface

JTAG access to the Zynq SoC and System Controller CPLD is provided through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

**Table 4:** JTAG pins connection.

 JTAGMODE pin 89 in B2B connector JM1 is used to switch access between devices, low selects Zynq SoC, high selects System Controller CPLD.

## 4.3 System Controller CPLD I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
RESIN	Input	Reset input	Active low reset input, default mapping forces POR_B reset to Zynq PS.
PGOOD	Output	Power good	Active high when all on-module power supplies are working properly.
MODE	Input	Boot mode	Force low for boot from the SD card. Latched at power-on only, not during soft reset!

48	MMC-CLK	W6
49	MMC-D1	H4
50	MMC-D2	H5
51	MMC-D3	J2

**Table 7:** eMMC interface MIOs and pins.

## 4.6 Ethernet Interface

The Marvell Alaska 88E1512 (U8) is a physical layer device containing a single Gigabit Ethernet transceiver and three separate major electrical interfaces: MDI interface to copper cable, SERDES/SGMII interface and RGMII interface. RGMII interface is connected to the Zynq SoC PS bank 501 MIO pins, see tables below.

SGMII (SFP copper or fiber) pins are routed to the B2B connector JM3 and MDI pins are routed to the B2B connector JM1 (see table below).

### Ethernet PHY to B2B connections

PHY Signal	B2B Pin		PHY Signal	B2B Pin
SOUT_N	JM3-1		PHY_MDI1_P	JM1-10
SOUT_P	JM3-3		PHY_MDI1_N	JM1-12
SIN_N	JM3-2		PHY_MDI2_P	JM1-16
SIN_P	JM3-4		PHY_MDI2_N	JM1-18
PHY_MDI0_P	JM1-4		PHY_MDI3_P	JM1-22
PHY_MDI0_N	JM1-6		PHY_MDI3_N	JM1-24

**Table 8:** Ethernet PHY to B2B connections.

### Ethernet PHY to Zynq SoC PS MIO ETH0 connections

PHY Signal	SoC MIO		PHY Signal	SoC MIO
ETH-TXCK	16		ETH-RXCK	22
ETH-TXD0	17		ETH-RXD0	23
ETH-TXD1	18		ETH-RXD1	24
ETH-TXD2	19		ETH-RXD2	25

USB PHY Pin	SC CPLD Pin	B2B Name	Notes
REFSEL0..2	-	-	Reference clock frequency select, all set to GND = 52.000000 MHz.
RESETB	B14, bank 1	-	Active low reset.
CLKOUT	-	-	ULPI output clock connected to Zynq PS MIO36.
DP, DM		OTG-D_P, OTG-D_N	USB data lines.
CPEN		VBUS_V_EN	External USB power switch active high enable signal.
VBUS	-	USB-VBUS	Connect to USB VBUS via a series of resistors, see reference schematic.
ID	-	OTG-ID	For A-device connect to the ground, for B-device leave floating.
SPK_L	M5, bank 2	-	In USB audio mode a switch connects the DM pin to the SPK_L.
SPK_R	M8, bank 2	-	In USB audio mode a switch connects the DP pin to the SPK_R.

**Table 11:** USB ULPI PHY connections.

## 4.8 I2C Interface

On-board I<sup>2</sup>C devices are connected to the System Controller CPLD which acts as a I<sup>2</sup>C bus repeater for the Zynq SoC. System Controller CPLD signals X1, X3 and X7 are routed to Zynq SoC bank 34. Exact functionality depends on the System Controller CPLD firmware.

Signal Name	SC CPLD Pin	SoC Pin	Notes
X1	F1	L16	SCL, I2C clock.
X5	J1	P22	SDA, I2C data out.
X7	M1	N22	SDA, I2C data in.

**Table 12:** Zynq SoC to System Controller CPLD I<sup>2</sup>C bus.

I <sup>2</sup> C Device	I <sup>2</sup> C Address	IC	Notes
ISL12020M RTC	0x6F	U20	RTC registers.
ISL12020M SRAM	0x57	U20	Battery backed RAM in RTC IC.
LSM303D	0x1D	U22	Optional, not soldered on current production variants.

**Table 13:** I<sup>2</sup>C slave device addresses.

## 5.5 Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 IC (U8). The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signalling. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK\_125MHZ is connected to the pin G13 of the System Controller CPLD chip (U19).

PHY Signal	SC CPLD Pin
ETH-MDC	L14
ETH-MDIO	K14
PHY_LED0	F14
PHY_LED1	D12
PHY_LED2	C13
PHY_CONFIG	C14
ETH-RST	E14
CLK_125MHZ	G13

**Table 15:** Ethernet PHY to SC CPLD connections.

## 5.6 High-speed USB ULPI PHY

Hi-speed USB ULPI PHY is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO28..39, bank 501 (see also section. The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U14).

## 5.7 RTC - Real Time Clock

Temperature compensated Intersil ISL12020M IC is used for Real Time Clock (U20). Battery voltage must be supplied to the module VBAT\_IN pin from the carrier board to use battery backed functionality. Battery backed registers can be accessed over I<sup>2</sup>C bus at slave address of 0x6F. General purpose RAM is at I<sup>2</sup>C slave address 0x57. RTC IC is supported by Linux so it can be used as *hwclock* device.

## 5.8 MAC-Address EEPROM

A Microchip 2Kbit 11AA02E48 serial EEPROM (U17) is connected to the System Controller CPLD pin M14 via single-I/O UNI/O serial interface and contains pre-programmed globally unique 48-bit node address compatible with EUI-48™ specification. Chip is programmed at the factory with a globally unique node address stored in the upper 1/4 of the memory array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

## 5.9 Atmel CryptoAuthentication Chip

The ATSHA204A Atmel CryptoAuthentication™ chip (U10) is connected to the System Controller CPLD pin N14 via single-wire interface providing various security functions and features such as anti-counterfeiting, firmware/media protection, password validation, secure session key exchanging, secure data storage and more. Refer to the product datasheet for more information.

## 5.10 eCompass module

Optionally TE0720 module can be fitted with ultra-compact high-performance eCompass device (LSM303D, U22) featuring 3D accelerometer and 3D magnetometer.

## 5.11 Oscillators

Source	Signal	Frequency	Destination	Pin Name	Notes
U6	PS-CLK	33.333333 MHz	U5	PS_CLK_500	Zynq SoC PS subsystem main clock.
U14	OTG-RCLK	52.000000 MHz	U18	REFCLK	USB3320C PHY reference clock.
U9	ETH-CLK	25.000000 MHz	U8	XTAL_IN	88E1512 PHY reference clock.

**Table 16:** Oscillators.

## 5.12 On-board LEDs

LED	Color	Connected to	Description and Notes
D2	Green	LED1	Controlled by System Controller CPLD firmware.
D4	Green	DONE	
D5	Red	LED2	Controlled by System Controller CPLD firmware.

**Table 17:** On-board LEDs.

## 6 Power and Power-On Sequence

### 6.1 Power Supply

Power supply with minimum current capability of 3A for system startup is recommended.

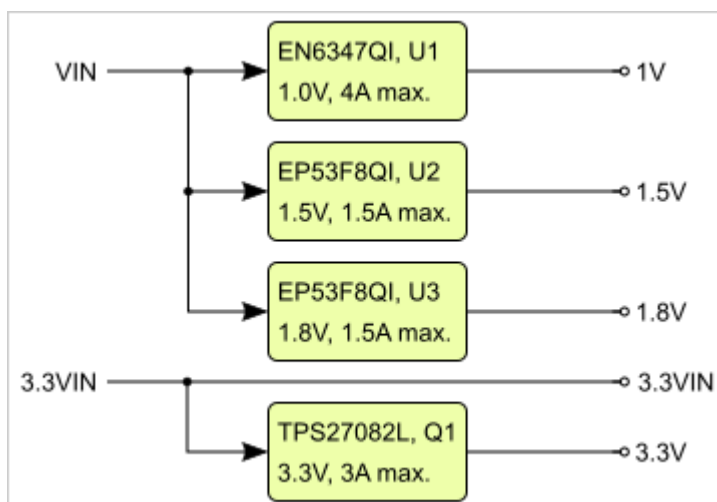
#### Power Consumption

Power Input Pin	Typical Current
VIN	TBD*
3.3VIN	TBD*

**Table 18:** Power Consumption.

\* TBD - To Be Determined.

#### Power Distribution Diagram



**Figure 3:** Power distribution diagram.

**⚠** Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

### 6.2 Power-On Sequence

For highest efficiency of the on-board DC-DC regulators, it is recommended to use single 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.



3.3VIN	13, 15	91	Input	Supply voltage from carrier board. JM2-91 is VREF_JTAG.
VCCIO3 5	9, 11	-	Input	High range bank voltage from carrier board.
VCCIO3 3	-	5	Input	High range bank voltage from carrier board.
VCCIO1 3	-	7, 9	Input	High range bank voltage from carrier board.
VCCIO3 4	-	1, 3	Input	High range bank voltage from carrier board.
VBAT_I N	79	-	Input	RTC battery-buffer supply voltage.
3.3V	-	10, 12	Output	Internal 3.3V voltage level.
1.8V	39	-	Output	Internal 1.8V voltage level.
1.5V <sup>1)</sup>	-	19	Output	Internal 1.5V voltage level.

**Table 19:** Module power rails.

<sup>1)</sup> In case of module variant of TE0720-03-L1IF which uses Xilinx Zynq XC7Z020-L1CLG484I chip with lower power consumption, power rails named 1.5V and VCCO\_DDR\_502 voltage is actually 1.35V. To achieve this, a resistor with different value is used for R4 (see schematic of the TE0720-03-L1IF for more information).

## 6.4 Bank Voltages

Bank	Schematic Name	Voltage	Notes
500	3.3V, VCCO_MIO0_500	3.3V	
501	1.8V, VCCO_MIO1_501	1.8V	
502	1.5V, VCCO_DDR_502	1.5V	
0 Config	3.3V	3.3V	

## 7 Board to Board Connectors

⚠ These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three [Samtec Razor Beam LSHM connectors](#) on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

### 7.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Connector on baseboard	compatible to	Mating height
REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

The module can be manufactured using other connectors upon request.

### 7.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps

12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

### 7.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

### 7.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

### 7.5 Manufacturer Documentation

#### **Geändert**

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

---

07 04, 2016 by Thorsten Trenz

## 8 Variants Currently in Production

Module Variant	Zynq SoC	RAM	eMMC Size	Temperature Range	B2B Connector Height
<b>TE0720-03-2IF</b>	XC7Z020-2CLG484I	1 GByte	4 GByte	Industrial	4.0 mm
<b>TE0720-03-2IF C3</b>	XC7Z020-2CLG484I	1 GByte	4 GByte	Industrial	2.5 mm
<b>TE0720-03-2IF C8</b>	XC7Z020-2CLG484I	1 GByte	32 GByte	Industrial	4.0 mm
<b>TE0720-03-L1IF</b>	XC7Z020-L1CLG484I	512 MByte	4 GByte	Industrial	4.0 mm
<b>TE0720-03-1CF</b>	XC7Z020-1CLG484C	1 GByte	4 GByte	Commercial	4.0 mm
<b>TE0720-03-1CR</b>	XC7Z020-1CLG484C	256 MByte	-	Commercial	4.0 mm
<b>TE0720-03-14S-1C</b>	XC7Z014S-1CLG484C	1 GByte	4 GByte	Commercial	4.0 mm
<b>TE0720-03-1QF</b>	XA7Z020-1CLG484Q	1 GByte	4 GByte	Automotive	4.0 mm

**Table 21:** Module variants currently in production.

## 10 Revision History


### 10.1 Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2015-10-12	03			<a href="#">TE0720-03</a>
-	02			<a href="#">TE0720-02</a>
-	01	Prototypes		

**Table 24:** Hardware revision history table.

There is no hardware revision number marking on the module PCB.

### 10.2 Document Change History

Date	Revision	Contributors	Description
 2017-11-10	v.85	John Hartfiel	<ul style="list-style-type: none"> <li>• Replace B2B connector section</li> </ul>
2017-09-07	v . 84	John Hartfiel	<ul style="list-style-type: none"> <li>• Correction of Boot Mode section</li> </ul>
2017-08-31	v . 83	Jan Kumann	<ul style="list-style-type: none"> <li>• Initial document.</li> </ul>

**Table 25:** Document change history table.