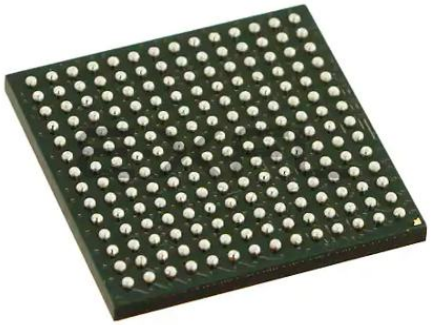

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M210
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	104
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mmc2114cfcvm33

Product Brief

MMC2114PB/D
Rev. 0, 6/2002

MMC2114 M•CORE Microcontroller Product Brief (also addresses MMC2113)

Freescale Semiconductor, Inc.

This document is an overview of the 32-bit MMC2114 and MMC2113 M•CORE microcontrollers, focusing on their highly integrated and diverse feature set. It includes general and detailed descriptions of features and of the various modules incorporated in these devices, and lists packaging, tools, and ordering information for the family.

The MMC2114 and MMC2113 are members of a family of general-purpose microcontroller units (MCU) based on the M•CORE M210 central processor unit (CPU). The M•CORE M210 CPU architecture is one of the most compact, full 32-bit core implementations available. The pipelined reduced instruction set computer (RISC) execution unit uses 16-bit instructions to achieve maximum speed and code efficiency, while conserving on-chip memory resources. The instruction set is designed to support high-level language implementation. A non-intrusive resident debugging system supports product development and in-situ testing.

Unless otherwise noted, all references to MMC2114 also apply to the MMC2113.

The main features of the M•CORE M210 CPU architecture are:

- 32-bit load/store RISC architecture
- Fixed 16-bit instruction length
- 13 32-bit control register file
- 32 32-bit general-purpose register file
- Availability of alternate file set of 32 32-bit general purpose registers
- Efficient 4-stage execution pipeline
- Single-cycle execution for most instructions, 2-cycle branches and memory accesses
- Support for byte/half-word/word memory access
- Support for both normal and fast interrupts
- Vectored and autovectored interrupt support
- On-chip emulation support (OnCE)
- Full static design for minimal power consumption

The M•CORE CPU also benefits applications requiring low power consumption. Total system power consumption is determined by all the system components, rather than the CPU alone. In particular, memory power consumption (both on-chip and external) is a dominant factor in total power consumption of the CPU plus memory subsystem. With this in mind, the CPU instruction set architecture trades absolute performance capability for reduced total energy consumption. This is accomplished while maintaining a high level of performance at a given clock frequency.

1.1 Features Overview

The MMC2114 and MMC2113 are the next devices in a family of devices that began with the MMC2107. The devices in this family are highly integrated with on-chip modules and include the following features:

- M•CORE M210 integer processor
- 256 Kbytes (MMC2114) or 128 Kbytes (MMC2113) FLASH memory
- 32 Kbytes (MMC2114) or 8 Kbytes (MMC2113) of static random-access memory (SRAM)
- Serial peripheral interface (SPI)
- Two serial communications interfaces (SCI)
- Two timers
- Queued analog-to-digital converter (QADC)
- 43-source interrupt controller with support for 8 external interrupt pins
- Two periodic interval timers
- Watchdog timer
- Phase-locked loop (PLL)
- Integrated low-voltage detector (LVD)
- General-purpose input/output (GPIO)
- Multiple chip configurations including single-chip or expanded mode operation
- 7 sources of reset
- External bus interface supporting multiple data widths
- OnCE/Joint Test Action Group (JTAG) support for debug and system-level board testing

The 32-bit MMC2114, with its microRISC central processing unit, delivers 31 Dhrystone 2.1 MIPS performance at 33 MHz.

Figure 1 shows a block diagram of the main modules on the MMC2114.

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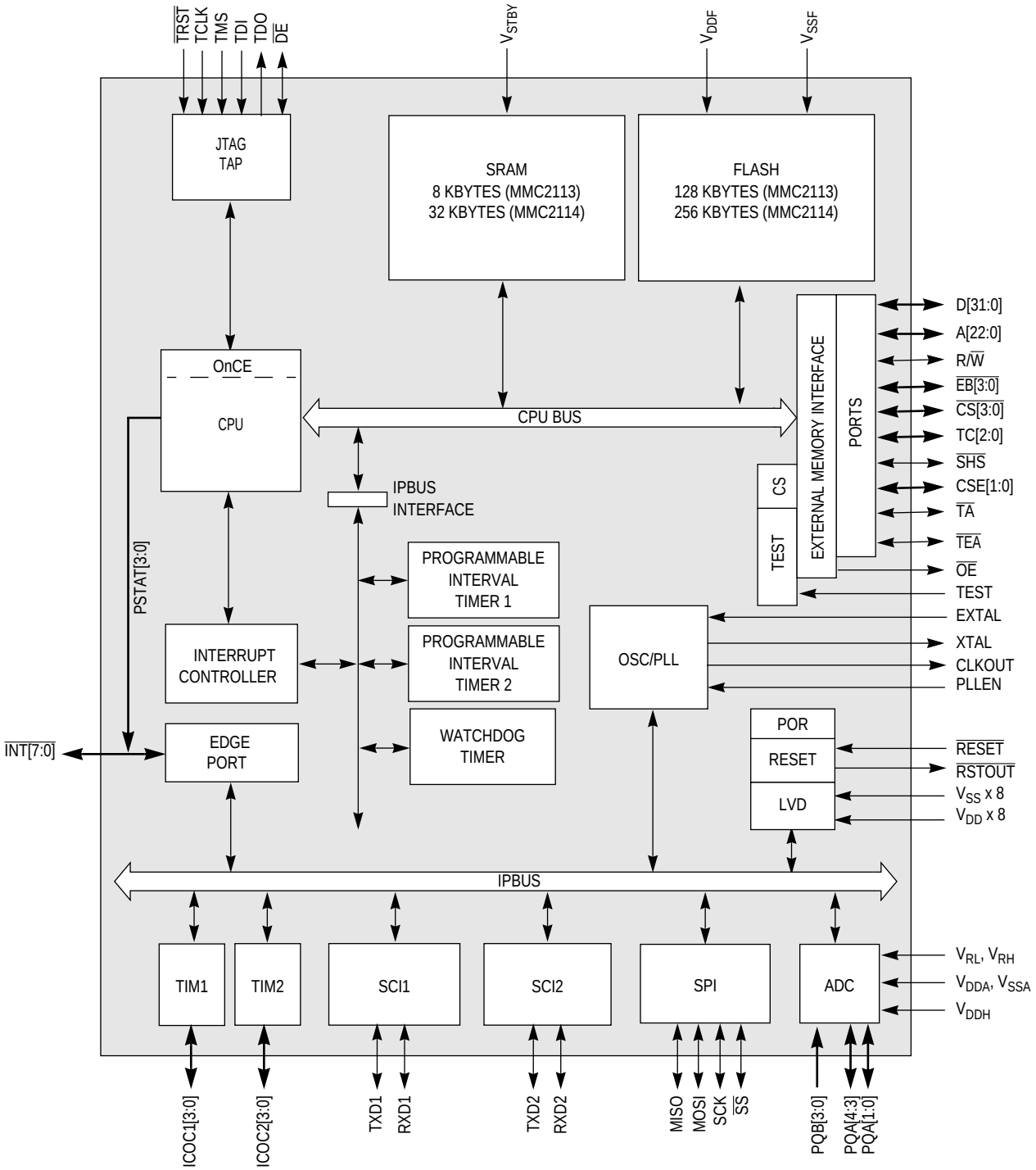

Figure 1. MMC2114 Block Diagram

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1.2 Enhancements over the MMC2107

Several important enhancements have been incorporated into the MMC2114 from its predecessor, the MMC2107. These enhancements are as follows:

- **Improved type of FLASH**. The MMC2114 uses Second Generation FLASH for M•CORE (SGFM), which has five distinct advantages over the MMC2107's CDR MoneT FLASH (CMFR) technology.
  - No externally applied programming voltage
  - Simpler programming and erasing algorithms and shorter programming time
  - A sophisticated security mechanism
  - A three-way code protection scheme
  - Higher endurance
- **More FLASH.** The MMC2114 has twice as much FLASH as that found in the MMC2107 (the MMC2113 has the same amount of FLASH as the MMC2107 at 128 Kbytes), and allows execution of code in one array to program the other array.
- **More static random-access memory (SRAM)**. The MMC2114 has four times the amount of MMC2107 (the MMC2113 has the same amount at 8 Kbytes).
- **LVD circuit.** The MMC2114 offer a low-voltage detection (LVD) monitor, which, upon the sensing of a low-voltage V_{DD} state, allows the central processor unit (CPU) to either cause an interrupt from normal program flow and take appropriate action, or reset the device.
- **5V-tolerant inputs.** The digital input/output (I/O) ports on the MMC2114 have been made more flexible by allowing up to 5 volts to be applied to all pins configured as inputs without danger of damage to the port or to the device.
- **New package.** Along with the 100-pin and 144-pin low-profile quad flat pack (LQFP) packages offered for the MMC2107, the MMC2114 is also offered in a very compact 196-ball plastic mold array process ball grid array (MAPBGA). This package has the same pinout features as those in the 144-pin LQFP.

1.3 Feature List

The following lists the major features of the MMC2114 and MMC2113:

- M•CORE M210 integer processor:
  - 32-bit reduced instruction set computer (RISC) architecture
  - Low power and high performance
- OnCE debug support
- 128 Kbytes (MMC2113) or 256 Kbytes (MMC2114) FLASH memory:
  - Single-cycle byte, half-word (16-bit) and word (32-bit) reads
  - Fast automated program and erase procedure with interrupt support
  - Ability to program one FLASH bank while executing from another (MMC2114 only)
  - Flexible protection scheme for accidental program/erase
  - Access restriction controls for both supervisor/user and data/program spaces

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  - Enhanced security feature prevents unauthorized access to contents of FLASH (protects company IP)
  - Single-supply operation (no need for separate, high voltage program/erase supply)
- 8 Kbytes (MMC2113) or 32 Kbytes (MMC2114) of static random-access memory (SRAM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) reads and writes
  - Standby power supply support
- Serial peripheral interface (SPI):
  - Master mode and slave mode with slave select output
  - Serial clock with programmable polarity and phase
  - Control of SPI operation during wait mode
  - Mode fault error flag with CPU interrupt capability
  - Wired-OR mode and reduced drive control
  - General-purpose input/output (I/O) capability
- Two serial communications interfaces (SCI):
  - Full-duplex operation
  - Standard mark/space non-return-to-zero (NRZ) format
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Hardware parity checking
  - Receiver framing error and 1/16 bit-time noise detection
  - Reduced drive control
  - General-purpose I/O capability
- Two timers:
  - Four 16-bit input capture/output compare channels
  - 16-bit pulse accumulator
  - Pulse widths variable from microseconds to seconds
  - Eight selectable timer prescalers
  - Toggle-on-overflow feature for pulse-width modulation
- Queued analog-to-digital converter (QADC):
  - Eight analog input channels
  - 10-bit resolution ±2 counts accuracy
  - Minimum 7 µS conversion time
  - Programmable input sample time for various source impedances
  - Two conversion command queues with a total of 64 entries
  - Subqueues possible using pause mechanism

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  - Queue complete and pause interrupts available on both queues
  - Queue pointers indicate current location for each queue execution
  - Automated queue modes initiated by external trigger or periodic/interval timer
  - Single-scan or continuous-scan of queues
  - Output data readable in three formats
  - Minimum pin set configuration implemented
  - Analog pins configurable as general-purpose I/O
- Interrupt controller:
  - Up to 43 interrupt sources
  - 32 unique programmable priority levels for each interrupt source
  - Independent enable/disable of pending interrupts based on priority level
  - Normal or fast interrupt request for each priority level
  - Maskable interrupts at and below a defined priority level
  - Selectable autovectored or vectored interrupt requests
  - Vectored interrupts generated based on priority level
  - Separate vector number possible for normal and fast interrupts
  - Visibility of pending interrupts and interrupt signals to core
  - Interrupt wakeup from low-power modes
- External interrupts supported:
  - Rising/falling edge or level sensitivity
  - Software generation of external interrupt event
  - Interrupt pins configurable as general-purpose I/O
- Two periodic interval timers:
  - 16-bit counter with modulus "initial count" register
  - Selectable as free running or count down
  - 16 selectable prescalers — 2^0 to 2^{15}
- Watchdog timer:
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Phase-lock loop (PLL):
  - Reference crystal from 2 to 10 MHz
  - Low-power modes supported
  - Separate clock-out signal
- Integrated low-voltage detector (LVD):
  - Enabled and disabled under software control
  - Internal comparator with bandgap reference threshold
  - Selectable reset or interrupt request action
  - Optional automatic disabling in low-power stop mode

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- Reset:
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog timer
    - Loss of clock
    - Loss of PLL lock
    - Low-voltage detect
  - Source of last reset viewable
- Chip configurations:
  - Support for single-chip, master, emulation, and test modes
  - System configuration during reset
  - Configurable clock mode and output pad drive strength control
- General-purpose input/output (GPIO):
  - Up to 104 bits of GPIO
  - Coherent 32-bit control
  - Bit manipulation supported via set/clear functions
- External bus interface:
  - Provides for direct support of asynchronous random-access memory (RAM), read-only memory (ROM), FLASH, and memory mapped peripherals
  - Bidirectional data bus with wide (32-bit) and narrow (16-bit) modes
  - 23-bit address bus with four chip selects provide access to 32 Mbytes of external memory
  - Byte/write enables
  - Boot from on-chip FLASH or external memories
  - Bus monitor
  - Internal bus activity is visible via show-cycle mode
  - Special chip selects support replacement of GPIO with external port replacement logic
- Joint Test Action Group (JTAG) support for system-level board testing

1.4 General Device Information

Available packages are:

- 100-pin low-profile quad flat pack (LQFP) for single-chip mode operation
- 144-pin LQFP for applications requiring an external memory interface or a large number of general-purpose inputs/outputs (GPIO)
- 196-ball plastic mold array process ball grid array (MAPBGA) providing the same functionality as the 144-pin LQFP in a smaller form factor

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Table 1. Package Option Summary

Device	On-Chip SRAM (Kbytes)	On-Chip FLASH (Kbytes)	Packages	Operating Modes [1]
MMC2113	8	128	100 LQFP 144 LQFP 196 MAPBGA	Single chip Master Emulation
MMC2114	32	256		

1 See Section 4.4, “Modes of Operation,” in the *MMC2114 Advance Information* manual for descriptions of the different MCU operating modes.

1.5 Development Tools

Table 2 lists the Motorola/Metrowerks development tools that are available for the MMC2114 and MMC2113. Tools and samples are available from a local Motorola distributor or a Motorola semiconductor sales office.

Table 2. Motorola/Metrowerks Development Tools for the MMC2114

Development Tool ID	Description
MMC2114DDL	MMC2114/MMC2113 Device Driver Library
MMCCMB2114	MMC2114/MMC2113 Controller and Memory Board Development Kit
MMCEVB2114	MMC2114/MMC2113 Evaluation Board Development Kit
MMC14EBDI02	M•CORE 14-Pin Enhanced Background Debug Interface (EBDI)
MMCPFB1200	MMCPFB1200 Platform Board
MMCLAB01	Logic Analyzer Board
KITEVS2114	MMC2114/MMC2113 Evaluation System
SysDS Loader	System Loader and Programmer for CMB/EVB2114 FLASH
OnChip SysDS Loader	Programmer for MMC2114/MMC2113 On-chip FLASH
CodeWarrior for M•CORE 2.0	CodeWarrior Compiler/Linker/Debugger IDE for M•CORE, Version 2.0

1.6 Documentation

Table 3 lists the documents that provide a complete description of the MMC2114 and MMC2113 and related development support tools. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, the Motorola Literature Distribution Center, or through the Motorola world-wide web address at http://www.motorola.com/semiconductors.

Table 3. Related Documentation

Document Name/Number	Description
MMC2114/D	MMC2114/MMC2113 Advance Information User’s Manual
MCORERM/AD	M•CORE Reference Manual
MMC2114DDLRM/D	MMC2114 Device Driver Library Reference Manual
MCOREABISM/AD	M•CORE Applications Binary Interface Standards Manual
MCOREARCHBRF	M•CORE Architectural Brief

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Table 3. Related Documentation (continued)

Document Name/Number	Description
MMCCMB2114UM/D	MMCCMB2114 Controller and Memory Board (CMB2114) User's Manual
MMCEVB2114UM/D	MMCEVB2114 Controller and Memory Board (EVB2114) User's Manual
MMC14EBDIUM/D	M•CORE 14-Pin Enhanced Background Debug Interface (14EBDI) User's Manual
MMCPFB1200UM/D	MMCPFB1200 Platform Board User's Manual
MMCLAB01UM/D	MMCLAB01 Logic Analyzer Board User's Manual

1.7 Ordering Information

Table 4 shows 2003 quantity pricing for the family's various parts and packages. Single quantity samples for each device/package are also available.

Table 4. Orderable Parts

Part Number	Features	Package	Price (10K in 2003)
MMC2107CFCPU33	128K FLASH, 8K SRAM	100-pin 14x14 mm LQFP	$12.07
MMC2107CFCPV33	128K FLASH, 8K SRAM	144-pin 20x20 mm LQFP	$12.07
MMC2113CFCPU33	128K FLASH, 8K SRAM	100-pin 14x14 mm LQFP	$12.74
MMC2113CFCPV33	128K FLASH, 8K SRAM	144-pin 20x20 mm LQFP	$12.74
MMC2113FCVF33	128K FLASH, 8K SRAM	196-pin 15x15 mm MAPBGA	$14.01
MMC2114CFCPU33	256K FLASH, 32K SRAM	100-pin 14x14 mm LQFP	$14.30
MMC2114CFCPV33	256K FLASH, 32K SRAM	144-pin 20x20 mm LQFP	$14.30
MMC2114FCVF33	256K FLASH, 32K SRAM	196-pin 15x15 mm MAPBGA	$15.73

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