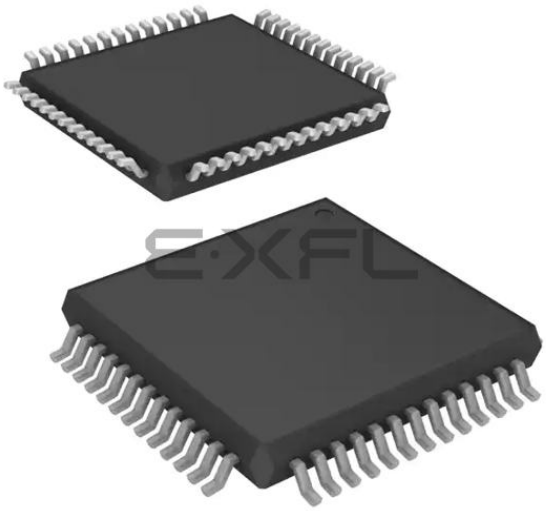

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	80KB (80K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3422evb40t6

Table 2. Pin definitions (continued)

Port pin	Signal name	80-pin No.	52-pin No.(1)	In/out	Function		
					Basic	Alternate 1	Alternate 2
P3.1	TXD0	77	24	I/O	General I/O port pin	UART0 Transmit (TxD0)	
P3.2	EXINT0 TGO	79	25	I/O	General I/O port pin	Interrupt 0 input (EXTINT0)/Timer 0 gate control (TG0)	
P3.3	INT1	2	26	I/O	General I/O port pin	Interrupt 1 input (EXTINT1)/Timer 1 gate control (TG1)	
P3.4	C0	40	27	I/O	General I/O port pin	Counter 0 input (C0)	
P3.5	C1	42	28	I/O	General I/O port pin	Counter 1 input (C1)	
P3.6	SDA	44	29	I/O	General I/O port pin	I^2C bus serial data (I^2CSDA)	
P3.7	SCL	46	30	I/O	General I/O port pin	I^2C bus clock (I^2CSCL)	
P4.0	T2 TCM0	33	22	I/O	General I/O port pin	Program counter array0 PCA0-TCM0	Timer 2 count input (T2)
P4.1	T2X TCM1	31	21	I/O	General I/O port pin	PCA0-TCM1	Timer 2 trigger input (T2X)
P4.2	RXD1 TCM2	30	20	I/O	General I/O port pin	PCA0-TCM2	UART1 or IrDA Receive (RxD1)
P4.3	TXD1 PCACLK0	27	18	I/O	General I/O port pin	PCACLK0	UART1 or IrDA Transmit (TxD1)
P4.4	SPICLK TCM3	25	17	I/O	General I/O port pin	Program counter Array1 PCA1-TCM3	SPI clock out (SPICLK)
P4.5	SPIRXD TCM4	23	16	I/O	General I/O port pin	PCA1-TCM4	SPI Receive (SPIRxD)
P4.6	SPITXD	19	15	I/O	General I/O port pin	PCA1-TCM5	SPI Transmit (SPITxD)
P4.7	SPISEL PCACLK1	18	14	I/O	General I/O port pin	PCACLK1	SPI Slave Select (SPISEL)
AV_{REF}		70	N/A	I	Reference Voltage input for ADC. Connect AV_{REF} to V_{CC} if the ADC is not used.		
RD		65	N/A	O	READ signal, external bus		
WR		62	N/A	O	WRITE signal, external bus		
PSEN		63	N/A	O	PSEN signal, external bus		

4 Memory organization

The 8032 MCU core views memory on the MCU module as “internal” memory and it views memory on the PSD module as “external” memory, see *Figure 5*

Internal memory on the MCU module consists of DATA, IDATA, and SFRs. These standard 8032 memories reside in 384 bytes of SRAM located at a fixed address space starting at address 0000h.

External memory on the PSD module consists of four types: main Flash (64 Kbyte, 128 Kbyte, or 256 Kbyte), a smaller secondary Flash (32 Kbyte), SRAM (4 Kbyte, 8 Kbyte or 32 Kbyte), and a block of PSD module control registers called csiop (256 bytes). These external memories reside at programmable address ranges, specified using the software tool PSDsoft Express. See the PSD module section of this document for more details on these memories.

External memory is accessed by the 8032 in two separate 64 Kbyte address spaces. One address space is for program memory and the other address space is for data memory. Program memory is accessed using the 8032 signal, $\overline{PSEN}$. Data memory is accessed using the 8032 signals, $\overline{RD}$ and $\overline{WR}$. If the 8032 needs to access more than 64 Kbytes of external program or data memory, it must use paging (or banking) techniques provided by the page register in the PSD module.

Note: When referencing program and data memory spaces, it has nothing to do with 8032 internal SRAM areas of DATA, IDATA, and SFR on the MCU module. Program and data memory spaces only relate to the external memories on the PSD module.

External memory on the PSD module can overlap the internal SRAM memory on the MCU module in the same physical address range (starting at 0000h) without interference because the 8032 core does not assert the $\overline{RD}$ or $\overline{WR}$ signals when accessing internal SRAM.

Figure 5. UPSD34xx memories

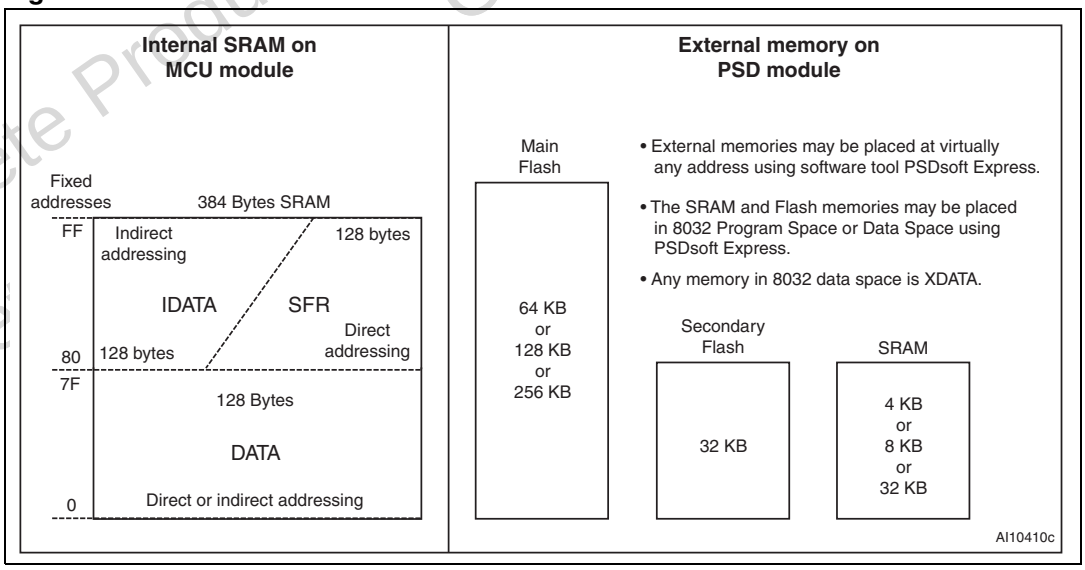
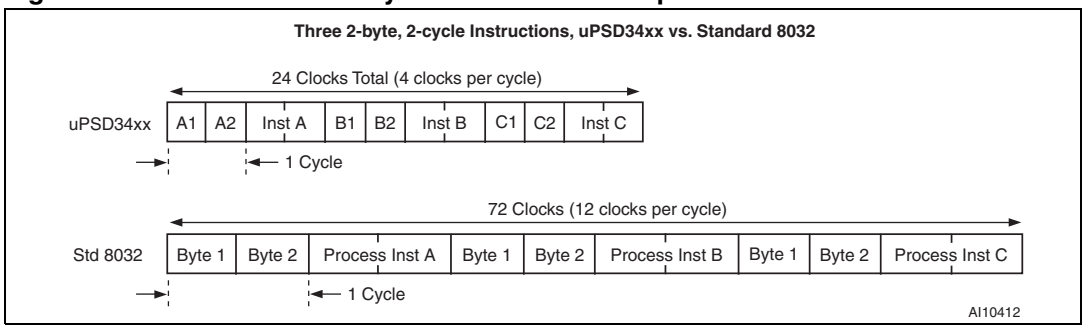


Figure 9. UPSD34xx multi-cycle instructions compared to standard 8032



7.4 Accumulator (ACC)

This is an 8-bit general purpose register which holds a source operand and receives the result of arithmetic operations. The ACC register can also be the source or destination of logic and data movement operations. For MUL and DIV instructions, ACC is combined with the B register to hold 16-bit operands. The ACC is referred to as “A” in the MCU instruction set.

7.5 B register (B)

The B register is a general purpose 8-bit register for temporary data storage and also used as a 16-bit register when concatenated with the ACC register for use with MUL and DIV instructions.

7.6 General purpose registers (R0 - R7)

There are four banks of eight general purpose 8-bit registers (R0 - R7), but only one bank of eight registers is active at any given time depending on the setting in the PSW word (described next). R0 - R7 are generally used to assist in manipulating values and moving data from one memory location to another. These register banks physically reside in the first 32 locations of 8032 internal DATA SRAM, starting at address 00h. At reset, only the first bank of eight registers is active (addresses 00h to 07h), and the stack begins at address 08h.

7.7 Program status word (PSW)

The PSW is an 8-bit register which stores several important bits, or flags, that are set and cleared by many 8032 instructions, reflecting the current state of the MCU core. *Figure 11 on page 40* shows the individual flags.

7.7.1 Carry flag (CY)

This flag is set when the last arithmetic operation that was executed results in a carry (addition) or borrow (subtraction). It is cleared by all other arithmetic operations. The CY flag is also affected by Shift and Rotate Instructions.

7.7.2 Auxiliary carry flag (AC)

This flag is set when the last arithmetic operation that was executed results in a carry into (addition) or borrow from (subtraction) the high-order nibble. It is cleared by all other arithmetic operations.

7.7.3 General purpose flag (F0)

This is a bit-addressable, general-purpose flag for use under software control.

7.7.4 Register bank select flags (RS1, RS0)

These bits select which bank of eight registers is used during R0 - R7 register accesses (see *Table 4*)

CAPCOML4, CAPCOMH4, TCMMODE4, CAPCOML5, CAPCOMH5, TCMMODE5, PWMF0, PMWF1

- SPI interface registers
  SPICLKD, SPISTAT, SPITDR, SPIRDR, SPICON0, SPICON1
- I^2C interface registers
  S1SETUP, S1CON, S1STA, S1DAT, S1ADR
- Analog to digital converter registers
  ACON, ADCPS, ADAT0, ADAT1
- IrDA interface register
  IRDACON
- USB interface registers
  UADDR, UPAIR, WE0-3, UIF0-3, UCTL, USTA, USEL, UCON, USIZE, UBASEH, UBASEL, USCI, USCV

Table 5. SFR memory map with direct address and reset value

SFR addr (hex)	SFR name	Bit name and <bit address>								Reset value (hex)	Reg. descr. with link
		7	6	5	4	3	2	1	0		
80	RESERVED										
81	SP	SP[7:0]								07	*Section 7.1*
82	DPL	DPL[7:0]								00	*Section 7.2*
83	DPH	DPH[7:0]								00	
84	RESERVED										
85	DPTC	–	AT	–	–	–	DPSEL[2:0]			00	*Table 13*
86	DPTM	–	–	–	–	MD1[1:0]		MD0[1:0]		00	*Table 15*
87	PCON	SMOD0	SMOD1	–	POR	RCLK1	TCLK1	PD	IDLE	00	*Table 33*
88(1)	TCON	TF1 <8Fh>	TR1 <8Eh>	TF0 <8Dh>	TR0 <8Ch>	IE1 <8Bh>	IT1 <8Ah>	IE0 <89h>	IT0 <88h>	00	*Table 56*
89	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00	*Table 58*
8A	TL0	TL0[7:0]								00	*Section 20.1*
8B	TL1	TL1[7:0]								00	
8C	TH0	TH0[7:0]								00	
8D	TH1	TH1[7:0]								00	
8E	P1SFS0	P1SFS0[7:0]								00	*Table 43*
8F	P1SFS1	P1SFS1[7:0]								00	*Table 44*
90(1)	P1	P1.7 <97h>	P1.6 <96h>	P1.5 <95h>	P1.4 <94h>	P1.3 <93h>	P1.2 <92h>	P1.1 <91h>	P1.0 <90h>	FF	*Table 35*
91	P3SFS	P3SFS[7:0]								00	*Table 41*
92	P4SFS0	P4SFS0[7:0]								00	*Table 46*
93	P4SFS1	P4SFS1[7:0]								00	*Table 47*

12 Debug unit

The 8032 MCU module supports run-time debugging through the JTAG interface. This same JTAG interface is also used for In-System Programming (ISP) and the physical connections are described in the PSD module section, *Section 28.6.1: JTAG ISP and JTAG debug on page 257*.

Debugging with a serial interface such as JTAG is a non-intrusive way to gain access to the internal state of the 8032 MCU core and various memories. A traditional external hardware emulator cannot be completely effective on the UPSD34xx because of the Pre-Fetch Queue and Branch Cache. The nature of the PFQ and BC hide the visibility of actual program flow through traditional external bus connections, thus requiring on-chip serial debugging instead.

Debugging is supported by Windows PC based software tools used for 8051 code development from 3rd party vendors listed at www.st.com/psm. Debug capabilities include:

- Halt or start MCU execution
- Reset the MCU
- Single step
- 3 match breakpoints
- 1 range breakpoint (inside or outside range)
- Program tracing
- Read or modify MCU core registers, DATA, IDATA, SFR, XDATA, and code
- External debug event pin, input or output

Some key points regarding use of the JTAG debugger.

  - The JTAG debugger can access MCU registers, data memory, and code memory while the MCU is executing at full speed by cycle-stealing. This means “watch windows” may be displayed and periodically updated on the PC during full speed operation. Registers and data content may also be modified during full speed operation.
  - There is no on-chip storage for Program Trace data, but instead this data is scanned from the UPSD34xx through the JTAG channel at run-time to the PC host for processing. As such, full speed program tracing is possible only when the 8032 MCU is operating below approximately one MIPS of performance. Above one MIPS, the program will not run real-time while tracing. One MIPS performance is determined by the combination of choice for MCU clock frequency, and the bit settings in SFR registers BUSCON and CCON0.
  - Breakpoints can optionally halt the MCU, and/or assert the external Debug Event pin.
  - Breakpoint definitions may be qualified with read or write operations, and may also be qualified with an address of code, SFR, DATA, IDATA, or XDATA memories.
  - Three breakpoints will compare an address, but the fourth breakpoint can compare an address and also data content. Additionally, the fouth breakpoint can be logically combined (AND/OR) with any of the other three breakpoints.
  - The Debug Event pin can be configured by the PC host to generate an output pulse for external triggering when a break condition is met. The pin can also be configured as an event input to the breakpoint logic, causing a break on the falling-edge of an external event signal. If not used, the Debug Event pin should be pulled

Table 34. PCON register bit definition (continued)

Bit	Symbol	R/W	Function
1	PD	R,W	Activate Power-down mode 0 = Not in Power-down mode 1 = Enter Power-down mode
0	IDL	R,W	Activate Idle mode 0 = Not in Idle mode 1 = Enter Idle mode

Table 61. T2CON register bit definition (continued)

Bit	Symbol	R/W	Definition
4	TCLK(1)	R,W	UART0 Transmit Clock control. When TCLK = 1, UART0 uses Timer 2 overflow pulses for its transmit clock in Modes 1 and 3. TCLK=0, Timer 1 overflow is used for transmit clock
3	EXEN2	R,W	Timer 2 External Enable. When EXEN2 = 1, capture or reload results when negative edge on pin T2X occurs. EXEN2 = 0 causes Timer 2 to ignore events at pin T2X.
2	TR2	R,W	Timer 2 run control. 1 = Timer/Counter 2 is on, 0 = Timer Counter 2 is off.
1	C/$\overline{T2}$	R,W	Counter or Timer function select. When C/$\overline{T2}$ = 0, function is timer, clocked by internal clock. When C/$\overline{T2}$ = 1, function is counter, clocked by signal sampled on external pin, T2.
0	CP/$\overline{RL2}$	R,W	Capture/Reload. When CP/$\overline{RL2}$ = 1, capture occurs on negative transition at pin T2X if EXEN2 = 1. When CP/$\overline{RL2}$ = 0, auto-reload occurs when Timer 2 overflows, or on negative transition at pin T2X when EXEN2=1. When RCLK = 1 or TCLK = 1, CP/$\overline{RL2}$ is ignored, and Timer 2 is forced to auto-reload upon Timer 2 overflow

Note: 1 The RCLK1 and TCLK1 Bits in the SFR named PCON control UART1, and have the exact same function as RCLK and TCLK.

Table 62. Timer/counter 2 operating modes

Mode	Bits in T2CON SFR				Pin T2X (1)	Remarks	Input clock	
	RCLK or TCLK	CP/$\overline{RL2}$	TR2	EXEN2			Timer, internal	Counter, external (Pin T2, P1.0)
16-bit Auto-reload	0	0	1	0	x	reload [RCAP2H, RCAP2L] to [TH2, TL2] upon overflow (upcounting)	$f_{OSC}/12$	MAX $f_{OSC}/24$
	0	0	1	1	↓	reload [RCAP2H, RCAP2L] to [TH2, TL2] at falling edge on pin T2X		
16-bit capture	0	1	1	0	x	16-bit timer/counter (upcounting)	$f_{OSC}/12$	MAX $f_{OSC}/24$
	0	1	1	1	↓	Capture [TH2, TL2] and store to [RCAP2H, RCAP2L] at falling edge on pin T2X		

Table 139. ACON register bit definition (continued)

Bit	Symbol	Function
1	ADST	ADC start bit 0 = Force to zero 1 = Start ADC, then after one cycle, the bit is cleared to '0.'
0	ADSF	ADC Status Bit 0 = ADC conversion is not completed 1 = ADC conversion is completed. The bit can also be cleared with software.

Table 140. ADCPS register details (SFR 94h, Reset Value 00h)

Bit	Symbol	Function
7:4	–	Reserved
3	ADCCE	ADC conversion reference clock enable 0 = ADC reference clock is disabled (default) 1 = ADC reference clock is enabled
2:0	ADCPS[2:0]	ADC reference clock prescaler Only three Prescaler values are allowed: ADCPS[2:0] = 0, for f_{OSC} frequency 16MHz or less. Resulting ADC clock is f_{OSC}. ADCPS[2:0] = 1, for f_{OSC} frequency 32MHz or less. Resulting ADC clock is $f_{OSC}/2$. ADCPS[2:0] = 2, for f_{OSC} frequency 32MHz > 40MHz. Resulting ADC clock is $f_{OSC}/4$.

Table 141. ADAT0 register (SFR 95h, reset value 00h)

Bit	Symbol	Function
7:0	–	Store ADC output, Bit 7 - 0

Table 142. ADAT1 register (SFR 96h, reset value 00h)

Bit	Symbol	Function
7:2	–	Reserved
1.. 0	–	Store ADC output, Bit 9, 8

Table 143. PCA0 and PCA1 registers

SFR address		Register name		RW	Register function
PCA0	PCA1	PCA0	PCA1		
A2	BA	PCACL0	PCACL1	RW	The low 8 bits of PCA 16-bit counter.
A3	BB	PCACH0	PCACH1	RW	The high 8 bits of PCA 16-bit counter.
A4	BC	PCACON0	PCACON1	RW	Control register – Enable PCA, Timer Overflow flag , PCA Idle Mode, and Select clock source.
A5	A5	PCASTA	N/A	RW	Status register, Interrupt Status flags – Common for both PCA Block 0 and 1.
A9, AA, AB	BD, BE, BF	TCMMODE0 TCMMODE1 TCMMODE2	TCMMODE3 TCMMODE4 TCMMODE5	RW	TCM Mode – Capture, Compare, and Toggle Enable Interrupts – PWM Mode Select.
AC AD	C1 C2	CAPCOML0 CAPCOMH0	CAPCOML3 CAPCOMH3	RW	Capture/Compare registers of TCM0
AF B1	C3 C4	CAPCOML1 CAPCOMH1	CAPCOML4 CAPCOMH4	RW	Capture/Compare registers of TCM1
B2 B3	C5 C6	CAPCOML2 CAPCOMH2	CAPCOML5 CAPCOMH5	RW	Capture/Compare registers of TCM2
B4	C7	PWMF0	PWMF1	RW	The 8-bit register to program the PWM frequency. This register is used for programmable, 8-bit PWM Mode only.
FB	FC	CCON2	CCON3	RW	Specify the pre-scaler value of PCA0 or PCA1 clock input

27.2 PCA clock selection

- The clock input to the 16-bit up counter in the PCA block is user-programmable. The three clock sources are:
- PCA Prescaler Clock (PCA0CLK, PCA1CLK)
- Timer 0 Overflow
- External Clock, Pin P4.3 or P4.7

The clock source is selected in the configuration register PCACON. The Prescaler output clock PCACLK is the f_{OSC} divided by the divisor which is specified in the CCON2 or CCON3 register. When External Clock is selected, the maximum clock frequency should not exceed $f_{OSC}/4$.

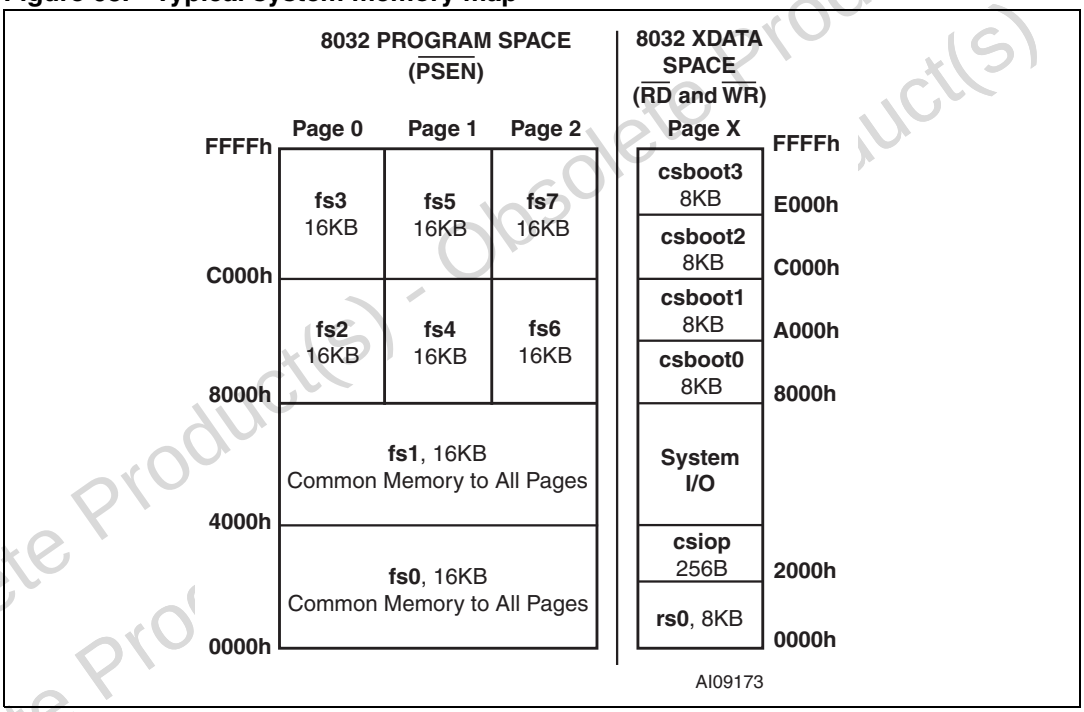
28.2.1 8032 program address space

In the example of *Figure 63*, six sectors of Main Flash memory (fs2.. fs7) are paged across three memory pages in the upper half of program address space, and the remaining two sectors of Main Flash memory (fs0, fs1) reside in the lower half of program address space, and these two sectors are independent of paging (they reside in “common” program address space). This paged memory example is quite common and supported by many 8051 software compilers.

28.2.2 8032 data address space (XDATA)

Four sectors of Secondary Flash memory reside in the upper half of 8032 XDATA space in the example of *Figure 63*. SRAM and csiop registers are in the lower half of XDATA space. The 8032 SFR registers and local SRAM inside the 8032 MCU module do not reside in XDATA space, so it is OK to place PSD module SRAM or csiop registers at an address that overlaps the address of internal 8032 MCU module SRAM and registers.

Figure 63. Typical system memory map

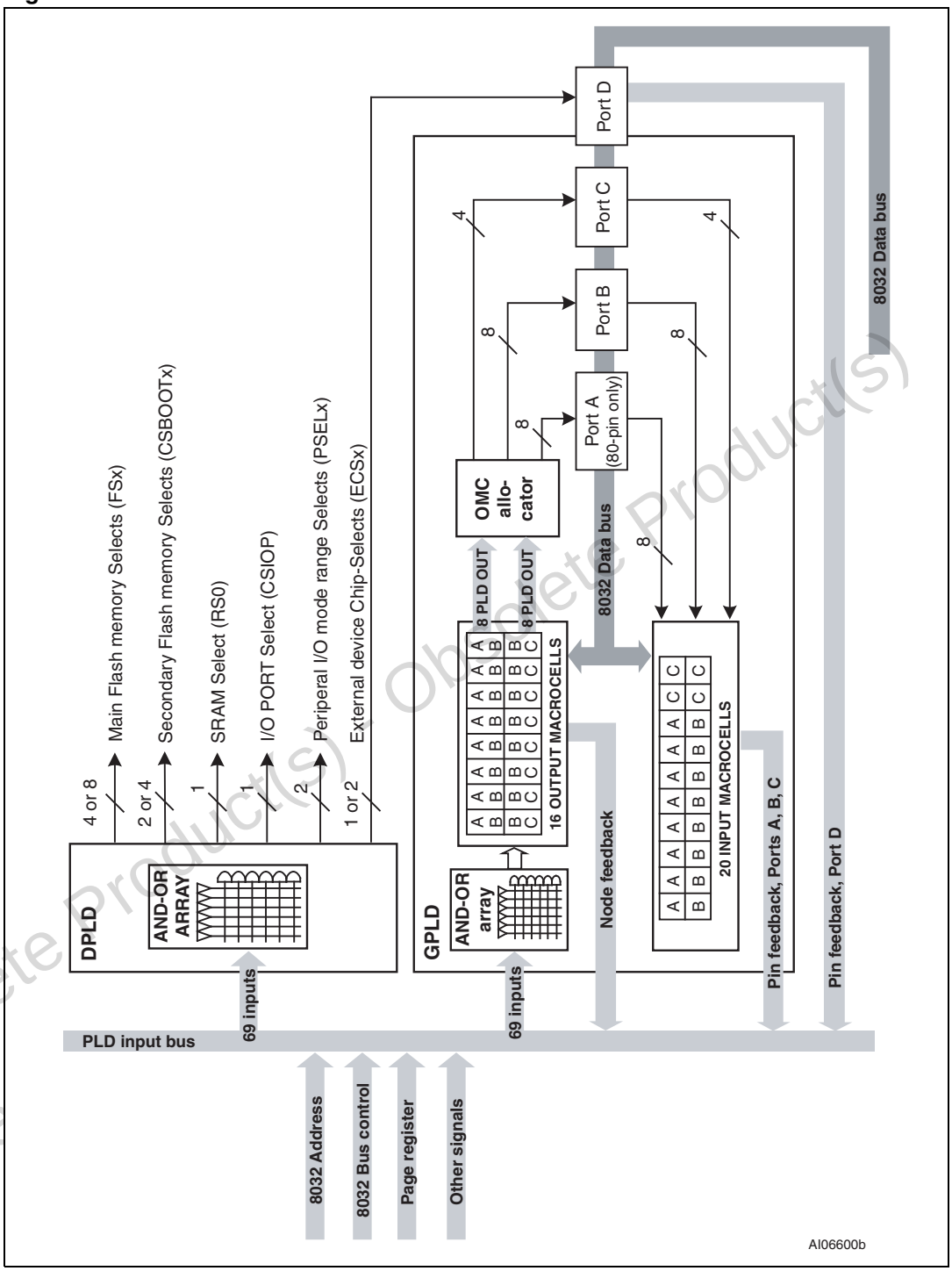


28.2.3 Specifying the memory map with PSDsoft express

The memory map example shown in *Figure 63 on page 198* is implemented using PSDsoft Express in a point-and-click environment. PSDsoft Express will automatically generate Hardware Definition Language (HDL) statements of the ABEL language for the DPLD, such as those shown in *Table 159*.

Specifying these equations using PSDsoft Express is very simple. For example, *Figure 64*, page 84 shows how to specify the chip-select equation for the 16 Kbyte Flash memory segment, fs4. Notice fs4 is on memory page 1. This specification process is repeated for all other Flash memory segments, the SRAM, the csiop register block, and any external chip select signals that may be needed.

Figure 73. DPLD and GPLD



mode, making the pin suitable for input mode (read by the input buffer shown in *Figure 79 on page 232*). *Figure 79* shows the three sources that can control the pin output enable signal: a product term from AND-OR array; the csiop Direction register; or the Peripheral I/O Mode logic (Port A only). The csiop Enable Out registers represent the state of the final output enable signal for each port pin driver, and are defined in *Table 196 on page 242* through *Table 199 on page 242*.

Table 192. Port A pin drive select register(1) (2) (3)(address = csiop + offset 08h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 open drain	PA6 open drain	PA5 open drain	PA4 open drain	PA3 slew rate	PA2 slew rate	PA1 slew rate	PA0 slew rate

1. Port A not available on 52-pin UPSD34xx devices.
2. For each bit, 1 = pin drive type is selected, 0 = pin drive type is default mode, CMOS push/pull.
3. Default state for register is 00h after reset or power-up.

assembly code example in *Table* , the PFQ will be loaded with the final instructions to command the MCU module to Power Down mode after the PDS Module goes to Power-Down mode. In this case, even though the code memory goes off-line in the PSD module, the last few MCU instruction are sourced from the PFQ.

Forced power-down example

```
PDOWN:  ANL   A8h, #7Fh      ; disable all interrupts
        ORL   9Dh, #C0h      ; ensure PFQ and BC are enabled
        MOV   DPTR, #xxC7    ; load XDATA pointer to select PMMR3 register (xx = base
                             ; address of csiop registers)
        CLR   A              ; clear A
        JMP   LOOP           ; first loop - fill PFQ/BQ with Power Down instructions
        NOP                  ; second loop - fetch code from PFQ/BC and set Power-
                             ; Down bits for PSD module and then MCU module
LOOP:   MOVX  @DPTR, A       ; set FORCE_PD Bit in PMMR3 in PSD module in second
                             ; loop
        MOV   87h, A         ; set PD Bit in PCON register in MCU module in second
                             ; loop
        MOV   A, #02h        ; set power-down bit in the A register, but not in PMMR3 or
                             ; PCON yet in first loop
        JMP   LOOP           ; uPSD enters into Power-Down mode in second loop
```

Figure 88. Automatic power-down (APD) unit

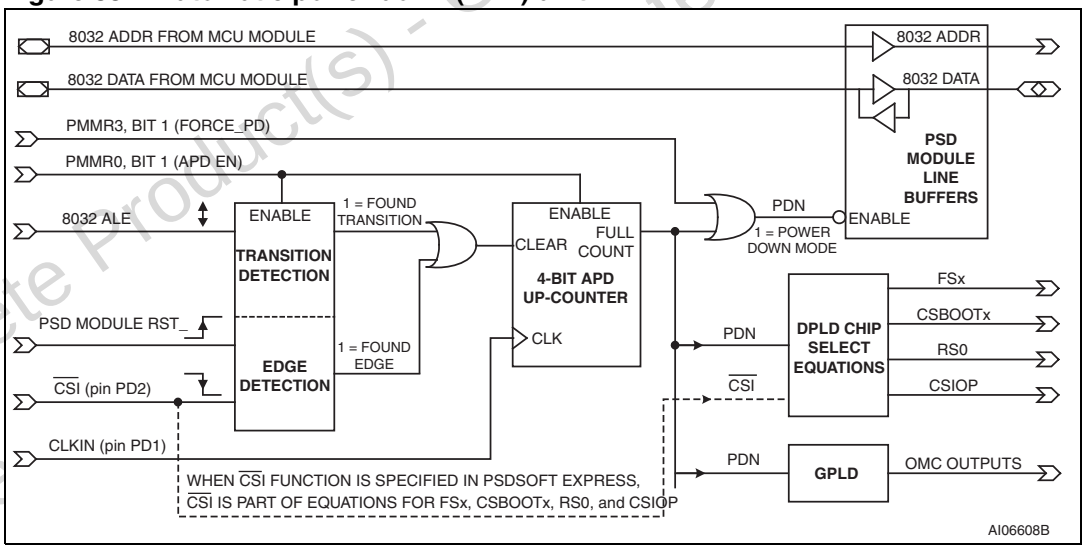
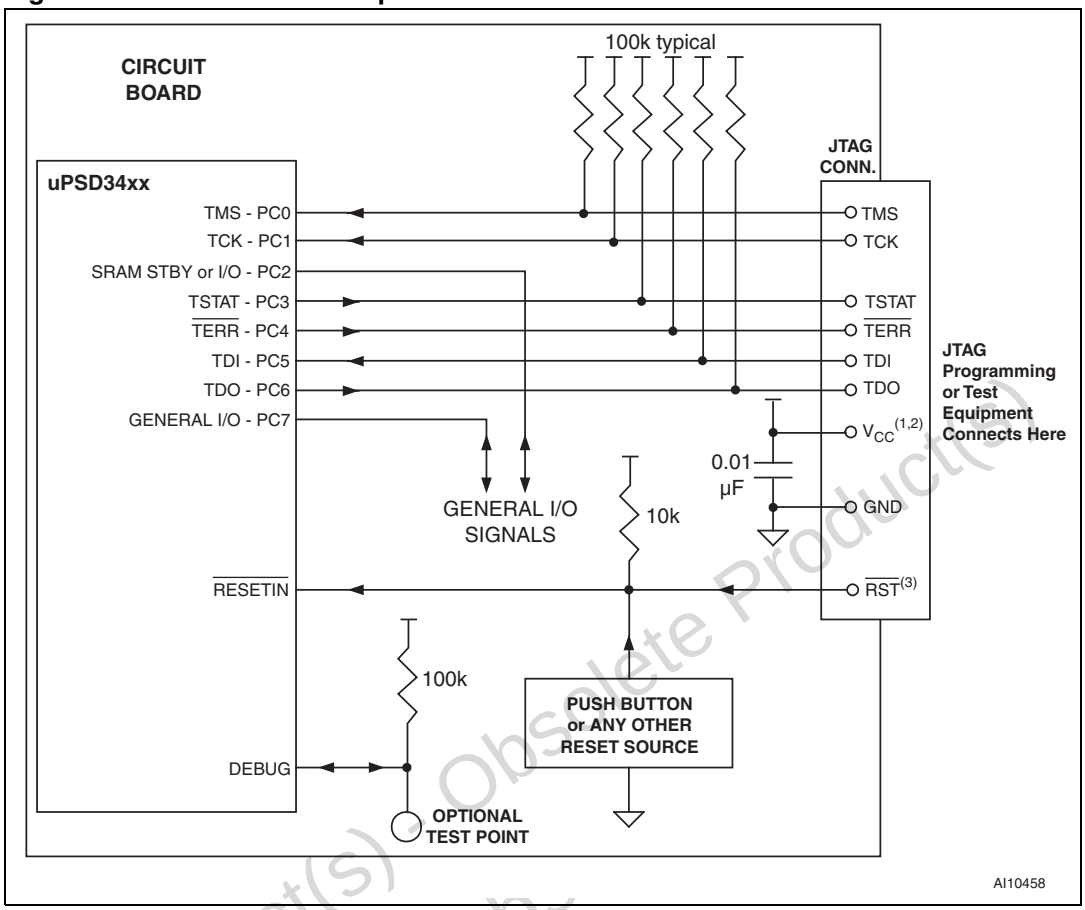


Figure 92. Recommended 6-pin JTAG connections



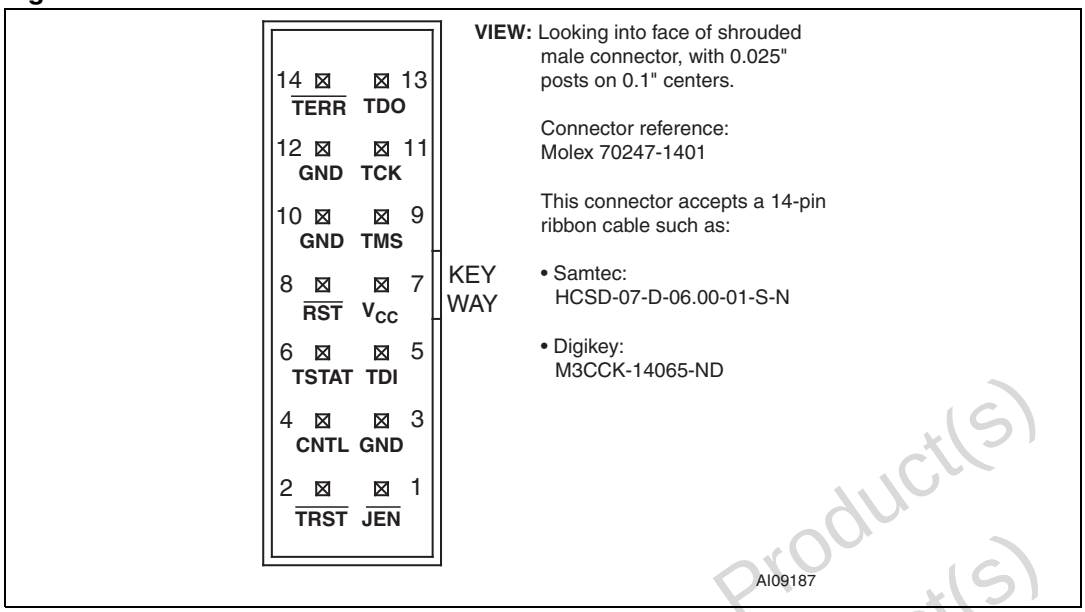
1. For 5 V UPSD34xx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 5 V system V_{DD}.
2. For 3.3 V UPSD34xx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 3.3 V system V_{CC}.
3. This signal is driven by an Open-Drain output in the JTAG equipment, allowing more than one source to activate RESET_IN.

28.6.6 Recommended JTAG connector

There is no industry standard JTAG connector. STMicroelectronics recommends a specific JTAG connector and pinout for uPSD3xxx so programming and debug equipment will easily connect to the circuit board. The user does not have to use this connector if there is a different connection scheme.

The recommended connector scheme can accept a standard 14-pin ribbon cable connector (2 rows of 7 pins on 0.1” centers, 0.025” square posts, standard keying) as shown in *Figure 93*. See the STMicroelectronics “FlashLINK, FL-101 User Manual” for more information.

Figure 93. Recommended JTAG connector



28.6.7 Chaining UPSD34xx devices

It is possible to chain a UPSD34xx device with other UPSD34xx devices on a circuit board, and also chain with IEEE 1149.1 compliant devices from other manufacturers. *Figure 94 on page 263* shows a chaining example. The TDO of one device connects to the TDI of the next device, and so on. Only one device is performing JTAG operations at any given time while the other two devices are in BYPASS mode. Configuration for JTAG chaining can be made in PSDsoft Express by choosing “More than one device” when prompted about chaining devices. Notice in *Figure 94 on page 263* that the UPSD34xx devices are chained externally, but also be aware that the two die within each UPSD34xx device are chained internally. This internal chaining of die is transparent to the user and is taken care of by PSDsoft Express and 3rd party JTAG tool software.

The example in *Figure 94 on page 263* also shows how to use 6-pin JTAG when chaining devices. The signals TSTAT and $\overline{\text{TERR}}$ are configured as open-drain type signals from PSDsoft Express. This facilitates a wired-OR connection of TSTAT signals from multiple UPSD34xx devices and also a wired-OR connection of $\overline{\text{TERR}}$ signals from those same multiple devices. PSDsoft Express puts TSTAT and $\overline{\text{TERR}}$ signals into open-drain mode by default, requiring external pull-up resistors. Click on 'Properties' in the JTAG-ISP window of PSDsoft Express to change to standard CMOS push-pull outputs if desired, but wired-OR logic is not possible in CMOS output mode.

Table 209. AC signal behavior symbols for timing

Letter	Meaning
t	Time
L	Logic level low or ALE
H	Logic level high
V	Valid
X	No longer a valid logic level
Z	Float
PW	Pulse width

Note: Example: t_{AVLX} = time from address valid to ALE invalid.

Figure 97. Switching waveforms – key

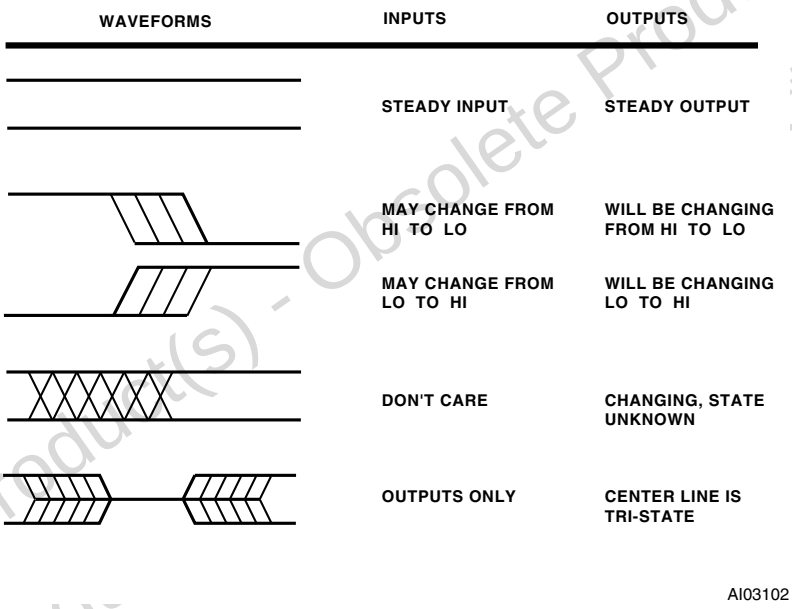


Figure 98. External READ cycle (80-pin device only)

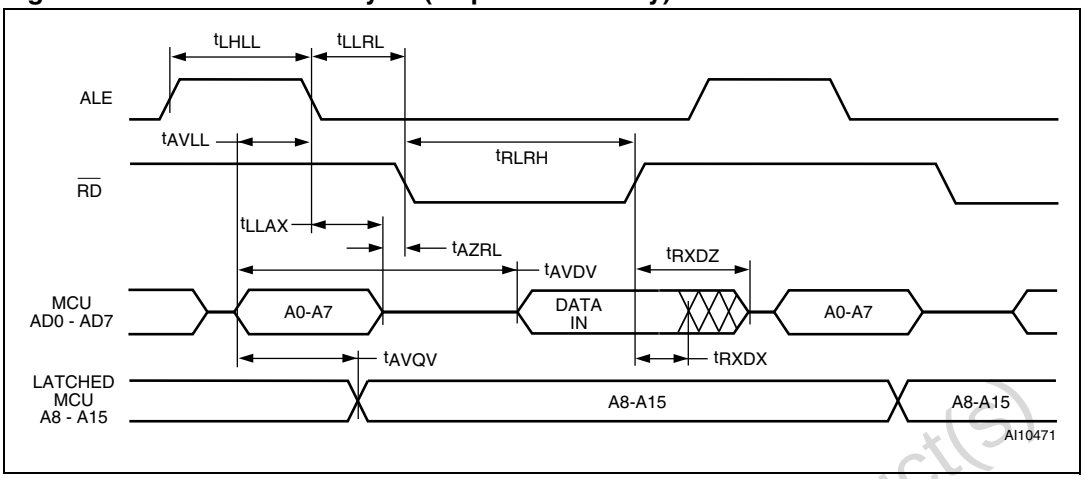


Table 214. External READ cycle AC characteristics (3 V or 5 V device)

Symbol	Parameter	40 MHz oscillator(1)		Variable oscillator $1/t_{CLCL}$ = 3 to 40 MHz		Unit
		Min	Max	Min	Max	
t_{LHLL}	ALE pulse width	17		$t_{CLCL} - 8$		ns
t_{AVLL}	Address setup to ALE	13		$t_{CLCL} - 12$		ns
t_{LLAX}	Address hold after ALE	7.5		$0.5t_{CLCL} - 5$		ns
t_{LLRL}	ALE to $\overline{RD}$	7.5		$0.5t_{CLCL} - 5$		ns
t_{RLRH}	$\overline{RD}$ pulse width(2)	40		$nt_{CLCL} - 10$		ns
t_{RXIX}	Input data hold after $\overline{RD}$	2		2		ns
t_{RHIZ}	Input data float after $\overline{RD}$		10.5		$0.5t_{CLCL} - 2$	ns
t_{AVDX}	Address to valid data in(2)		70		$mt_{CLCL} - 5$	ns
t_{AZRL}	Address float to $\overline{RD}$	–2		–2		ns
t_{AVQV}	Address valid to latched address out on Ports A and B		35.5 (3 V)		$1.5t_{CLCL} - 2$	ns
			28 (5 V)		$t_{CLCL} - 9.5$	ns

1. BUSCON register is configured for 4 PFQCLK.
2. Refer to *Table 215* for “n” and “m” values.

Table 215. n, m, and x, y values

# of PFQCLK in BUSCON register	READ cycle		WRITE cycle	
	n	m	x	y
4	2	3	2	1
5	3	4	3	2
6	4	5	4	3
7	5	6	5	4

35 Revision history

Table 241. Document revision history

Date	Version	Revision details
04-Feb-2005	1	First Edition
30-Mar-2005	2	Added one note in *Section 1: Description on page 20* Added two notes in *Section 25: USB interface on page 150* Changed values in *Table 230 on page 285* (Turbo Off column) Added *Section 34: Important notes on page 294*
25-Oct-2005	3	Changed *Table on page 293* to add sales types with 32K SRAM Changed *Figure 1 on page 21* Changed *Figure 5 on page 30* Corrected Port Pin P1.5 from ADC6 to ADC5 in *Table 2 on page 24* Removed duplicate entry for 80-pin no. 11 in *Table 2 on page 24* Changed *Figure 61 on page 191* Updated *Table 157 on page 193* Updated *Table 239 on page 292*
11-Jul-2006	4	Pin descriptions, *Figure 2 on page 22* and *Figure 3* updated with V_{REF} changed to AV_{REF} V_{REF} changed to AV_{REF} throughout document *Figure 13* updated, correcting CCON[2:0] Clarification of V_{CC}, V_{DD}, AV_{CC} supply voltages in section *Section 30: Maximum rating on page 268* *Section 34: Important notes* updated with differences between silicon revisions A and B, and new Important Notes added. SPI Master Controller corrected to 10MHz in features on first page Latched address out modified, adding A8-A15 to PB0-PB7, *Section Table 2.: Pin definitions* UCON register reset value changed from 00h to 08h throughout Reference to USBCE bit corrected to UPLLCE*Section 14 on page 68* Incorrect references to UART#2 changed to UART#1*Section 22.1 on page 120* UADDR register description enhanced, *Table 100 on page 162* USB interrupts section text expanded, *Section 25.4.3 on page 163* UIFO register table modified, *Table 112 on page 166* UCTL register table enhanced, *Table 120 on page 170* Note added below *Table 122 on page 171* Many modifications made to UCON register description, *Table 126 on page 173* An incorrect reference to CAPCOMHn changed to CAPCOMLn *Section 27.7 on page 184* Part numbering guide updated with B revision information *Section 33 on page 292* *Figure 40 on page 123* updated Document reformatted Note added related to non-support of external indirect addressing, in*Section 9.6* and in *Table 8 on page 54*
26-Jan-2009	5	SRAM standby mode removed. Backup battery feature removed. All products are delivered in ECOPACK-compliant packages. *Section 32: Package mechanical information on page 289* updated. Small text changes including part number capitalization.