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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	80KB (80K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3422evb40u6

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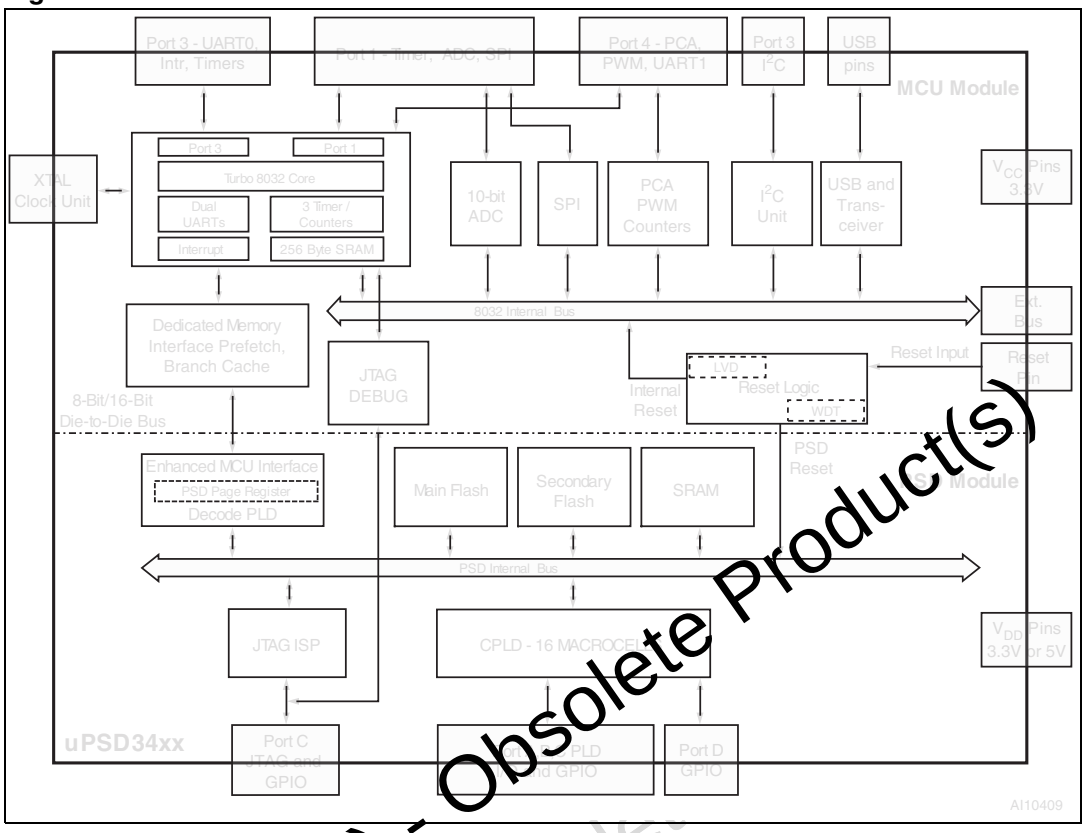
Figure 4. Functional modules



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28.1.4 Secondary Flash memory

The smaller Secondary Flash memory is also divided into equal sized sectors that are individually selectable by the Decode PLD signals, named CSBOOTx, one signal for each Secondary Flash memory sector. Each sector can be located at any address within 8032 program address space (accessed with $\overline{PSEN}$) or XDATA space (accessed with $\overline{RD}$ or $\overline{WR}$) as defined with PSDsoft Express. The user only has to specify an address range for each segment, and specify if Secondary Flash memory will reside in 8032 data or program address space, and then $\overline{PSEN}$, $\overline{RD}$, or $\overline{WR}$ are automatically activated for the specified range. 8032 firmware is easily programmed into Secondary Flash memory using PSDsoft Express and others. See Table 157 on page 193 for Secondary Flash sector sizes.

28.1.5 SRAM

The SRAM is selected by a single signal, named RS0, from the Decode PLD. SRAM may be located at any address within 8032 XDATA space (accessed with $\overline{RD}$ or $\overline{WR}$). These choices are specified using PSDSoft Express, where the user specifies an SRAM address range. See Table 157 on page 193 for SRAM sizes.

Table 157. UPSD34xx memory configuration

Device	Main Flash memory			Secondary Flash memory			SRAM
	Total Flash size (bytes)	Individual sector size (bytes)	Number of sectors (Sector Select signal)	Total Flash size (bytes)	Individual sector size (bytes)	Number of sectors (Sector Select signal)	SRAM size (bytes)
UPSD3422	64 KB	16 KB	4 (FS0-3)	32 KB	8 KB	4 (CSBOOT0-3)	4 KB
UPSD3433	128 KB	16 KB	8 (FS0-7)	32 KB	8 KB	4 (CSBOOT0-3)	8 KB
UPSD3434	256 KB	32 KB	8 (FS0-7)	32 KB	8 KB	4 (CSBOOT0-3)	8 KB
UPSD3454	256 KB	32 KB	8 (FS0-7)	32 KB	8 KB	4 (CSBOOT0-3)	32 KB

28.1.6 Runtime control registers, csiop

A block of 256 bytes is decoded inside the PSD module for module control and status (see Table 162 on page 205). The base address of these 256 locations is referred to in this data sheet as csiop (Chip Select I/O Port), and is selected by the Decode PLD output signal, CSIOP. The csiop registers are always viewed by the 8032 as XDATA, and are accessed with $\overline{RD}$ and $\overline{WR}$ signals. The address range of csiop is specified using PSDsoft Express where the user only has to specify an address range of 256 bytes, and then the $\overline{RD}$ or $\overline{WR}$ signals are automatically activated for the specified range. Individual registers within this block are accessed with an offset from the specified csiop base address. 39 registers are used out of the 256 locations to control the output state of I/O pins, to read I/O pins, to set the memory page, to control 8032 program and data address space, to control power management, to READ/WRITE macrocells inside the General PLD, and other functions during runtime. Unused locations within csiop are reserved and should not be accessed.

28.1.7 Memory page register

8032 MCU architecture has an inherent size limit of 64K bytes in either program address space or XDATA space. Some UPSD34xx devices have much more memory that 64K, so special logic such as this page register is needed to access the extra memory. This 8-bit

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