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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3433evb40u6

Figure 1. Block diagram

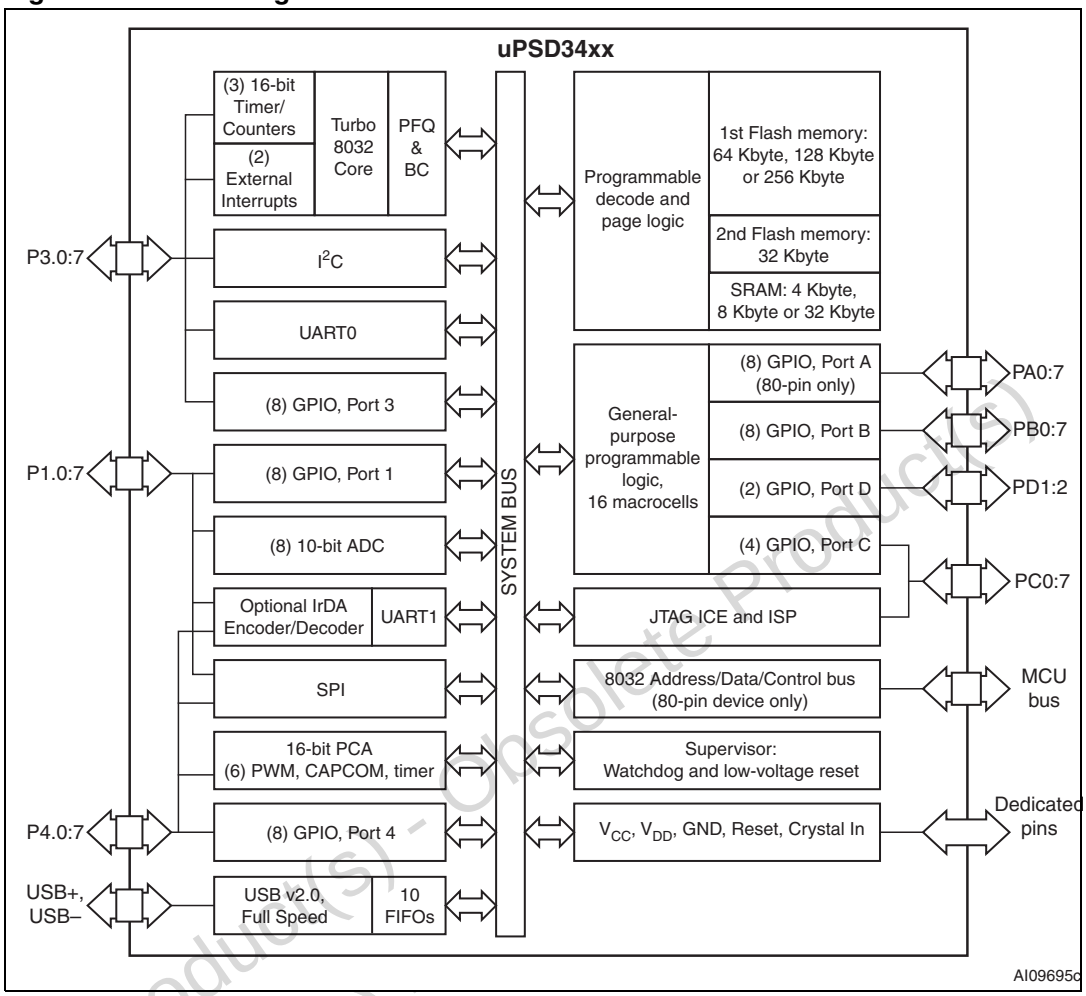


Table 2. Pin definitions

Port pin	Signal name	80-pin No.	52-pin No.(1)	In/out	Function		
					Basic	Alternate 1	Alternate 2
MCUAD0	AD0	36	N/A	I/O	External bus multiplexed address/data bus A0/D0		
MCUAD1	AD1	37	N/A	I/O	Multiplexed address/data bus A1/D1		
MCUAD2	AD2	38	N/A	I/O	Multiplexed address/data bus A2/D2		
MCUAD3	AD3	39	N/A	I/O	Multiplexed address/data bus A3/D3		
MCUAD4	AD4	41	N/A	I/O	Multiplexed address/data bus A4/D4		
MCUAD5	AD5	43	N/A	I/O	Multiplexed address/data bus A5/D5		
MCUAD6	AD6	45	N/A	I/O	Multiplexed address/data bus A6/D6		
MCUAD7	AD7	47	N/A	I/O	Multiplexed address/data bus A7/D7		
P1.0	T2 ADC0	52	34	I/O	General I/O port pin	Timer 2 Count input (T2)	ADC Channel 0 input (ADC0)
P1.1	T2X ADC1	54	35	I/O	General I/O port pin	Timer 2 Trigger input (T2X)	ADC Channel 1 input (ADC1)
P1.2	RxD1 ADC2	56	36	I/O	General I/O port pin	UART1 or IrDA Receive (RxD1)	ADC Channel 2 input (ADC2)
P1.3	TXD1 ADC3	58	37	I/O	General I/O port pin	UART or IrDA Transmit (TxD1)	ADC Channel 3 input (ADC3)
P1.4	SPICLK ADC4	59	38	I/O	General I/O port pin	SPI Clock Out (SPICLK)	ADC Channel 4 input (ADC4)
P1.5	SPIRxD ADC5	60	39	I/O	General I/O port pin	SPI Receive (SPIRxD)	ADC Channel 5 input (ADC5)
P1.6	SPITXD ADC6	61	40	I/O	General I/O port pin	SPI Transmit (SPITxD)	ADC Channel 6 input (ADC6)
P1.7	SPISEL ADC7	64	41	I/O	General I/O port pin	SPI Slave Select (SPISEL)	ADC Channel 7 input (ADC7)
P3.0	RxD0	75	23	I/O	General I/O port pin	UART0 Receive (RxD0)	

Figure 13. Clock generation logic

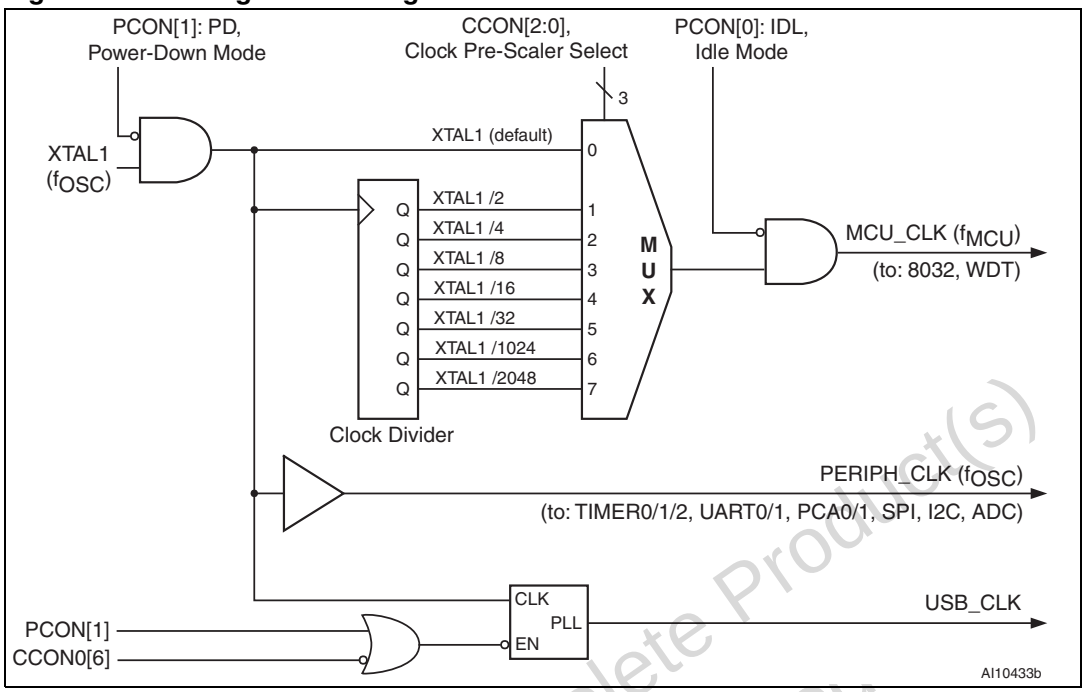


Table 27. CCON0: clock control register (SFR F9h, reset value 50h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLM[4]	PLLEN	UPLLCE	DBGCE	CPUAR	CPUPS[2:0]		

Table 28. CCON0 register bit definition

Bit	Symbol	R/W	Definition
7	PLLM[4]	R,W	Upper bit of the 5-bit PLLM[4:0] Multiplier (Default: '0' for PLLM = 00h)
6	PLLEN	R,W	PLL Enable 0 = Disable PLL operation 1 = Enable PLL operation (Default condition after reset)
5	UPLLCE	R,W	USB Clock Enable 0 = USB clock is disabled (Default condition after reset) 1 = USB clock is enabled
4	DBGCE	R,W	Debug Unit Breakpoint Comparator Enable 0 = JTAG Debug Unit comparators are disabled 1 = JTAG Debug Unit comparators are enabled (Default condition after reset)

Table 45. P1SFS0 and P1SFS1 details (continued)

Port 1 Pin	R/W	Default port function	Alternate 1 port function	Alternate 2 port function
		P1SFS0[i] = 0 P1SFS1[i] = x	P1SFS0[i] = 1 P1SFS1[i] = 0	P1SFS0[i] = 1 P1SFS1[i] = 1
		Port 1 Pin, i = 0.. 7	Port 1 Pin, i = 0.. 7	Port 1 Pin, i = 0.. 7
6	R,W	GPIO	SPI Transmit, SPITXD	ADC Chn 6 input, ADC6
7	R,W	GPIO	SPI Select, SPISEL_	ADC Chn 7 input, ADC7

Table 46. P4SFS0: Port 4 special function select 0 register (SFR 92h, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4SF07	P4SF06	P4SF05	P4SF04	P4SF03	P4SF02	P4SF01	P4SF00

Table 47. P4SFS1: Port 4 special function select 1 register (SFR 93h, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4SF17	P4SF16	P4SF15	P4SF14	P4SF13	P4SF12	P4SF11	P4SF10

Table 48. P4SFS0 and P4SFS1 details

Port 4 pin	R/W	Default port function	Alternate 1 port function	Alternate 2 port function
		P4SFS0[i] = 0 P4SFS1[i] = x	P4SFS0[i] = 1 P4SFS1[i] = 0	P4SFS0[i] = 1 P4SFS1[i] = 1
		Port 4 Pin, i = 0.. 7	Port 4 Pin, i = 0.. 7	Port 4 Pin, i = 0.. 7
0	R,W	GPIO	PCA0 Module 0, TCM0	Timer 2 count input, T2
1	R,W	GPIO	PCA0 Module 1, TCM1	Timer 2 trigger input, TX2
2	R,W	GPIO	PCA0 Module 2, TCM2	UART1 Receive, RXD1
3	R,W	GPIO	PCA0 ext clock, PCACLK0	UART1 Transmit, TXD1
4	R,W	GPIO	PCA1 Module 3, TCM3	SPI Clock, SPICLK
5	R,W	GPIO	PCA1 Module 4, TCM4	SPI Receive, SPIRXD
6	R,W	GPIO	PCA1 Module 5, TCM5	SPI Transmit, SPITXD
7	R,W	GPIO	PCA1 ext clock, PCACLK1	SPI Select, SPISEL_

20 Standard 8032 timer/counters

There are three 8032-style 16-bit Timer/Counter registers (Timer 0, Timer 1, Timer 2) that can be configured to operate as timers or event counters.

There are two additional 16-bit Timer/Counters in the Programmable Counter Array (PCA), see *Section 27.1: PCA block on page 181* for details.

20.1 Standard timer SFRs

Timer 0 and Timer 1 have very similar functions, and they share two SFRs for control:

- TCON (*Table 56 on page 97*)
- TMOD (*Table 58 on page 99*).

Timer 0 has two SFRs that form the 16-bit counter, or that can hold reload values, or that can scale the clock depending on the timer/counter mode:

- TH0 is the high byte, address 8Ch
- TL0 is the low byte, address 8Ah

Timer 1 has two similar SFRs:

- TH1 is the high byte, address 8Dh
- TL1 is the low byte, address 8Bh

Timer 2 has one control SFR:

- T2CON (*Table 60 on page 101*)

Timer 2 has two SFRs that form the 16-bit counter, and perform other functions:

- TH2 is the high byte, address CDh
- TL2 is the low byte, address CCh

Timer 2 has two SFRs for capture and reload:

- RCAP2H is the high byte, address CBh
- RCAP2L is the low byte, address CAh

20.2 Clock sources

When enabled in the "**Timer**" function, the registers THx and TLx are incremented every 1/12 of the oscillator frequency (f_{OSC}). This timer clock source is not effected by MCU clock dividers in the CCON0, stalls from PFQ/BC, or bus transfer cycles. Timers are always clocked at 1/12 of f_{OSC}.

When enabled in the "**Counter**" function, the registers THx and TLx are incremented in response to a 1-to-0 transition sampled at their corresponding external input pin: pin C0 for Timer 0; pin C1 for Timer 1; or pin T2 for Timer 2. In this function, the external clock input pin is sampled by the counter at a rate of 1/12 of f_{OSC}. When a logic '1' is determined in one sample, and a logic '0' in the next sample period, the count is incremented at the very next sample period (period1: sample=1, period2: sample=0, period3: increment count while continuing to sample). This means the maximum count rate is 1/24 of the f_{OSC}. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be active for at least one full sample

Figure 28. Timer 2 in auto-reload mode

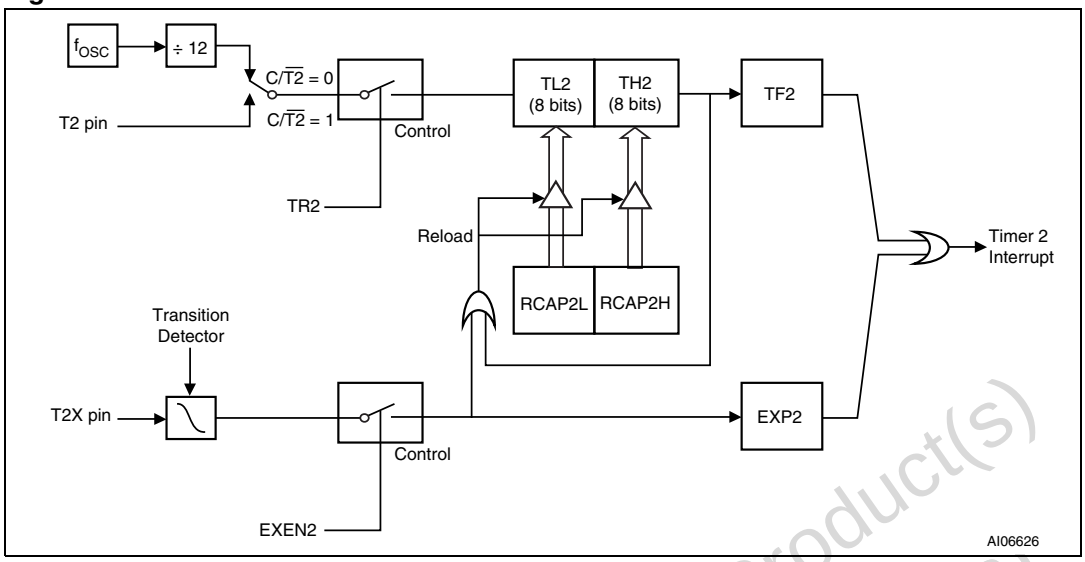


Figure 29. Timer 2 in baud rate generator mode

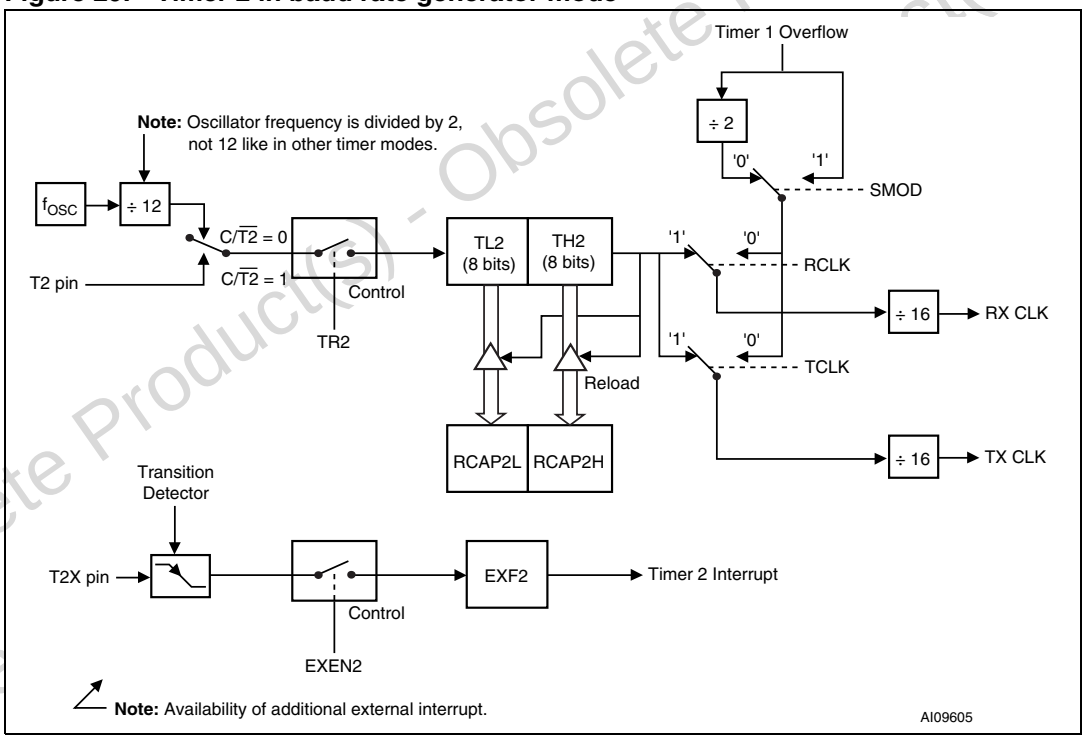


Table 74. Recommended CDIV[4:0] values to generate SIRClk (default CDIV[4:0] = 0Fh, 15 decimal)

f_{OSC} (MHz)	Value in CDIV[4:0]	Resulting f_{SIRCLK} (MHz)
40.00	16h, 22 decimal	1.82
36.864, or 36.00	14h, 20 decimal	1.84, or 1.80
24.00	0Dh, 13 decimal	1.84
11.059, or 12.00	06h, 6 decimal	1.84, or 2.00
7.3728(1)	04h, 4 decimal	1.84

1. When PULSE bit = 0 (fixed data pulse width), this is minimum recommended f_{OSC} because CDIV[4:0] must be 4 or greater.

23.8 I²C interface control register (S1CON)

Table 75. Serial control register S1CON (SFR DCh, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CR2	ENI1	STA	STO	ADDR	AA	CR[1:0]	

Table 76. S1CON register bit definition

Bit	Symbol	R/W	Function
7	CR2	R,W	This bit, along with bits CR1 and CR0, determine the SCL clock frequency (f_{SCL}) when SIOE is in Master mode. These bits create a clock divisor for f_{OSC}. See *Table 77*.
6	ENI1	R,W	I²C Interface Enable 0 = SIOE disabled, 1 = SIOE enabled. When disabled, both SDA and SCL signals are in high impedance state.
5	STA	R,W	START flag. When set, Master mode is entered and SIOE generates a Start condition only if the I²C bus is not busy. When a Start condition is detected on the bus, the STA flag is cleared by hardware. When the STA bit is set during an interrupt service, the Start condition will be generated after the interrupt service.
4	STO	R,W	STOP flag When STO is set in Master mode, the SIOE generates a Stop condition. When a Stop condition is detected, the STO flag is cleared by hardware. When the STO bit is set during an interrupt service, the Stop condition will be generated after the interrupt service.
3	ADDR	R,W	This bit is set when an address byte received in Slave mode matches the device address programmed into the S1ADR register. The ADDR bit must be cleared with firmware.
2	AA	R,W	Assert Acknowledge enable If AA = 1, an acknowledge signal (low on SDA) is automatically returned during the acknowledge bit-time on the SCL line when any of the following three events occur: 1. SIOE in Slave mode receives an address that matches contents of S1ADR register 2. A data byte has been received while SIOE is in Master Receiver mode 3. A data byte has been received while SIOE is a selected Slave Receiver When AA = 0, no acknowledge is returned (high on SDA during acknowledge bit-time).
1, 0	CR1, CR0	R,W	These bits, along with bit CR2, determine the SCL clock frequency (f_{SCL}) when SIOE is in Master mode. These bits create a clock divisor for f_{OSC}. See *Table 77* for values.

Enable individual I2C interrupt and set priority
- SFR IEA.I2C = 1
- SFR IPA.I2C = 1 if high priority is desired

Set the Device address for Slave mode
- SFR S1ADR = XXh, desired address

Enable SIOE (as Slave) to return an ACK signal
- SFR S1CON.AA = 1

Master-Transmitter

Disable all interrupts
- SFR IE.EA = 0

Set pointer to global data xmit buffer, set count
- *xmit_buf = *pointer to data
- buf_length = number of bytes to xmit

Set global variables to indicate Master-Xmitter
- I2C_master = 1, I2C_xmitter = 1

Disable Master from returning an ACK
- SFR S1CON.AA = 0

Enable I2C SIOE
- SFR S1CON.INI1 = 1

Transmit Address and R/W bit = 0 to Slave
- Is bus not busy? (SFR S1STA.BBUSY = 0?)

<If busy, then test until not busy>
- SFR S1DAT[7:0] = Load Slave Address & FEh
- SFR S1CON.STA = 1, send Start on bus

<bus transmission begins>

Enable All Interrupts and go do something else
- SFR IE.EA = 1

Master-Receiver

Disable all interrupts
- SFR IE.EA = 0

Set pointer to global data recv buffer, set count
- *recv_buf = *pointer to data
- buf_length = number of bytes to recv

Set global variables to indicate Master-Xmitter
- I2C_master = 1, I2C_xmitter = 0

Disable Master from returning an ACK
- SFR S1CON.AA = 0

- USB endpoint0 status (USTA)

  The USB Endpoint0 Status register (see *Table 122*) provides the status for events that occur on the USB that are directed to endpoint0.

Table 122. USB endpoint0 status (USTA 0EDh, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	RCVT	SETUP	IN	OUT

Table 123. USTA register bit definition

Bit	Symbol	R/W	Definition
7	–	–	Reserved
6	–	–	Reserved
5	–	–	Reserved
4	–	–	Reserved
3	RCVT	R	Received Data Toggle Bit This bit indicates the toggle bit of the received data packet: 0 = Data0, and 1 = Data1
2	SETUP	R/W	SETUP Token Detect Bit This bit is set when Endpoint0 receives a SETUP token. This bit is not cleared when Endpoint0 receives an IN or OUT token following the SETUP token that set this bit. This bit is cleared by software or a reset.
1	IN	R	IN Token Detect Bit This bit is set when Endpoint0 receives an IN token. This bit is cleared when Endpoint0 receives a SETUP or OUT token.
0	OUT	R	OUT Token Detect Bit This bit is set when Endpoint0 receives an OUT token. This bit is cleared when Endpoint0 receives a SETUP or IN token.

Caution: Disabling and enabling the USB SIE using the USBEN bit in the UCTL register clears the RCVT, IN, and OUT bits in this register.

Table 143. PCA0 and PCA1 registers

SFR address		Register name		RW	Register function
PCA0	PCA1	PCA0	PCA1		
A2	BA	PCACL0	PCACL1	RW	The low 8 bits of PCA 16-bit counter.
A3	BB	PCACH0	PCACH1	RW	The high 8 bits of PCA 16-bit counter.
A4	BC	PCACON0	PCACON1	RW	Control register – Enable PCA, Timer Overflow flag , PCA Idle Mode, and Select clock source.
A5	A5	PCASTA	N/A	RW	Status register, Interrupt Status flags – Common for both PCA Block 0 and 1.
A9, AA, AB	BD, BE, BF	TCMMODE0 TCMMODE1 TCMMODE2	TCMMODE3 TCMMODE4 TCMMODE5	RW	TCM Mode – Capture, Compare, and Toggle Enable Interrupts – PWM Mode Select.
AC AD	C1 C2	CAPCOML0 CAPCOMH0	CAPCOML3 CAPCOMH3	RW	Capture/Compare registers of TCM0
AF B1	C3 C4	CAPCOML1 CAPCOMH1	CAPCOML4 CAPCOMH4	RW	Capture/Compare registers of TCM1
B2 B3	C5 C6	CAPCOML2 CAPCOMH2	CAPCOML5 CAPCOMH5	RW	Capture/Compare registers of TCM2
B4	C7	PWMF0	PWMF1	RW	The 8-bit register to program the PWM frequency. This register is used for programmable, 8-bit PWM Mode only.
FB	FC	CCON2	CCON3	RW	Specify the pre-scaler value of PCA0 or PCA1 clock input

27.2 PCA clock selection

- The clock input to the 16-bit up counter in the PCA block is user-programmable. The three clock sources are:
- PCA Prescaler Clock (PCA0CLK, PCA1CLK)
- Timer 0 Overflow
- External Clock, Pin P4.3 or P4.7

The clock source is selected in the configuration register PCACON. The Prescaler output clock PCACLK is the f_{OSC} divided by the divisor which is specified in the CCON2 or CCON3 register. When External Clock is selected, the maximum clock frequency should not exceed $f_{OSC}/4$.

28.5.35 I/O ports

There are four programmable I/O ports on the PSD module: Port A (80-pin device only), Port B, Port C, and Port D. Ports A and B are eight bits each, Port C is four bits, and Port D is two bits for 80-pin devices or 1-bit for 52-pin devices. Each port pin is individually configurable, thus allowing multiple functions per port. The ports are configured using PSDsoft Express then programming with JTAG, and also by the 8032 writing to csiop registers at run-time.

Topics discussed in this section are:

- General port architecture
- Port operating modes
- Individual port structure

28.5.36 General port architecture

The general architecture for a single I/O Port pin is shown in *Figure 79 on page 232*. Port structures for Ports A, B, C, and D differ slightly and are shown in *Figure 84 on page 243* though *Figure 87 on page 247*.

Figure 79 on page 232 shows four csiop registers whose outputs are determined by the value that the 8032 writes to csiop Direction, Drive, Control, and Data Out. The I/O Port logic contains an output mux whose mux select signal is determined by PSDsoft Express and the csiop Control register bits at run-time. Inputs to this output mux include the following:

1. Data from the csiop Data Out register for MCU I/O output mode (All ports)
2. Latched de-multiplexed 8032 Address for Address Output mode (Ports A and B only)
3. Peripheral I/O mode data bit (Port A only)
4. GPLD OMC output (Ports A, B, and C).

The Port Data Buffer (PDB) provides feedback to the 8032 and allows only one source at a time to be read when the 8032 reads various csiop registers. There is one PDB for each port pin enabling the 8032 to read the following on a pin-by-pin basis:

1. MCU I/O signal direction setting (csiop Direction reg)
2. Pin drive type setting (csiop Drive Select reg)
3. Latched Addr Out mode setting (csiop Control reg)
4. MCU I/O pin output setting (csiop Data Out reg)
5. Output Enable of pin driver (csiop Enable Out reg)
6. MCU I/O pin input (csiop Data In reg)

A port pin's output enable signal is controlled by a two input OR gate whose inputs come from: a product term of the AND-OR array; the output of the csiop direction register. If an output enable from the AND-OR Array is not defined, and the port pin is not defined as an OMC output, and if Peripheral I/O mode is not used, then the csiop direction register has sole control of the OE signal.

As shown in *Figure 79 on page 232*, a physical port pin is connected to the I/O Port logic and is also separately routed to an IMC, allowing the 8032 to read a port pin by two different methods (MCU I/O input mode or read the IMC).

28.5.37 Port operating modes

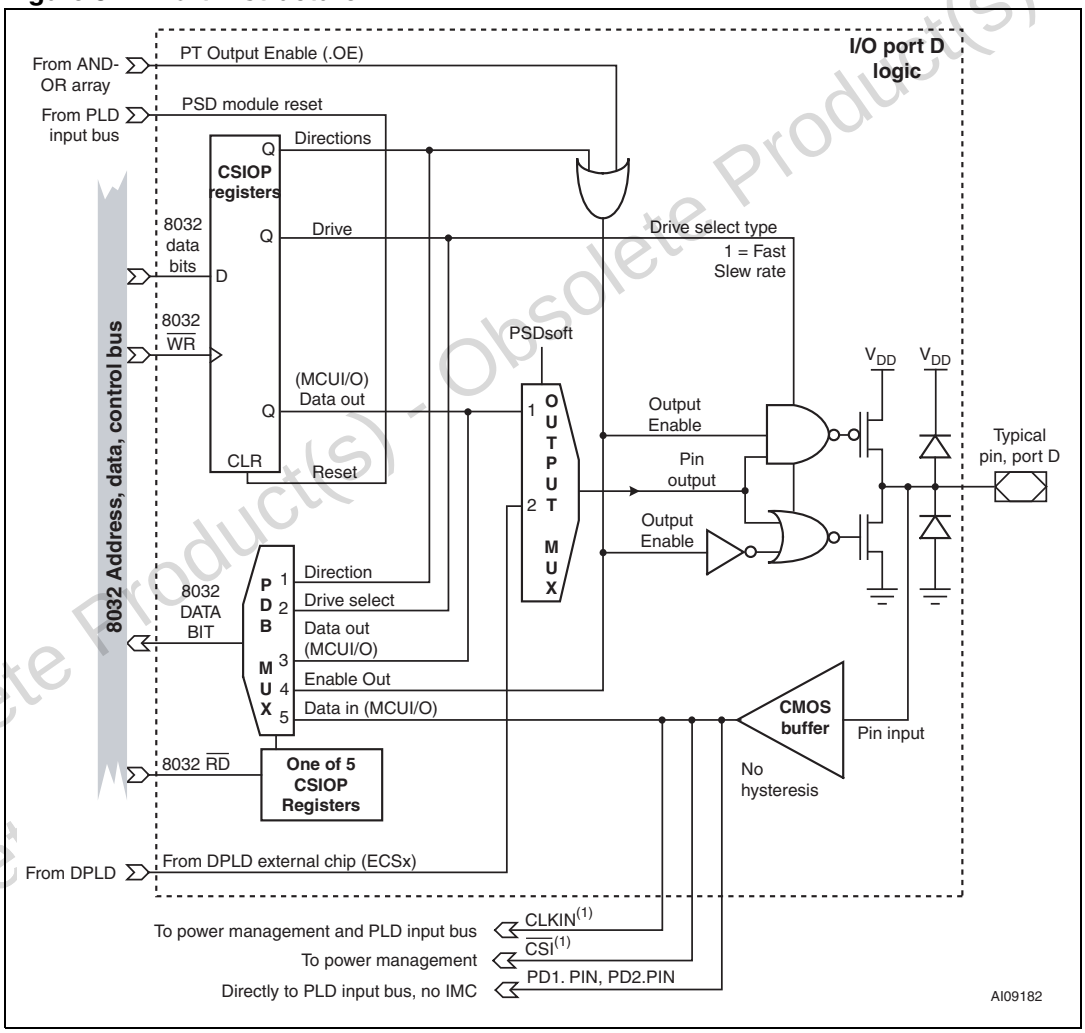
I/O Port logic has several modes of operation. *Table 171 on page 229* summarizes which modes are available on each port. Each of the port operating modes are described in

Port D pins can also be configured in PSDsoft as pins for other dedicated functions:

- PD1 can be used as a common clock input to all 16 OMC Flip-flops (see *Section 28.1.11: OMCs on page 195*) and also the *Section 28.5.53: Automatic power-down (APD) on page 250*.
- PD2 can be used as a common chip select signal ($\overline{CSI}$) for the Flash and SRAM memories on the PSD module (see *Section 28.5.55: Chip select input (CSI) on page 253*). If driven to logic '1' by an external source, $\overline{CSI}$ will force the Flash memory into standby mode regardless of what other internal memory select signals are doing on the PSD module. This is specified in PSDsoft as "PSD Chip Select Input, $\overline{CSI}$".

Port D also supports the Fast Slew Rate output drive type option using the csiop Drive Select registers.

Figure 87. Port D structure



Note: 1 Optional function on a specific Port D pin.

28.6.5 6-pin JTAG ISP (optional)

The optional signals TSTAT and $\overline{\text{TERR}}$ are programming status flags that can reduce programming time by as much as 30% compared to 4-pin JTAG because this status information does not have to be scanned out of the device serially. TSTAT and $\overline{\text{TERR}}$ must be used as a pair for 6-pin JTAG operation.

- TSTAT (pin PC3) indicates when programming of a single Flash location is complete. Logic 1 = Ready, Logic 0 = busy.
- $\overline{\text{TERR}}$ (pin PC4) indicates if there was a Flash programming error. Logic 1 = no error, Logic 0 = error.

The pin functions for PC3 and PC4 must be selected as “Dedicated JTAG - TSTAT” and “Dedicated JTAG - $\overline{\text{TERR}}$” in PSDsoft Express to enable 6-pin JTAG ISP.

No 8032 firmware is needed to use 6-pin ISP because all ISP functions are controlled from the external JTAG program/test equipment.

TSTAT and $\overline{\text{TERR}}$ are functional only when JTAG ISP operations are occurring, which means they are non-functional during JTAG debugging of the 8032 on the MCU module.

Programming times vary depending on the number of locations to be programmed and the JTAG programming equipment, but typical JTAG ISP programming times are 10 to 25 seconds using 6-pin JTAG. The signals TSTAT and $\overline{\text{TERR}}$ are not included in the IEEE 1149.1 specification.

Figure 92 on page 261 shows recommended connections on a circuit board to a JTAG program/test tool using 6-pin JTAG. It is required to connect the $\overline{\text{RST}}$ output signal from the JTAG program/test equipment to the $\overline{\text{RESET\_IN}}$ input on the UPSD34xx. The $\overline{\text{RST}}$ signal is driven by the equipment with an Open Drain driver, allowing other sources (like a push button) to drive $\overline{\text{RESET\_IN}}$ without conflict.

Note: The recommended pull-up resistors and decoupling capacitor are illustrated in Figure 92.

30 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 205. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	125	°C
T_{LEAD}	Lead temperature during soldering (20 seconds max.)(1)		235	°C
V_{IO}	Input and output voltage (Q = V_{OH} or Hi-Z)	–0.5	6.5	V
V_{CC}, V_{DD}, AV_{CC}	Supply voltage	–0.5	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–2000	2000	V

1. IPC/JEDEC J-STD-020A.
2. *JEDEC Std JESD22-A114A (C1=100pF, R1=1500 Ω, R2=500 Ω).*

Table 212. PSD module DC characteristics (with 5 V V_{DD})

Symbol	Parameter		Test condition (in addition to those in *Table 211 on page 271*)	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage		4.5 V < V_{DD} < 5.5 V	2		V_{DD} +0.5	V
V_{IL}	Input low voltage		4.5 V < V_{DD} < 5.5 V	–0.5		0.8	V
V_{LKO}	V_{DD} (min) for Flash erase and program			2.5		4.2	V
V_{OL}	Output low voltage		I_{OL} = 20 µA, V_{DD} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{DD} = 4.5 V		0.25	0.45	V
V_{OH}	Output high voltage		I_{OH} = –20 µA, V_{DD} = 4.5 V	4.4	4.49		V
			I_{OH} = –2 mA, V_{DD} = 4.5 V	2.4	3.9		V
I_{SB}	Standby supply current for power-down mode		$\overline{CSI}$ > V_{DD} – 0.3 V(1)(2)		120	250	µA
I_{LI}	Input leakage current		V_{SS} < V_{IN} < V_{DD}	–1	±0.1	1	µA
I_{LO}	Output leakage current		0.45 < V_{OUT} < V_{DD}	–10	±5	10	µA
I_{CC} (DC)(3)	Operating supply current	PLD only	PLD_TURBO = Off, f = 0 MHz (3)		0		µA/PT
			PLD_TURBO = On, f = 0 MHz		400	700	µA/PT
		Flash memory	During Flash memory WRITE/Erase Only		15	30	mA
			Read only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC)(3)	PLD AC adder					(4)	
	Flash memory AC adder				1.5	2.5	mA/MHz
	SRAM AC adder				1.5	3.0	mA/MHz

1. Internal Power-down mode is active.
2. PLD is in non-Turbo mode, and none of the inputs are switching.
3. I_{OUT} = 0 mA.
4. Please see *Figure 95 on page 265* for the PLD current calculation.

Figure 104. Input macrocell timing (product term clock)

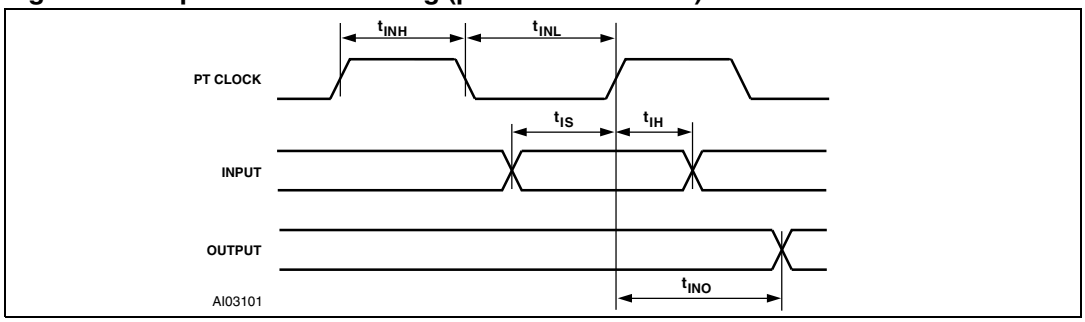


Table 226. Input macrocell timing (5 V PSD module)

Symbol	Parameter	Conditions	Min	Max	PT Aloc	Turbo off	Unit
t_{IS}	Input setup time	(1)	0				ns
t_{IH}	Input hold time		15			+ 10	ns
t_{INH}	NIB input high time		9				ns
t_{INL}	NIB input low time		9				ns
t_{INO}	NIB input to combinatorial delay			34	+ 2	+ 10	ns

1. Inputs from Port A, B, and C relative to register/ latch clock from the PLD. ALE/AS latch timings refer to t_{AVLX} and t_{LXAX}.

Table 227. Input macrocell timing (3 V PSD module)

Symbol	Parameter	Conditions	Min	Max	PT Aloc	Turbo off	Unit
t_{IS}	Input setup time	(1)	0				ns
t_{IH}	Input hold time	(Note 1)	25			+ 15	ns
t_{INH}	NIB input high time	(Note 1)	12				ns
t_{INL}	NIB input low time	(Note 1)	12				ns
t_{INO}	NIB input to combinatorial delay	(Note 1)		43	+ 4	+ 15	ns

1. Inputs from Port A, B, and C relative to register/latch clock from the PLD. ALE latch timings refer to t_{AVLX} and t_{LXAX}.

Table 228. Program, WRITE and erase times (5 V, 3 V PSD modules)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Flash program		8.5		s
	Flash bulk erase(1) (pre-programmed)		3(2)	10	s
	Flash bulk erase (not pre-programmed)		5		s
t_{WHQV3}	Sector erase (pre-programmed)		1	10	s
t_{WHQV2}	Sector erase (not pre-programmed)		2.2		s
t_{WHQV1}	byte program		14	150	µs
	Program / erase cycles (per sector)	100 000			cycles

32 Package mechanical information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

35 Revision history

Table 241. Document revision history

Date	Version	Revision details
04-Feb-2005	1	First Edition
30-Mar-2005	2	Added one note in *Section 1: Description on page 20* Added two notes in *Section 25: USB interface on page 150* Changed values in *Table 230 on page 285* (Turbo Off column) Added *Section 34: Important notes on page 294*
25-Oct-2005	3	Changed *Table on page 293* to add sales types with 32K SRAM Changed *Figure 1 on page 21* Changed *Figure 5 on page 30* Corrected Port Pin P1.5 from ADC6 to ADC5 in *Table 2 on page 24* Removed duplicate entry for 80-pin no. 11 in *Table 2 on page 24* Changed *Figure 61 on page 191* Updated *Table 157 on page 193* Updated *Table 239 on page 292*
11-Jul-2006	4	Pin descriptions, *Figure 2 on page 22* and *Figure 3* updated with V_{REF} changed to AV_{REF} V_{REF} changed to AV_{REF} throughout document *Figure 13* updated, correcting CCON[2:0] Clarification of V_{CC}, V_{DD}, AV_{CC} supply voltages in section *Section 30: Maximum rating on page 268* *Section 34: Important notes* updated with differences between silicon revisions A and B, and new Important Notes added. SPI Master Controller corrected to 10MHz in features on first page Latched address out modified, adding A8-A15 to PB0-PB7, *Section Table 2.: Pin definitions* UCON register reset value changed from 00h to 08h throughout Reference to USBCE bit corrected to UPLLCE*Section 14 on page 68* Incorrect references to UART#2 changed to UART#1*Section 22.1 on page 120* UADDR register description enhanced, *Table 100 on page 162* USB interrupts section text expanded, *Section 25.4.3 on page 163* UIFO register table modified, *Table 112 on page 166* UCTL register table enhanced, *Table 120 on page 170* Note added below *Table 122 on page 171* Many modifications made to UCON register description, *Table 126 on page 173* An incorrect reference to CAPCOMHn changed to CAPCOMLn *Section 27.7 on page 184* Part numbering guide updated with B revision information *Section 33 on page 292* *Figure 40 on page 123* updated Document reformatted Note added related to non-support of external indirect addressing, in*Section 9.6* and in *Table 8 on page 54*
26-Jan-2009	5	SRAM standby mode removed. Backup battery feature removed. All products are delivered in ECOPACK-compliant packages. *Section 32: Package mechanical information on page 289* updated. Small text changes including part number capitalization.