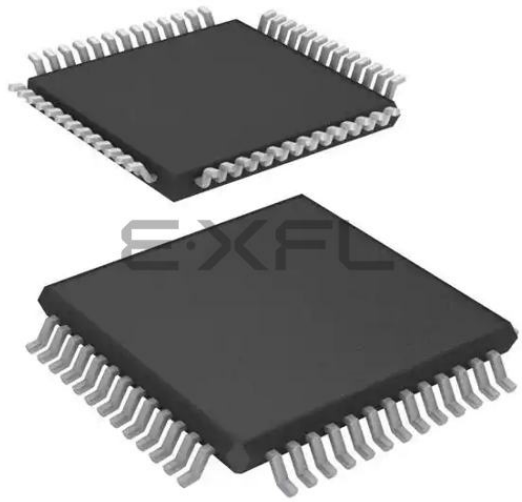

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3434e-40t6

List of figures

19.2 Low V_{CC} voltage detect, LVD

An internal reset is generated by the LVD circuit when V_{CC} drops below the reset threshold, V_{LV_THRESH}. After V_{CC} returns to the reset threshold, the MCU_RESET signal will remain asserted for t_{RST_ACTV} before it is released. The LVD circuit is always enabled (cannot be disabled by SFR), even in Idle mode and Power-down mode. The LVD input has a voltage hysteresis of V_{RST_HYS} and will reject voltage spikes less than a duration of t_{RST_FIL}.

Important note: The LVD voltage threshold is V_{LV_THRESH}, suitable for monitoring both the 3.3 V V_{CC} supply on the MCU module and the 3.3 V V_{DD} supply on the PSD module for 3.3 V UPSD34xxV devices, since these supplies are one in the same on the circuit board.

However, for 5 V UPSD34xx devices, V_{LV_THRESH} is not suitable for monitoring the 5 V V_{DD} voltage supply (V_{LV_THRESH} is too low), but good for monitoring the 3.3 V V_{CC} supply. In the case of 5 V UPSD34xx devices, an external means is required to monitor the separate 5 V V_{DD} supply, if desired.

19.3 Power-up reset

At power up, the internal reset generated by the LVD circuit is latched as a logic '1' in the POR bit of the SFR named PCON (*Table 33 on page 74*). Software can read this bit to determine whether the last MCU reset was the result of a power up (cold reset) or a reset from some other condition (warm reset). This bit must be cleared with software.

19.4 JTAG debug reset

The JTAG Debug Unit can generate a reset for debugging purposes. This reset source is also available when the MCU is in Idle mode and Power-Down mode (the user can use the JTAG debugger to exit these modes).

19.5 Watchdog timer, WDT

When enabled, the WDT will generate a reset whenever it overflows. Firmware that is behaving correctly will periodically clear the WDT before it overflows. Run-away firmware will not be able to clear the WDT, and a reset will be generated.

By default, the WDT is disabled after each reset.

Note: The WDT is not active during Idle mode or Power-down mode.

There are two SFRs that control the WDT, they are WDKEY (*Table 52 on page 94*) and WDRST (*Table 54 on page 94*).

If WDKEY contains 55h, the WDT is disabled. Any value other than 55h in WDKEY will enable the WDT. By default, after any reset condition, WDKEY is automatically loaded with 55h, disabling the WDT. It is the responsibility of initialization firmware to write some value other than 55h to WDKEY after each reset if the WDT is to be used.

The WDT consists of a 24-bit up-counter (*Figure 23*), whose initial count is 000000h by default after every reset. The most significant byte of this counter is controlled by the SFR, WDRST. After being enabled by WDKEY, the 24-bit count is increased by 1 for each MCU machine cycle. When the count overflows beyond FFFFFh (2^{24} MCU machine cycles), a reset is issued and the WDT is automatically disabled (WDKEY = 55h again).

Table 69. Commonly used baud rates generated from timer 1 (continued)

UART mode	f_{OSC} MHz	Desired baud rate	Resultant baud rate	Baud rate deviation	SMOD bit in PCON	Timer 1		
						C/$\overline{T}$ Bit in TMOD	Timer mode in TMOD	TH1 reload value (hex)
Modes 1 or 3	3.6864	19200	19200	0	1	0	2	FF
Modes 1 or 3	3.6864	9600	9600	0	1	0	2	FE
Modes 1 or 3	1.8432	9600	9600	0	1	0	2	FF
Modes 1 or 3	1.8432	4800	4800	0	1	0	2	FE

21.4 More about UART mode 0

Refer to the block diagram in *Figure 30 on page 113*, and timing diagram in *Figure 31 on page 113*.

Transmission is initiated by any instruction which writes to the SFR named SBUF. At the end of a write operation to SBUF, a 1 is loaded into the 9th position of the transmit shift register and tells the TX Control unit to begin a transmission. Transmission begins on the following MCU machine cycle, when the “SEND” signal is active in *Figure 31*.

SEND enables the output of the shift register to the alternate function on the port containing pin RxD, and also enables the SHIFT CLOCK signal to the alternate function on the port containing the pin, TxD. At the end of each SHIFT CLOCK in which SEND is active, the contents of the transmit shift register are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the '1' that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift, then deactivate SEND, and then set the interrupt flag TI. Both of these actions occur at S1P1.

Reception is initiated by the condition REN = 1 and RI = 0. At the end of the next MCU machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE. RECEIVE enables the SHIFT CLOCK signal to the alternate function on the port containing the pin, TxD. Each pulse of SHIFT CLOCK moves the contents of the receive shift register one position to the left while RECEIVE is active. The value that comes in from the right is the value that was sampled at the RxD pin. As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control unit to do one last shift, and then it loads SBUF. After this, RECEIVE is cleared, and the receive interrupt flag RI is set.

Figure 32. UART mode 1, block diagram

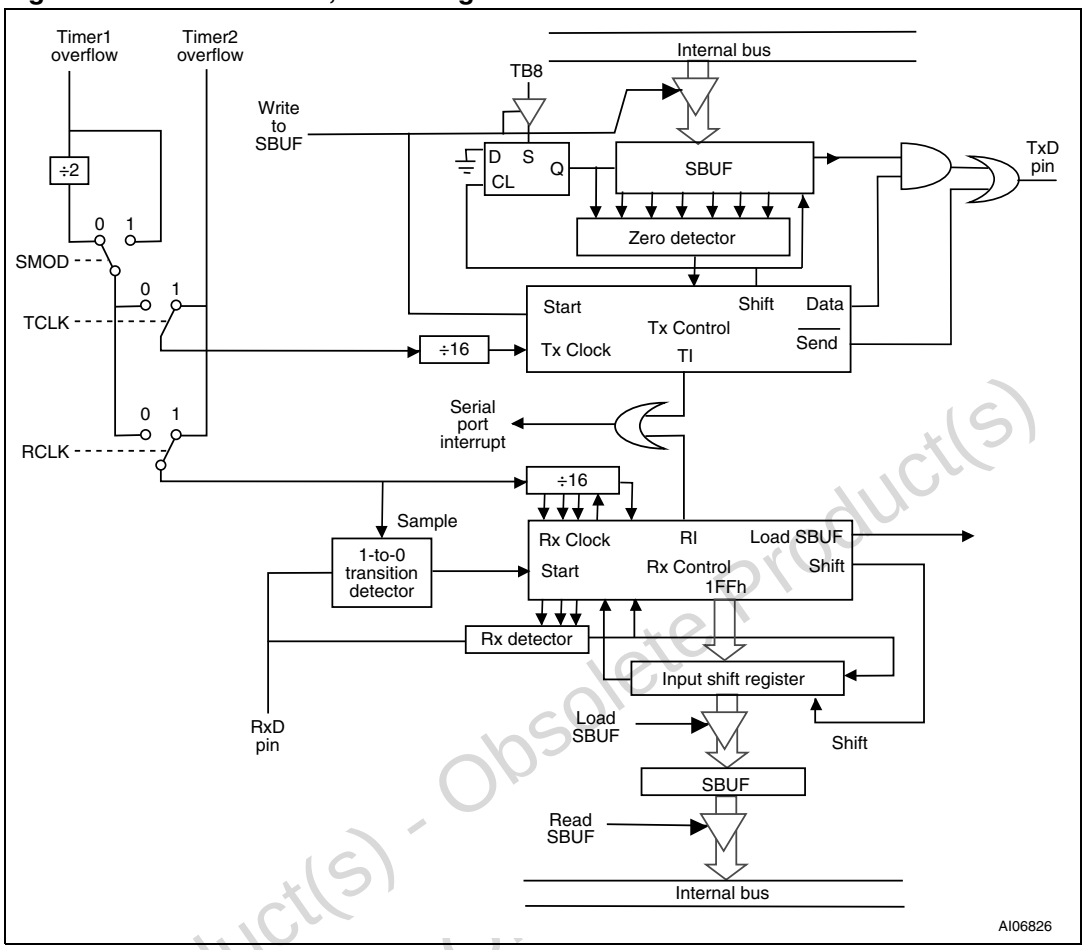


Figure 33. UART mode 1, timing diagram

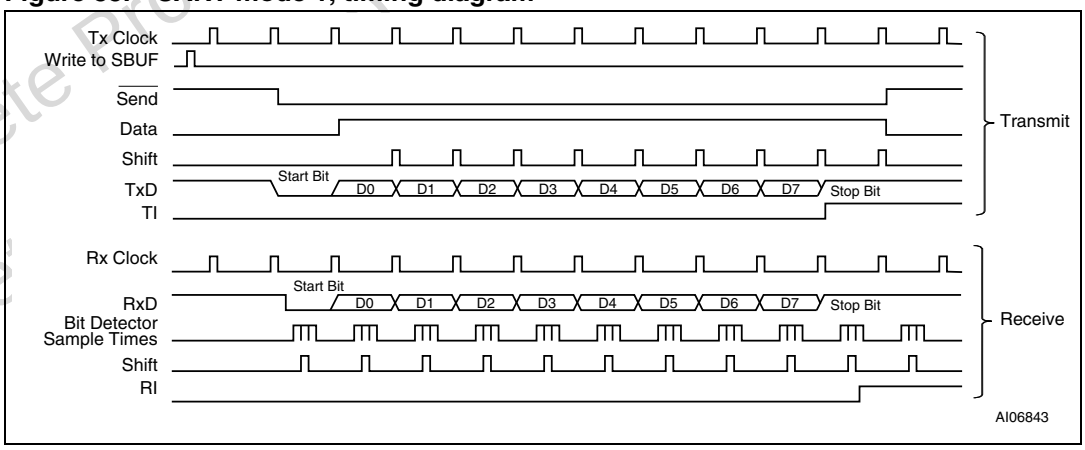
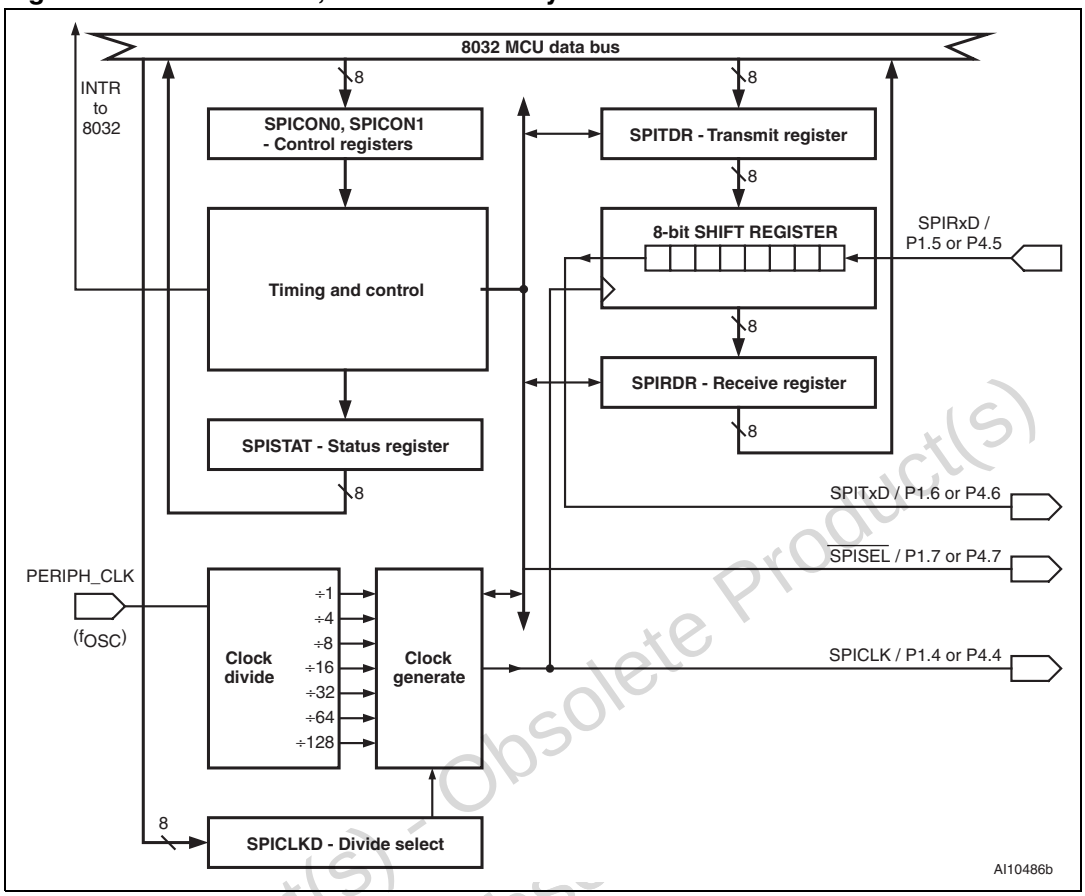


Figure 47. SPI interface, master mode only



24.5 SPI configuration

The SPI interface is reset by the MCU reset, and firmware needs to initialize the SFRs SPICON0, SPICON1, and SPICLKD to define several operation parameters.

The SPO Bit in SPICON0 determines the clock polarity. When SPO is set to '0,' a data bit is transmitted on SPITxD from one rising edge of SPICLK to the next and is guaranteed to be valid during the falling edge of SPICLK. When SPO is set to '1,' a data bit is transmitted on SPITxD from one falling edge of SPICLK to the next and is guaranteed to be valid during the rising edge of SPICLK. The UPSD34xx will sample received data on the appropriate edge of SPICLK as determined by SPO. The effect of the SPO Bit can be seen in *Figure 45* and *Figure 46 on page 145*.

The FLSB Bit in SPICON0 determines the bit order while transmitting and receiving the 8-bit data. When FLSB is '0,' the 8-bit data is transferred in order from MSB (first) to LSB (last). When FLSB Bit is set to '1,' the data is transferred in order from LSB (first) to MSB (last).

The clock signal generated on SPICLK is derived from the internal PERIPH_CLK signal. PERIPH_CLK always operates at the frequency, f_{OSC}, and runs constantly except when stopped in MCU Power Down mode. SPICLK is a result of dividing PERIPH_CLK by a sum of different divisors selected by the value contained in the SPICLKD register. The default value in SPICLKD after a reset divides PERIPH_CLK by a factor of 4. The bits in SPICLKD can be set to provide resulting divisor values in of sums of multiples of 4, such as 4, 8, 12,

- USB global interrupt flag register (UIF0)

  There are many different events that generate a USB interrupt requiring a number of registers to indicate the cause of the interrupt. To more efficiently identify the cause of the interrupt, the USB global interrupt flag register (see *Table 112*) indicates the type of interrupt that occurred. Once the type of interrupt is identified, the associated interrupt flag register may be read to determine the exact cause of the interrupt.

Table 112. USB global interrupt flag register (UIF0 0E8h, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GLF	INF	OUTF	NAKF	RSTF	SUSPENDF	EOPF	RESUMF

Table 113. UIF0 register bit definition

Bit	Symbol	R/W	Definition
7	GLF	R	Global Interrupt flag Logical OR of the RSTF, SUSPENDF, EOPF, and RESUMF interrupt flags
6	INF	R	IN FIFO Interrupt flag Logical OR of the IN4F, IN3F, IN2F, IN1F, and IN0F interrupt flags
5	OUTF	R	OUT FIFO Interrupt flag Logical OR of the OUT4F, OUT3F, OUT2F, OUT1F, and OUT0F interrupt flags
4	NAKF	R	NAK FIFO Interrupt flag Logical OR of the NAK4F, NAK3F, NAK2F, NAK1F, and NAK0F interrupt flags
3	RSTF	R/W	USB Reset flag This bit is set when a USB Reset is detected on the D+ and D- lines. *Note: A USB Reset does not reset the MCU nor the USB module. Firmware should disable/enable the USB SIE using the USEN bit in the UCTL register and initialize all USB related registers as appropriate.*
2	SUSPENDF	R/W	USB suspend mode flag This bit is set when the SIE detects 3ms of no activity on the bus and the clock to the SIE is also shut down to conserve power. Clearing this bit turns the SIE clock on.
1	EOPF	R/W	End of Packet flag This bit is set when a valid End of Packet sequence is detected on the D+ and D– line.
0	RESUMEF	R/W	Resume flag This bit is set when USB bus activity is detected while the SUSPNDF Bit is set. When a Resume is detected, the SUSPENDF bit must be cleared (if set) to turn the SIE clock on.

- USB endpoint0 status (USTA)

  The USB Endpoint0 Status register (see *Table 122*) provides the status for events that occur on the USB that are directed to endpoint0.

Table 122. USB endpoint0 status (USTA 0EDh, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	RCVT	SETUP	IN	OUT

Table 123. USTA register bit definition

Bit	Symbol	R/W	Definition
7	–	–	Reserved
6	–	–	Reserved
5	–	–	Reserved
4	–	–	Reserved
3	RCVT	R	Received Data Toggle Bit This bit indicates the toggle bit of the received data packet: 0 = Data0, and 1 = Data1
2	SETUP	R/W	SETUP Token Detect Bit This bit is set when Endpoint0 receives a SETUP token. This bit is not cleared when Endpoint0 receives an IN or OUT token following the SETUP token that set this bit. This bit is cleared by software or a reset.
1	IN	R	IN Token Detect Bit This bit is set when Endpoint0 receives an IN token. This bit is cleared when Endpoint0 receives a SETUP or OUT token.
0	OUT	R	OUT Token Detect Bit This bit is set when Endpoint0 receives an OUT token. This bit is cleared when Endpoint0 receives a SETUP or IN token.

Caution: Disabling and enabling the USB SIE using the USBEN bit in the UCTL register clears the RCVT, IN, and OUT bits in this register.

Table 155. TCMMODE0 - TCMMODE5 register bit definition (continued)

Bit	Symbol	Function
2	TOGGLE	1 - A match on the comparator results in a toggling output on CEXn pin.
1-0	PWM[1:0]	01 Enable PWM Mode (x8), fixed frequency. Enable the CEXn pin as a PWM output. 10 Enable PWM Mode (x8) with programmable frequency. Enable the CEXn pin as a PWM output. 11 Enable PWM Mode (x10 or x16), fixed frequency. Enable the CEXn pin as a PWM output.

Table 156. TCMMODE register configurations

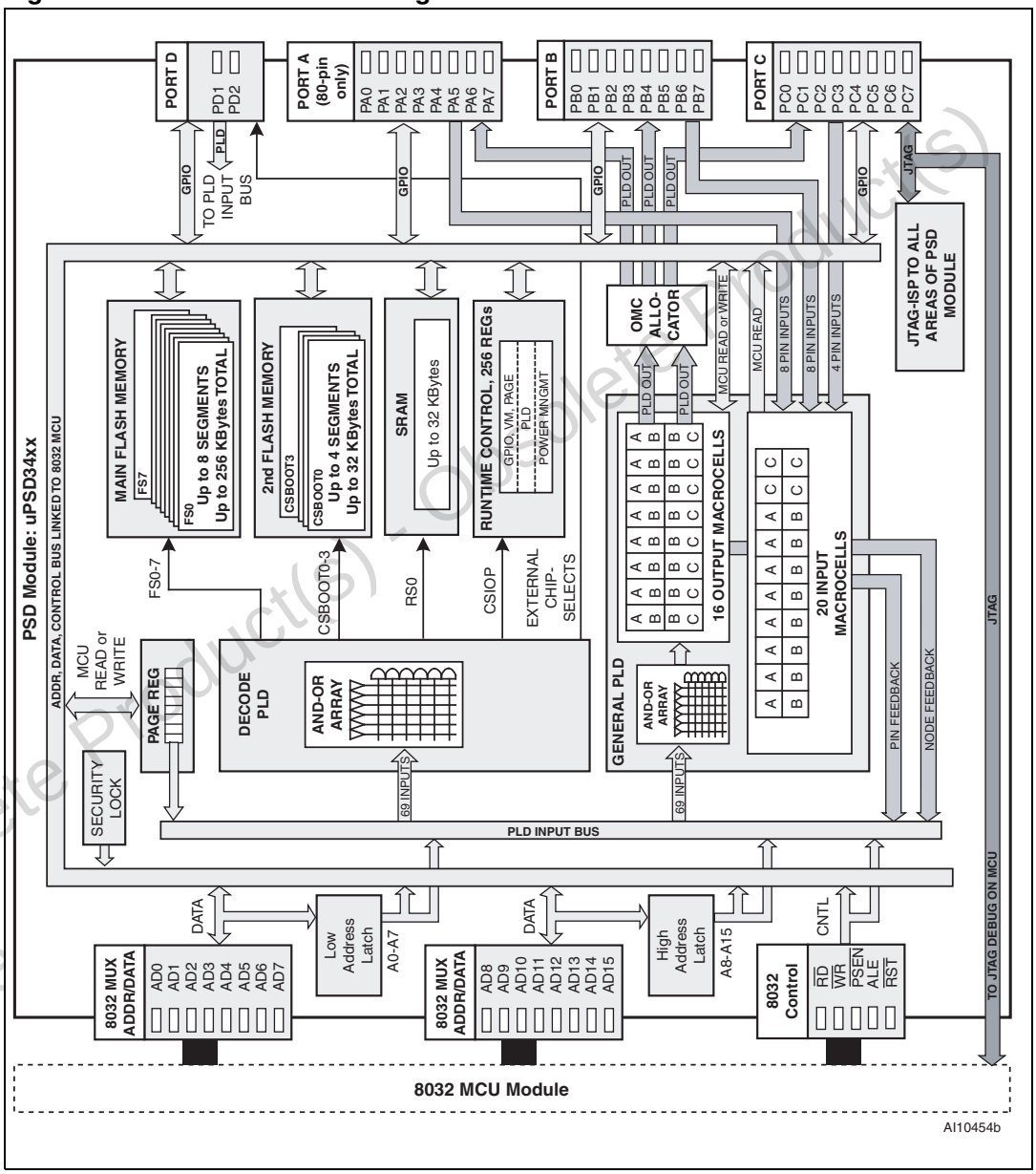
EINTF	E_COMP	CAP_PE	CAP_NE	MATCH	TOGGLE	PWM1	PWM0	TCM FUNCTION
0	0	0	0	0	0	0	0	No operation (reset value)
0	1	0	0	0	0	0	1	8-bit PWM, fixed frequency
0	1	0	0	0	0	1	0	8-bit PWM, programmable frequency
0	1	0	0	0	0	1	1	10-bit or 16-bit PMW, fixed frequency(1)
X	1	0	0	1	1	0	0	16-bit toggle
X	1	0	0	1	0	0	0	16-bit Software Timer
X	X	0	1	0	0	0	0	16-bit capture, negative trigger
X	X	1	0	0	0	0	0	16-bit capture, positive trigger
X	X	1	1	0	0	0	0	16-bit capture, transition trigger

1. 10-bit PWM mode requires the 10B_PWM Bit in the PCACON register set to '1.'

28 PSD module

The PSD module is stacked with the MCU module to form the UPSD34xx, see *Section 3: Hardware description on page 28*. Details of the PSD module are shown in *Figure 61*. The two separate modules interface with each other at the 8032 Address, Data, and Control interface blocks in *Figure 61*.

Figure 61. PSD module block diagram



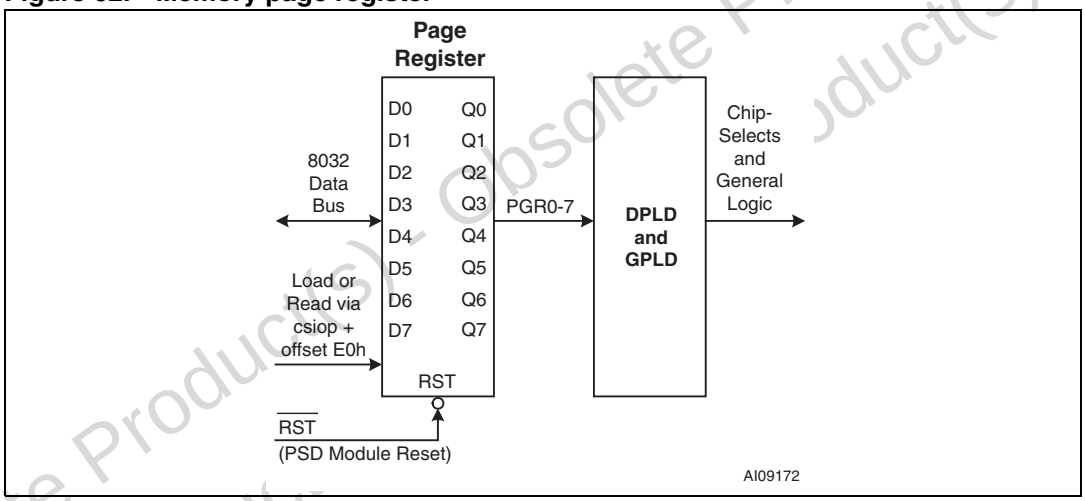
page register (*Figure 62*) can be loaded and read by the 8032 at runtime as one of the csiop registers. Page register outputs feed directly into both PLDs creating extended address signals used to “page” memory beyond the 64K byte limit (program space or XDATA). Most 8051 compilers directly support memory paging, also known as memory banking. If memory paging is not needed, or if not all eight page register bits are needed for memory paging, the remaining bits may be used in the General PLD for general logic. Page register outputs are cleared to logic ’0’ at reset and power-up.

28.1.8 Programmable logic (PLDs)

The UPSD34xx contains two PLDs (*Figure 73 on page 221*) that may optionally run in Turbo or Non-Turbo mode. PLDs operate faster (less propagation delay) while in Turbo mode but consume more power than in Non-Turbo mode. Non-Turbo mode allows the PLDs to go to standby automatically when no PLD inputs are changing to conserve power.

The logic configuration (from equations) of both PLDs is stored with non-volatile Flash technology and the logic is active upon power-up. PLDs may NOT be programmed by the 8032, PLD programming only occurs through the JTAG interface.

Figure 62. Memory page register



28.1.9 PLD #1, decode PLD (DPLD)

This programmable logic implements memory mapping and is used to select one of the individual Main Flash memory segments, one of individual Secondary Flash memory segments, the SRAM, or the group of csiop registers when the 8032 presents an address to DPLD inputs (see *Figure 74 on page 223*). The DPLD can also optionally drive external chip select signals on Port D pins. The DPLD also optionally produces two select signals (PSEL0 and PSEL1) used to enable a special data bus repeater function on Port A, referred to as Peripheral I/O Mode. There are 69 DPLD input signals which include: 8032 address and control signals, page register outputs, PSD module Port pin inputs, and GPLD logic feedback.

28.1.10 PLD #2, general PLD (GPLD)

This programmable logic is used to create both combinatorial and sequential general purpose logic (see *Figure 75 on page 224*). The GPLD contains 16 Output Macrocells (OMCs) and 20 Input Macrocells (IMCs). Output Macrocell registers are unique in that they

Native product terms come from the AND-OR Array. Each OMC may borrow product terms only from certain other OMCs, if they are not in use. Product term allocation does not add any propagation delay to the logic. The fitter report generated by PSDsoft Express will show any PT allocation that has occurred.

If an equation requires more product terms than are available to it through PT allocation, then “external” product terms are required, which consumes other OMCs. This is called product term expansion and also happens automatically in PSDsoft Express as needed. PT expansion causes additional propagation delay because an additional OMC is consumed by the expansion process and its output is rerouted (or fed back) into the AND-OR array. The user can examine the fitter report generated by PSDsoft Express to see resulting PT allocation and PT expansion (expansion will have signal names, such as ‘*.fb_0’ or ‘*.fb_1’). PSDsoft Express will always try to fit the logic design first by using PT allocation, and if that is not sufficient then PSDsoft Express will use PT expansion.

Product term expansion may occur in the DPLD for complex chip select equations for Flash memory sectors and for SRAM, but this is a rare occurence. If PSDsoft Express does use PT expansion in the DPLD, it results in an approximate 15ns additional propagation delay for that chip select signal, which gives 15ns less time for the memory to respond. Be aware of this and consider adding a wait state to the 8032 bus access (using the SFR named, BUSCON), or lower the 8032 clock frequency to avoid problems with memory access time.

Figure 77. OMC allocator

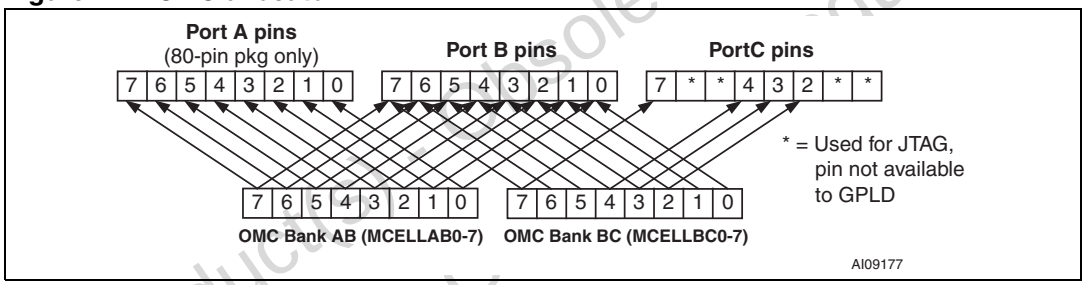
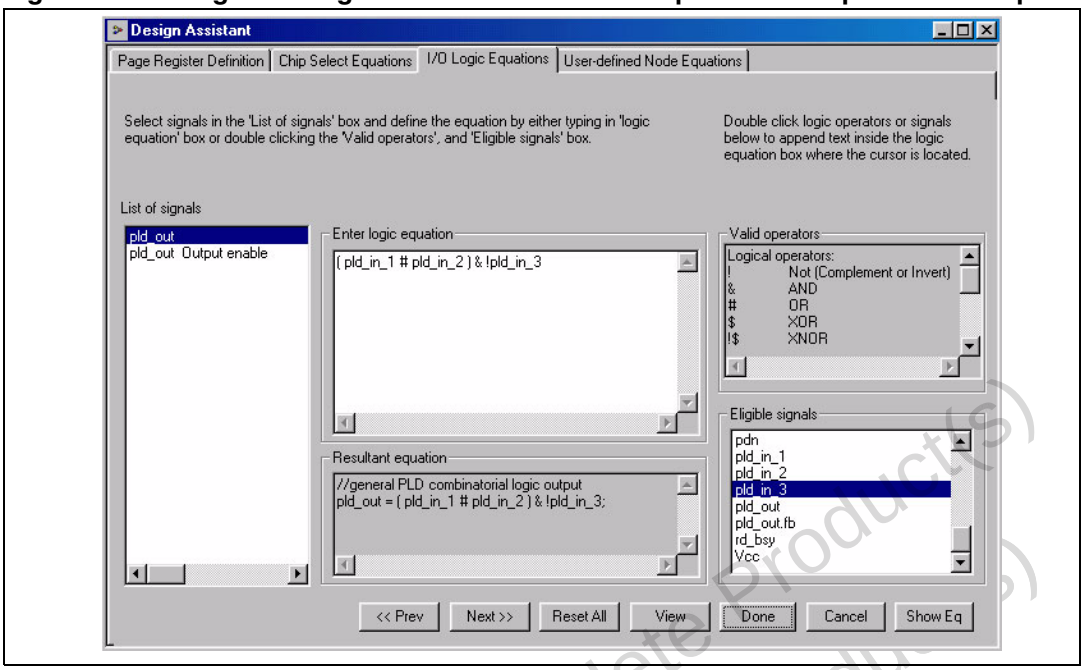


Table 168. OMC port and data bit assignments

OMC	Port assignment(1),(2)	Native product terms from AND-OR array	Maximum borrowed product terms	Data bit on 8032 data bus for loading or reading OMC
MCELLAB0	Port A0 or B0	3	6	D0
MCELLAB1	Port A1 or B1	3	6	D1
MCELLAB2	Port A2 or B2	3	6	D2
MCELLAB3	Port A3 or B3	3	6	D3
MCELLAB4	Port A4 or B4	3	6	D4
MCELLAB5	Port A5 or B5	3	6	D5
MCELLAB6	Port A6 or B6	3	6	D6
MCELLAB7	Port A7 or B7	3	6	D7
MCELLBC0	Port B0	4	5	D0
MCELLBC1	Port B1	4	5	D1
MCELLBC2	Port B or C2	4	5	D2

Figure 82. Using the design assistant in PSDsoft Express for simple PLD example



28.5.40 Latched address output mode

In the MCU module, the data bus Bits D0-D15 are multiplexed with the address Bits A0-A15, and the ALE signal is used to separate them with respect to time. Sometimes it is necessary to send de-multiplexed address signals to external peripherals or memory devices. Latched Address Output mode will drive individual demuxed address signals on pins of Ports A or B. Port pins can be designated for this function on a pin-by-pin basis, meaning that an entire port will not be sacrificed if only a few address signals are needed.

To activate this mode, the desired pins on Port A or Port B are designated as “Latched Address Out” in PSDsoft. Then in the 8032 initialization firmware, a logic ’1’ is written to the csiop Control register for Port A or Port B in each bit position that corresponds to the pin of the port driving an address signal. *Table 190* and *Table 191* define the csiop Control register locations and bit assignments.

The latched low address byte A4-A7 is available on both Port A and Port B. The high address byte A8-A15 is available on Port B only. Selection of high or low address byte is specified in PSDsoft Express.

Table 190. Latched address output, port A contro register(1)(2)(3)(address = csiop + offset 02h)l

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 (addr A7)	PA6 (addr A6)	PA5 (addr A5)	PA4 (addr A4)	PA3 (addr A3)	PA2 (Addr A2)	PA1 (addr A1)	PA0 (addr A0)

1. Port A not available on 52-pin UPSD34xx devices.
2. For each bit, 1 = drive demuxed 8032 address signal on pin, 0 = pin is default mode, MCU I/O.
3. Default state for register is 00h after reset or power-up.

Upon power-up, and while $\overline{RST}$ is asserted, the PSD module immediately loads its configuration from non-volatile bits to configure the PLDs and other items. PLD logic is operational and ready for use well before $\overline{RST}$ is de-asserted. The state of PLD outputs are determined by equations specified in PSDsoft Express.

The Flash memories are reset to Read Array mode after any assertion of $\overline{RST}$ (even if a program or erase operation is occurring).

Flash memory WRITE operations are automatically prevented while V_{DD} is ramping up until it rises above the V_{LKO} voltage threshold at which time Flash memory WRITE operations are allowed.

Once the UPSD34xx is up and running, any subsequent reset operation is referred to as a warm reset, until power is turned off again. Some PSD module functions are reset in different ways depending if the reset condition was caused from a power-up reset or a warm reset. *Table 203 on page 256* summarizes how PSD module functions are affected by power-up and warm resets, as well as the affect of PSD module power-down mode (from APD).

The I/O pins of PSD module Ports A, B, C, and D do not have weak internal pull-ups.

In MCU I/O mode, Latched Address Out mode, and Peripheral I/O mode, the pins of Ports A, B, C, and D become standard CMOS inputs during a reset condition. If no external devices are driving these pins during reset, then these inputs may float and draw excessive current. If low power consumption is critical during reset, then these floating inputs should be pulled up externally to V_{DD} with a weak (100KΩ minimum) resistor.

In PLD I/O mode, pins of Ports A, B, C, and D may also float during reset if no external device is driving them, and if there is no equation specified for the DPLD or GPLD to make them an output. In this case, a weak external pull-up resistor (100KΩ minimum) should be used on floating pins to avoid excessive current draw.

The pins on Ports 1, 3, and 4 of the 8032 MCU module do have weak internal pull-ups and the inputs will not float, so no external pull-ups are needed.

Table 203. Function status during power-up reset, warm reset, power-down mode

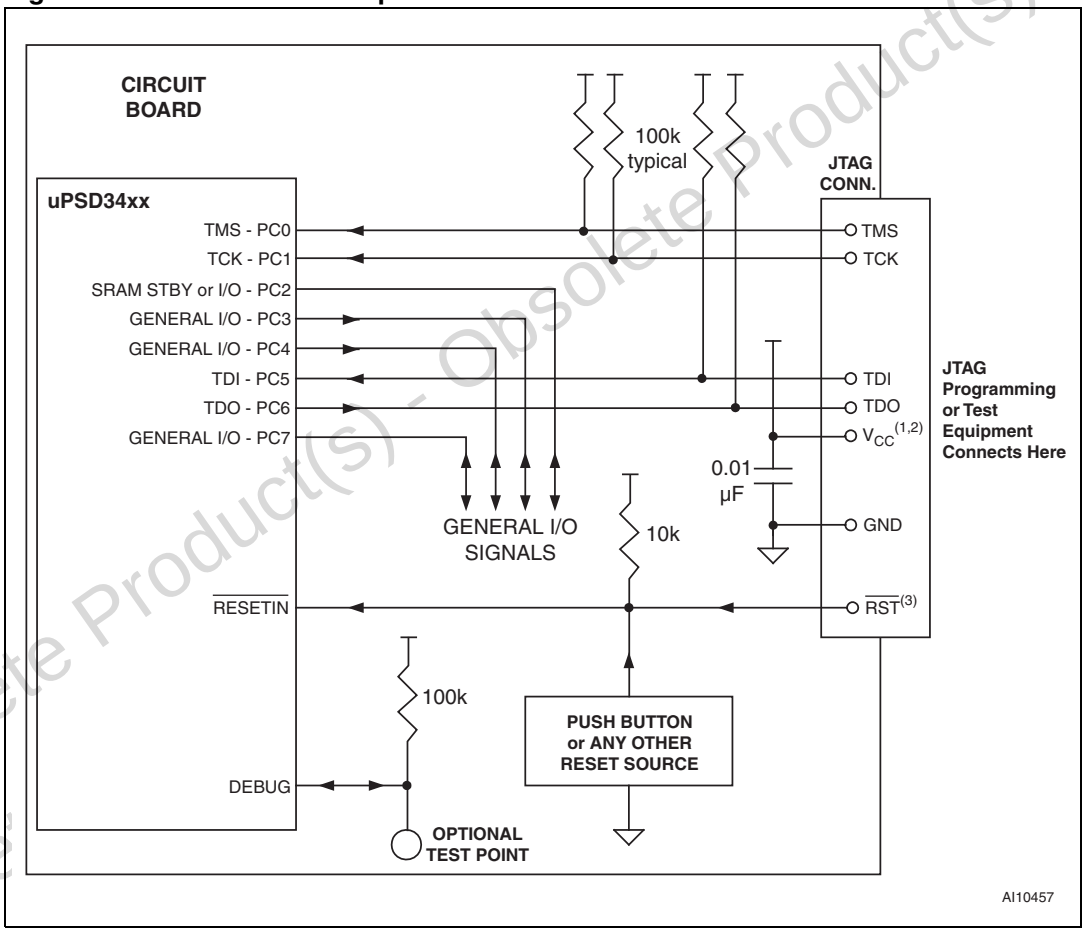
Port configuration or register	Power-up reset	Warm reset	APD Power-down mode
MCU I/O	Pins are in input mode	Pins are in input mode	Pin logic state is unchanged
PLD I/O	Pin logic is valid after internal PSD module configuration bits are loaded. Happens long before $\overline{RST}$ is de-asserted	Pin logic is valid and is determined by PLD logic equations	Pin logic depends on inputs to PLD (8032 addresses are blocked from reaching PLD inputs during power-down mode)
Latched address out mode	Pins are High Impedance	Pins are high impedance	Pins logic state not defined since 8032 address signals are blocked
Peripheral I/O mode	Pins are High Impedance	Pins are High Impedance	Pins are High Impedance
JTAG ISP and debug	JTAG channel is active and available	JTAG channel is active and available	JTAG channel is active and available
PMMR0 and PMMR2	Cleared to 00h	Unchanged	Unchanged
Output of OMC Flip-flops	Cleared to '0'	Depends on .re and .pr equations	Depends on .re and .pr equations

28.6.4 4-pin JTAG ISP (default)

The four basic JTAG pins on Port C are enabled for JTAG operation at all times. These pins may not be used for other I/O functions. There is no action needed in PSDsoft Express to configure a device to use 4-pin JTAG, as this is the default condition. No 8032 firmware is needed to use 4-pin ISP because all ISP functions are controlled from the external JTAG program/test equipment. *Figure 91* shows recommended connections on a circuit board to a JTAG program/test tool using 4-pin JTAG. It is required to connect the $\overline{\text{RST}}$ output signal from the JTAG program/test equipment to the $\overline{\text{RESET\_IN}}$ input on the UPSD34xx. The $\overline{\text{RST}}$ signal is driven by the equipment with an Open Drain driver, allowing other sources (like a push button) to drive $\overline{\text{RESET\_IN}}$ without conflict.

Note: The recommended pull-up resistors and decoupling capacitor are illustrated in Figure 91.

Figure 91. Recommended 4-pin JTAG connections



1. For 5 V UPSD34xx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 5 V system V_{DD}.
2. For 3.3 V UPSD34xx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 3.3 V system V_{CC}.
3. This signal is driven by an Open-Drain output in the JTAG equipment, allowing more than one source to activate $\overline{\text{RESETIN}}$.

Table 211. MCU module DC characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL2}	Output low voltage (other ports)	I_{OL} =5 mA			0.6	V
						V
V_{OH2}	Output high voltage (Port 0 push-pull)	I_{OH} = –5 mA	2.4			V
						V
V_{OH3}	Output high voltage (other ports bidirectional mode)	I_{OH} = –20 µA	2.4			V
V_{OP}	XTAL open bias voltage (XTAL1, XTAL2)	I_{OL} = 3.2 mA	1.0		2.0	V
I_{RST}	RESET pin pull-up current (RESET)	$V_{IN} = V_{SS}$	–10		–55	µA
I_{FR}	XTAL feedback resistor current (XTAL1)	XTAL1 = V_{CC}; XTAL2 = V_{SS}	–20		50	µA
I_{IHL1}	Input high leakage current (port 0)	$V_{SS} < V_{IN} < 5.5$ V	–10		10	µA
I_{IHL2}	Input high leakage current (ports 1, 3, 4)	V_{IH} = 2.3 V	–10		10	µA
I_{ILL}	Input low leakage current (ports 1, 3, 4)	V_{IL} < 0.5 V	–10		10	µA
I_{PD} (3)	Power-down mode	V_{CC} = 3.6 V		65	95	µA
$I_{CC\text{-}CPU}$ (4)(5)(6)	Active - 12 MHz	V_{CC} = 3.6 V		14	20	mA
	Idle - 12 MHz			10	12	mA
	Active - 24 MHz	V_{CC} = 3.6 V		19	30	mA
	Idle - 24 MHz			13	17	mA
	Active - 40 MHz	V_{CC} = 3.6 V		26	40	mA
	Idle - 40 MHz			17	22	mA

1. Power supply (V_{CC}, AV_{CC}) is always 3.0 to 3.6 V for the MCU module. V_{DD} for the PSD module may be 3 V or 5 V.
2. Port 1 is not 5 V tolerant; maximum $V_{IH} = V_{CC} + 0.5$.
3. I_{PD} (Power-down Mode) is measured with: XTAL1 = V_{SS}; XTAL2 = NC; RESET = V_{CC}; Port 0 = V_{CC}; all other pins are disconnected.
4. $I_{CC\text{-}CPU}$ (Active mode) is measured with: XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} – 0.5$ V, XTAL2 = NC; RESET = V_{SS}; Port 0 = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (approximately 1mA).
5. $I_{CC\text{-}CPU}$ (Idle Mode) is measured with: XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} – 0.5$ V, XTAL2 = NC; RESET = V_{CC}; Port 0 = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (approximately 1 mA). All IP clocks are disabled and the MCU clock is set to $f_{OSC}/2048$.
6. I/O current = 0 mA, all I/O pins are disconnected.

Table 219. USB transceiver specification

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
UV_{IL}	Low input voltage	V_{DD} = 3.6V			0.8	V
R_{DH}	Output impedance (high state)	(2)	28		43	Ω
R_{DL}	Output impedance (low state)	(2)	28		43	Ω
I_L	Input leakage current	V_{DD} = 3.6 V		±0.1	±5	µA
I_{OZ}	3-state output OFF state current	$V_I = V_{IH}$ or V_{IL}			±10	µA
V_{CR}	Crossover point		1.3		2	V
t_{RISE}	Rise time		4		20	ns
t_{FALL}	Fall time		4		20	ns

1. Temperature range = –45°C to 85°C.
2. *This value includes an external resistor of 24Ω±1%.*

Figure 100. Input to output disable / enable

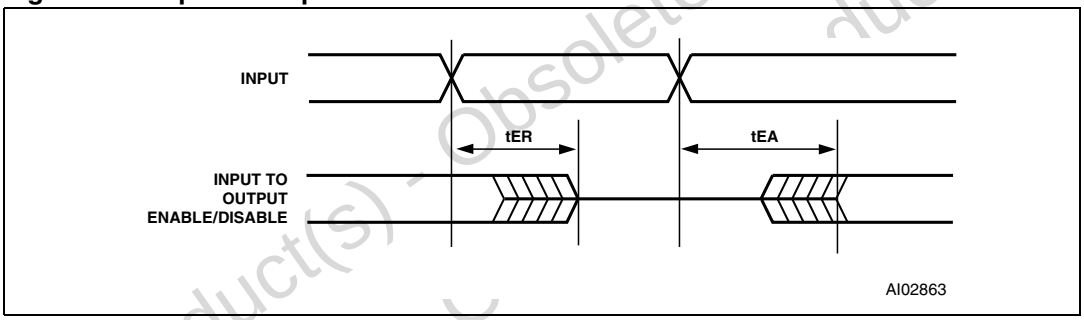
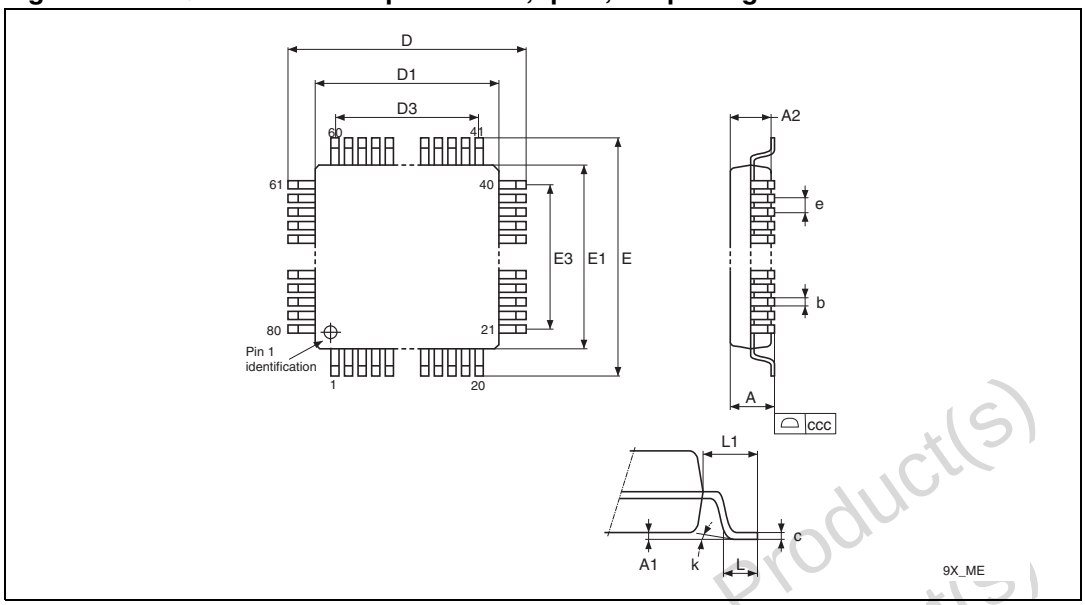


Figure 114. LQFP80 – 80-lead plastic thin, quad, flat package outline



1. Drawing is not to scale.

Table 238. LQFP80 – 80-lead plastic thin, quad, flat package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.090	0.200		0.0035	0.0079
D	14.000			0.5512		
D1	12.000			0.4724		
D3	9.500			0.3740		
E	14.000			0.5512		
E1	12.000			0.4724		
E3	9.500			0.3740		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k		0°	7°		0°	7°
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.