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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3434e-40u6

Table 5. SFR memory map with direct address and reset value (continued)

SFR addr (hex)	SFR name	Bit name and <bit address>								Reset value (hex)	Reg. descr. with link
		7	6	5	4	3	2	1	0		
F9	CCON0	PLLM[4]	PLLEN	UPLLCE	DBGCE	CPU_AR	CPUPS[2:0]			50	*Table 27*
FA	CCON1	PLLM[3:0]				PLLD[3:0]				00	
FB	CCON2	–	–	–	PCA0CE	PCA0PS[3:0]				10	*Table 144*
FC	CCON3	–	–	–	PCA1CE	PCA1PS[3:0]				10	*Table 146*
FD	RESERVED										
FE	RESERVED										
FF	RESERVED										
FE	RESERVED										
FF	RESERVED										

1. This SFR can be addressed by individual bits (bit address mode) or addressed by the entire byte (direct address mode).

14 MCU clock generation

Internal system clocks generated by the clock generation unit are derived from the signal, XTAL1, shown in *Figure 13*. XTAL1 has a frequency f_{OSC}, which comes directly from the external crystal or oscillator device. The SFR named CCON0 (*Table 27 on page 70*) controls the clock generation unit.

There are two clock signals produced by the clock generation unit:

- MCU_CLK
- PERIPH_CLK

14.1 MCU_CLK

This clock drives the 8032 MCU core and the Watchdog Timer (WDT). The frequency of MCU_CLK is equal to f_{OSC} by default, but it can be divided by as much as 2048, shown in *Figure 13*. The bits CPUPS[2:0] select one of eight different divisors, ranging from 2 to 2048. The new frequency is available immediately after the CPUPS[2:0] bits are written. The final frequency of MCU_CLK is f_{MCU}.

MCU_CLK is blocked by either bit, PD or IDL, in the SFR named PCON during MCU Power-down mode or Idle mode respectively.

MCU_CLK clock can be further divided as required for use in the WDT. See details of the WDT in *Section 19: Supervisory functions on page 91*.

14.2 PERIPH_CLK

This clock drives all the UPSD34xx peripherals except the WDT. The Frequency of PERIPH_CLK is always f_{OSC}. Each of the peripherals can independently divide PERIPH_CLK to scale it appropriately for use.

PERIPH_CLK runs at all times except when blocked by the PD bit in the SFR named PCON during MCU Power-down mode.

14.2.1 JTAG interface clock

The JTAG interface for ISP and for Debugging uses the externally supplied JTAG clock, coming in on pin TCK. This means the JTAG ISP interface is always available, and the JTAG Debug interface is available when enabled, even during MCU Idle mode and Power-down mode.

However, since the MCU participates in the JTAG debug process, and MCU_CLK is halted during Idle and Power-down modes, the majority of debug functions are not available during these low power modes. But the JTAG debug interface is capable of executing a reset command while in these low power modes, which will exit back to normal operating mode where all debug commands are available again.

The CCON0 SFR contains a bit, DBGCE, which enables the breakpoint comparators inside the JTAG Debug Unit when set. DBGCE is set by default after reset, and firmware may clear this bit at run-time. Disabling these comparators will reduce current consumption on the MCU module, and it is recommended to do so if the Debug Unit will not be used (such as in the production version of an end-product).

Table 45. P1SFS0 and P1SFS1 details (continued)

Port 1 Pin	R/W	Default port function	Alternate 1 port function	Alternate 2 port function
		P1SFS0[i] = 0 P1SFS1[i] = x	P1SFS0[i] = 1 P1SFS1[i] = 0	P1SFS0[i] = 1 P1SFS1[i] = 1
		Port 1 Pin, i = 0.. 7	Port 1 Pin, i = 0.. 7	Port 1 Pin, i = 0.. 7
6	R,W	GPIO	SPI Transmit, SPITXD	ADC Chn 6 input, ADC6
7	R,W	GPIO	SPI Select, SPISEL_	ADC Chn 7 input, ADC7

Table 46. P4SFS0: Port 4 special function select 0 register (SFR 92h, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4SF07	P4SF06	P4SF05	P4SF04	P4SF03	P4SF02	P4SF01	P4SF00

Table 47. P4SFS1: Port 4 special function select 1 register (SFR 93h, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4SF17	P4SF16	P4SF15	P4SF14	P4SF13	P4SF12	P4SF11	P4SF10

Table 48. P4SFS0 and P4SFS1 details

Port 4 pin	R/W	Default port function	Alternate 1 port function	Alternate 2 port function
		P4SFS0[i] = 0 P4SFS1[i] = x	P4SFS0[i] = 1 P4SFS1[i] = 0	P4SFS0[i] = 1 P4SFS1[i] = 1
		Port 4 Pin, i = 0.. 7	Port 4 Pin, i = 0.. 7	Port 4 Pin, i = 0.. 7
0	R,W	GPIO	PCA0 Module 0, TCM0	Timer 2 count input, T2
1	R,W	GPIO	PCA0 Module 1, TCM1	Timer 2 trigger input, TX2
2	R,W	GPIO	PCA0 Module 2, TCM2	UART1 Receive, RXD1
3	R,W	GPIO	PCA0 ext clock, PCACLK0	UART1 Transmit, TXD1
4	R,W	GPIO	PCA1 Module 3, TCM3	SPI Clock, SPICLK
5	R,W	GPIO	PCA1 Module 4, TCM4	SPI Receive, SPIRXD
6	R,W	GPIO	PCA1 Module 5, TCM5	SPI Transmit, SPITXD
7	R,W	GPIO	PCA1 ext clock, PCACLK1	SPI Select, SPISEL_

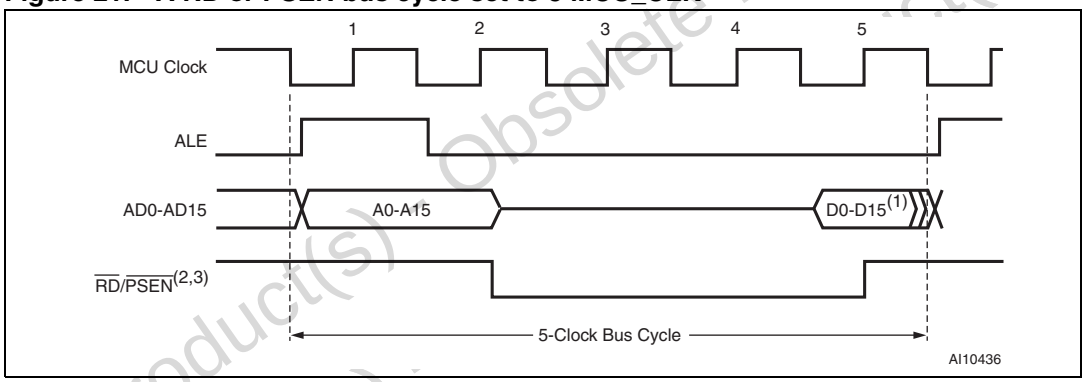
It is not possible to specify in the BUSCON register a different number of MCU_CLK periods for various address ranges. For example, the user cannot specify 4 MCU_CLK periods for RD read cycles to one address range on the PSD module, and 5 MCU_CLK periods for RD read cycles to a different address range on an external device. However, the user can specify one number of clock periods for PSEN read cycles and a different number of clock periods for RD or WR cycles (see *Figure 21 on page 88*).

18.5 Controlling the PFQ and BC

The BUSCON register allows firmware to enable and disable the PFQ and BC at run-time. Sometimes it may be desired to disable the PFQ and BC to ensure deterministic execution. The dynamic action of the PFQ and BC may cause varying program execution times depending on the events that happen prior to a particular section of code of interest. For this reason, it is not recommended to implement timing loops in firmware, but instead use one of the many hardware timers in the UPSD34xx. By default, the PFQ and BC are enabled after a reset condition.

Important note: Disabling the PFQ or BC will seriously reduce MCU performance.

Figure 21. A RD or PSEN bus cycle set to 5 MCU_CLK



1. The PSEN cycle is 16-bit, while the RD cycle is 8-bit only.
2. A PSEN bus cycle in progress may be aborted before completion if the PFQ and Branch Cache (BC) determines the current code fetch cycle is not needed.
3. Whenever the same number of MCU_CLK periods is specified in BUSCON for both PSEN and RD cycles, the bus cycle timing is typically identical for each of these types of bus cycles. In this case, the only time PSEN read cycles are longer than RD read cycles is when the PFQ issues a stall while reloading. PFQ stalls do not affect RD read cycles. By comparison, in many traditional 8051 architectures, RD bus cycles are always longer than PSEN bus cycles.

Table 49. BUSCON: bus control register (SFR 9Dh, reset value EBh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EPFQ	EBC	WRW[1:0]		RDW[1:0]		CW[1:0]	

period (12 / $f_{OSC,}$ seconds). However, if MCU_CLK is divided by the SFR CCON0, then the sample period must be calculated based on the resultant, longer, MCU_CLK frequency. In this case, an external clock signal on pins C0, C1, or T2 should have a duration longer than one MCU machine cycle, t_{MACH_CYC}. *Section 19.5: Watchdog timer, WDT on page 92* explains how to estimate t_{MACH_CYC}.

Table 56. TCON: Timer control register (SFR 88h, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 57. TCON register bit definition

Bit	Symbol	R/W	Definition
7	TF1	R	Timer 1 overflow interrupt flag. Set by hardware upon overflow. Automatically cleared by hardware after firmware services the interrupt for Timer 1.
6	TR1	R,W	Timer 1 run control. 1 = Timer/Counter 1 is on, 0 = Timer/Counter 1 is off.
5	TF0	R	Timer 0 overflow interrupt flag. Set by hardware upon overflow. Automatically cleared by hardware after firmware services the interrupt for Timer 0.
4	TR0	R,W	Timer 0 run control. 1 = Timer/Counter 0 is on, 0 = Timer/Counter 0 is off.
3	IE1	R	Interrupt flag for external interrupt pin, EXTINT1. Set by hardware when edge is detected on pin. Automatically cleared by hardware after firmware services EXTINT1 interrupt.
2	IT1	R,W	Trigger type for external interrupt pin EXTINT1. 1 = falling edge, 0 = low-level
1	IE0	R	Interrupt flag for external interrupt pin, EXTINT0. Set by hardware when edge is detected on pin. Automatically cleared by hardware after firmware services EXTINT0 interrupt.
0	IT0	R,W	Trigger type for external interrupt pin EXTINT0. 1 = falling edge, 0 = low-level

20.3 SFR, TCON

Timer 0 and Timer 1 share the SFR, TCON, that controls these timers and provides information about them. See *Table 56 on page 97*.

Bits IE0 and IE1 are not related to Timer/Counter functions, but they are set by hardware when a signal is active on one of the two external interrupt pins, EXTINT0 and EXTINT1. For system information on all of these interrupts, see *Table 17 on page 63*, Interrupt Summary.

Bits IT0 and IT1 are not related to Timer/Counter functions, but they control whether or not the two external interrupt input pins, EXTINT0 and EXTINT1 are edge or level triggered.

23 I²C interface

UPSD34xx devices support one serial I²C interface. This is a two-wire communication channel, having a bidirectional data signal (SDA, pin P3.6) and a clock signal (SCL, pin P3.7) based on open-drain line drivers, requiring external pull-up resistors, R_P, each with a typical value of 4.7kΩ (see *Figure 40*).

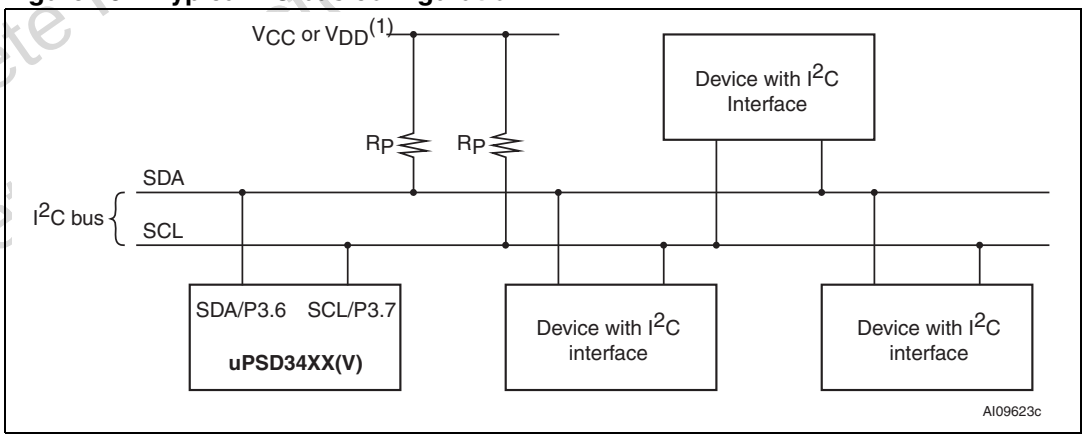
23.1 I²C interface main features

Byte-wide data is transferred, MSB first, between a Master device and a Slave device on two wires. More than one bus Master is allowed, but only one Master may control the bus at any given time. Data is not lost when another Master requests the use of a busy bus because I²C supports collision detection and arbitration. The bus Master initiates all data movement and generates the clock that permits the transfer. Once a transfer is initiated by the Master, any device addressed is considered a Slave. Automatic clock synchronization allows I²C devices with different bit rates to communicate on the same physical bus. A single device can play the role of Master or Slave, or a single device can be a Slave only. Each Slave device on the bus has a unique address, and a general broadcast address is also available. A Master or Slave device has the ability to suspend data transfers if the device needs more time to transmit or receive data.

This I²C interface has the following features:

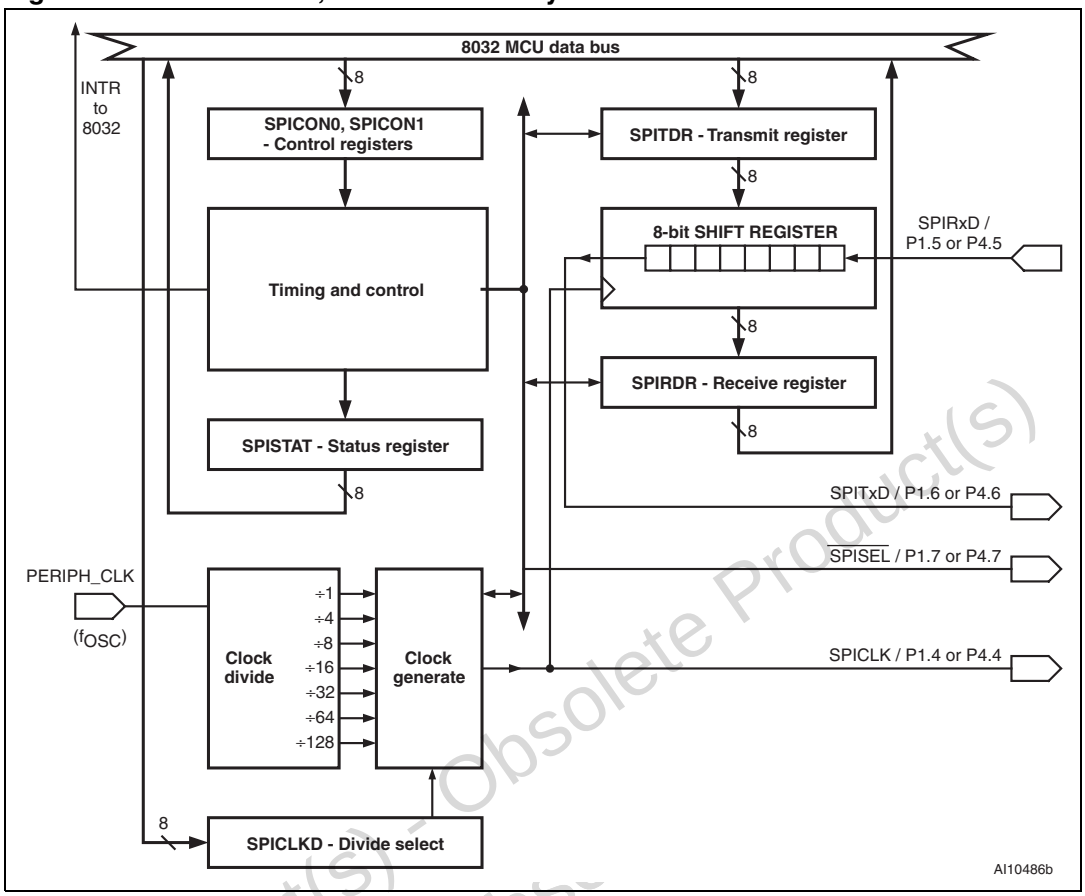
- Serial I/O Engine (SIOE): serial/parallel conversion; bus arbitration; clock generation and synchronization; and handshaking are all performed in hardware
- Interrupt or Polled operation
- Multi-master capability
- 7-bit Addressing
- Supports standard speed I²C (SCL up to 100kHz), fast mode I²C (101KHz to 400kHz), and high-speed mode I²C (401KHz to 833kHz)

Figure 40. Typical I²C bus configuration



1. For 3.3 V system, connect R_P to 3.3 V V_{CC}. For 5.0 V system, connect R_P to 5.0 V V_{DD}.

Figure 47. SPI interface, master mode only



24.5 SPI configuration

The SPI interface is reset by the MCU reset, and firmware needs to initialize the SFRs SPICON0, SPICON1, and SPICLKD to define several operation parameters.

The SPO Bit in SPICON0 determines the clock polarity. When SPO is set to '0,' a data bit is transmitted on SPITxD from one rising edge of SPICLK to the next and is guaranteed to be valid during the falling edge of SPICLK. When SPO is set to '1,' a data bit is transmitted on SPITxD from one falling edge of SPICLK to the next and is guaranteed to be valid during the rising edge of SPICLK. The UPSD34xx will sample received data on the appropriate edge of SPICLK as determined by SPO. The effect of the SPO Bit can be seen in *Figure 45* and *Figure 46 on page 145*.

The FLSB Bit in SPICON0 determines the bit order while transmitting and receiving the 8-bit data. When FLSB is '0,' the 8-bit data is transferred in order from MSB (first) to LSB (last). When FLSB Bit is set to '1,' the data is transferred in order from LSB (first) to MSB (last).

The clock signal generated on SPICLK is derived from the internal PERIPH_CLK signal. PERIPH_CLK always operates at the frequency, f_{OSC}, and runs constantly except when stopped in MCU Power Down mode. SPICLK is a result of dividing PERIPH_CLK by a sum of different divisors selected by the value contained in the SPICLKD register. The default value in SPICLKD after a reset divides PERIPH_CLK by a factor of 4. The bits in SPICLKD can be set to provide resulting divisor values in of sums of multiples of 4, such as 4, 8, 12,

25.2 Types of transfers

The USB specification defines four types of transfers, Bulk, Interrupt, Isochronous, and Control.

Note: The UPSD34xx supports all types of transfers except Isochronous.

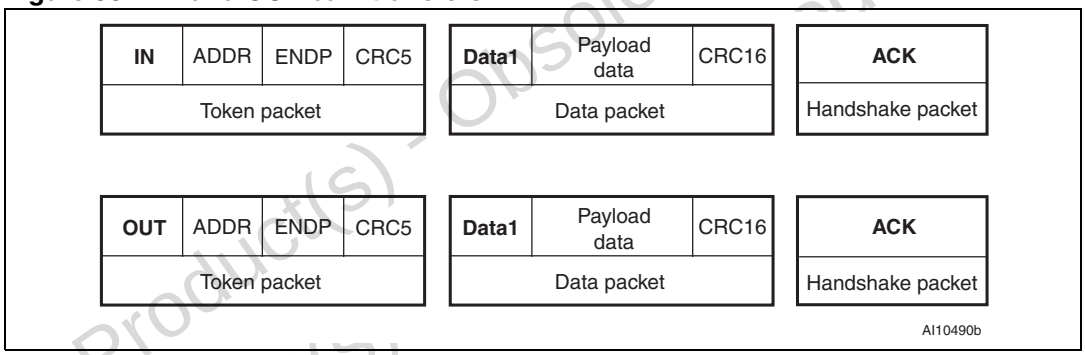
- Bulk Transfers (see *Figure 50*)

  Bulk data is transferred in both directions and is used with both IN and OUT endpoints. Packets may be 8, 16, 32, or 64 bytes in length. Bulk transfers occur in bursts, and are scheduled by the host when there is available time on the bus. While there is no guaranteed delivery time for bulk transfers, the accuracy of the data is guaranteed due to automatic retries for erroneous data. Bulk transfers are typically used for mass storage, printer, and scanner data.

- Interrupt Transfers (see *Figure 51*)

  Interrupt data is a lot like bulk data but travels only in one direction, from the device to the host, so only IN endpoints are used. Interrupt data holds packet sizes ranging from 1 to 64 bytes. Interrupt endpoints have an associated polling interval, meaning that the host sends IN tokens at a periodic interval to the host on a regular basis. Interrupt transfers are typically used for human interface devices such as keyboards, mice, and joysticks.

Figure 50. IN and OUT bulk transfers



26 Analog-to-digital convertor (ADC)

The ADC unit in the UPSD34xx is a SAR type ADC with an SAR register, an auto-zero comparator and three internal DACs. The unit has 8 input channels with 10-bit resolution. The A/D converter has its own AV_{REF} input (80-pin package only), which specifies the voltage reference for the A/D operations. The analog to digital converter (A/D) allows conversion of an analog input to a corresponding 10-bit digital value. The A/D module has eight analog inputs (P1.0 through P1.7) to an 8x1 multiplexor. One ADC channel is selected by the bits in the configuration register. The converter generates a 10-bits result via successive approximation. The analog supply voltage is connected to the AV_{REF} input, which powers the resistance ladder in the A/D module.

The A/D module has 3 registers, the control register ACON, the A/D result register ADAT0, and the second A/D result register ADAT1. The ADAT0 register stores Bits 0.. 7 of the converter output, Bits 8.. 9 are stored in Bits 0..1 of the ADAT1 register. The ACON register controls the operation of the A/D converter module. Three of the bits in the ACON register select the analog channel inputs, and the remaining bits control the converter operation.

ADC channel pin input is enabled by setting the corresponding bit in the P1SFS0 and P1SFS1 registers to '1' and the channel select bits in the ACON register.

The ADC reference clock (ADCCLK) is generated from f_{OSC} divided by the divider in the ADCPS register. The ADC operates within a range of 2 to 16MHz, with typical ADCCLK frequency at 8MHz.

The conversion time is 4µs typical at 8MHz.

The processing of conversion starts when the Start Bit ADST is set to '1.' After one cycle, it is cleared by hardware. The ADC is monotonic with no missing codes. Measurement is by continuous conversion of the analog input. The ADAT register contains the results of the A/D conversion. When conversion is complete, the result is loaded into the ADAT. The A/D Conversion Status Bit ADSF is set to '1.' The block diagram of the A/D module is shown in *Figure 56*. The A/D status bit ADSF is set automatically when A/D conversion is completed and cleared when A/D conversion is in process.

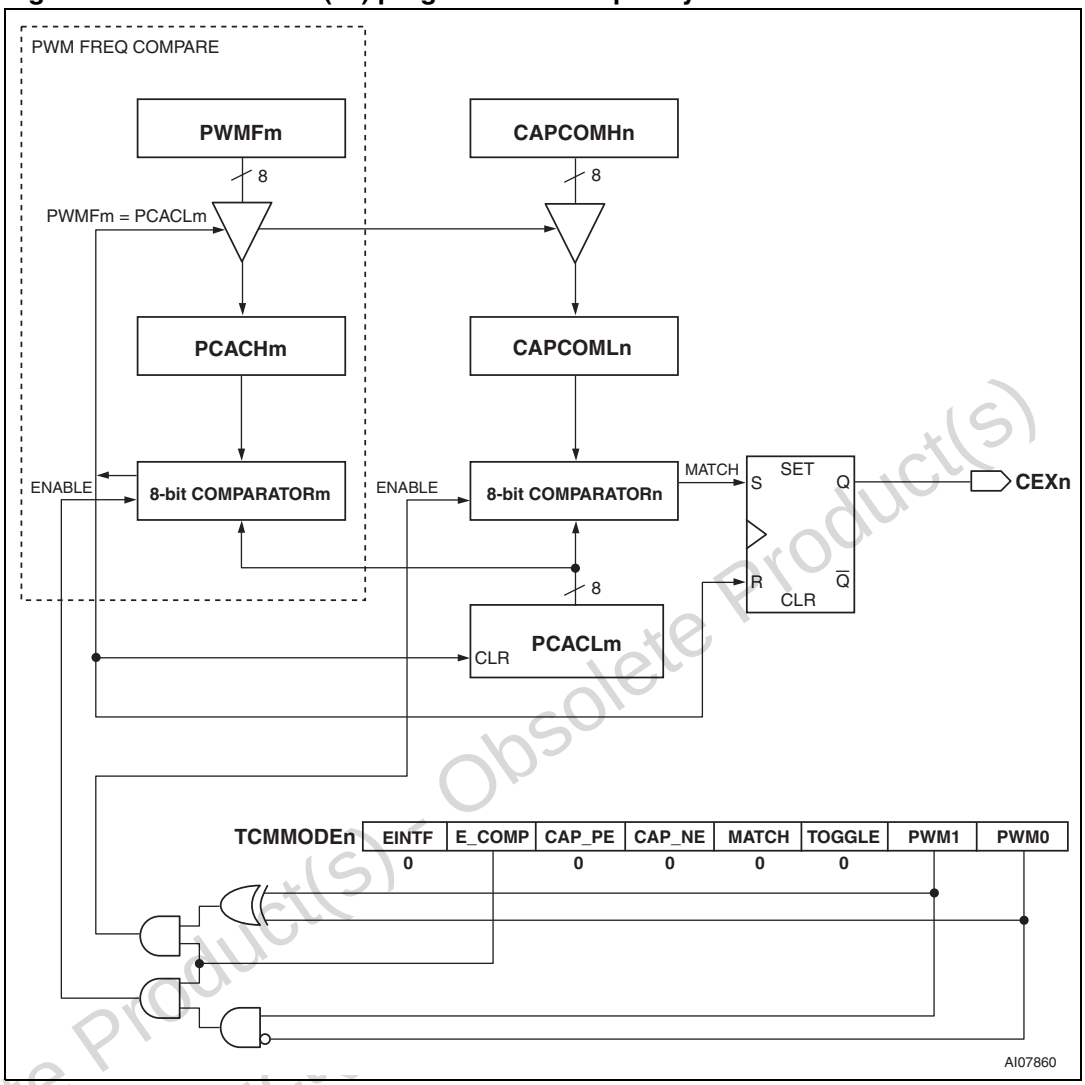
In addition, the ADC unit sets the interrupt flag in the ACON register after a conversion is complete (if AINTEN is set to '1'). The ADC interrupts the CPU when the enable bit AINTEN is set.

26.1 Port 1 ADC channel selects

The P1SFS0 and P1SFS1 registers control the selection of the Port 1 pin functions. When the P1SFS0 Bit is '0,' the pin functions as a GPIO. When bits are set to '1,' the pins are configured as alternate functions. A new P1SFS1 register selects which of the alternate functions is enabled. The ADC channel is enabled when the bit in P1SFS1 is set to '1.'

Note: In the 52-pin package, there is no individual AV_{REF} pin because AV_{REF} is combined with AV_{CC} pin.

Figure 60. PWM mode - (x8) programmable frequency



1. m = 0: n = 0, 1, or 2
   m = 1: n = 3, 4, or 5

27.9 PWM mode - fixed frequency, 16-bit

The operation of the 16-bit PWM is the same as the 8-bit PWM with fixed frequency. In this mode, one or all the TCM can be configured to have a fixed frequency PWM output on the port pins. The PWM frequency is depending on the clock input frequency to the 16-bit Counter. The duty cycle of each TCM module can be specified in the CAPCOMHn and CAPCOMLn registers. When the 16-bit PCA_Counter is equal or greater than the values in registers CAPCOMHn and CAPCOMLn, the PWM output is switched to a high state. When the PCA_Counter overflows, CEXn is asserted low.

Note: The 8032 data bus, D0 - D7, does not route directly to PLD inputs. Instead, the 8032 data bus has indirect access to the GPLD (not the DPLD) when the 8032 reads and writes the OMC and IMC registers within csiop address space.

28.5.26 Turbo bit and PLDs

The PLDs can minimize power consumption by going to standby after ALL the PLD inputs remain unchanged for an extended time (about 70ns). When the Turbo Bit is set to logic one (Bit 3 of the csiop PMMR0 register), Turbo mode is turned off and then this automatic standby mode is achieved. Turning off Turbo mode increases propagation delays while reducing power consumption. The default state of the Turbo Bit is logic zero, meaning Turbo mode is on. Additionally, four bits are available in the csiop PMMR0 and PMMR2 registers to block the 8032 bus control signals ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE) from entering the PLDs. This reduces power consumption and can be used only when these 8032 control signals are not used in PLD logic equations. See *Section 28.5.52: Power management on page 248*.

Table 167. DPLD and GPLD inputs

Input source	Input name	Number of signals
8032 address bus	A0-A15	16
8032 bus control signals	$\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$, ALE	4
Reset from MCU module	$\overline{RESET}$	1
Power-Down from Auto-Power Down counter	PDN	1
PortA input macrocells (80-pin devices only)	PA0-PA7	8
PortB input macrocells	PB0-PB7	8
PortC input macrocells	PC2, PC3, PC4, PC7	4
Port D inputs (52-pin devices have only PD1)	PD1, PD2	2
Page register	PGR0-PGR7	8
Macrocell OMC bank AB Feedback	MCELLAB FB0-7	8
Macrocell OMC bank BC Feedback	MCELLBC FB0-7	8
Flash memory status bit	Ready/$\overline{Busy}$	1

Table 189. MCU I/O mode port D direction register (address = csiop + offset 15h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	N/A	PD2(3)	PD1	N/A

1. For each bit, 1 = out from UPSD34xx port pin1, 0 = in to PSD34xx port pin.
2. Default state for register is 00h after reset or power-up.
3. Not available on 52-pin uPSD34xx devices.

28.5.39 PLD I/O mode

Pins on Ports A, B, C, and D can serve as inputs to either the DPLD or the GPLD. Inputs to these PLDs from Ports A, B, and C are routed through IMCs before reaching the PLD input bus. Inputs to the PLDs from Port D do not pass through IMCs, but route directly to the PLD input bus.

Pins on Ports A, B, and C can serve as outputs from GPLD OMCs, and Port D pins can be outputs from the DPLD (external chip-selects) which do not consume OMCs.

Whenever a pin is specified to be a PLD output, it cannot be used for MCU I/O mode, or other pin modes. If a pin is specified to be a PLD input, it is still possible to read the pin using MCU I/O input mode with the csiop register Data In. Also, the csiop Direction register can still affect a pin which is used for a PLD input. The csiop Data Out register has no effect on a PLD output pin.

Each pin on Ports A, B, C, and D have a tri-state buffer at the final output stage. The Output Enable signal for this buffer is driven by the logical OR of two signals. One signal is an Output Enable signal generated by the AND-OR array (from an .oe equation specified in PSDsoft), and the other signal is the output of the csiop Direction register. This logic is shown in *Figure 79 on page 232*. At power-on, all port pins default to high-impedance input (Direction registers default to 00h). However, if an equation is written for the Output Enable that is active at power-on, then the pin will behave as an output.

PLD I/O equations are specified in PSDsoft Express and programmed into the uPSD using JTAG. *Figure 80* shows a very simple combinatorial logic example which is implemented on pins of Port B.

To give a general idea of how PLD logic is implemented using PSDsoft Express, *Figure 81 on page 237* illustrates the pin declaration window of PSDsoft Express, showing the PLD output at pin PB0 declared as “Combinatorial” in the “PLD Output” section, and a signal name, “pld_out”, is specified. The other three signals on pins PB1, PB2, and PB3 would be declared as “Logic or Address” in the “PLD Input” section, and given signal names.

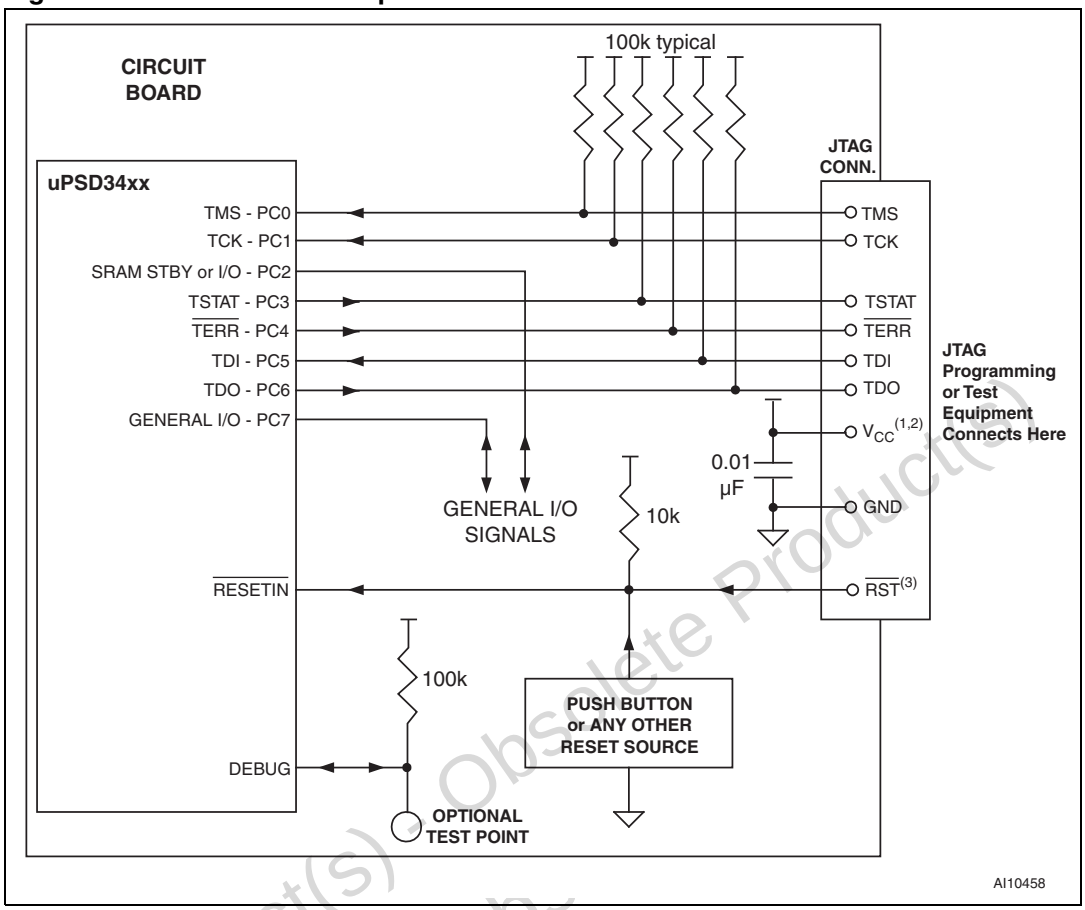
In the “Design Assistant” window of PSDsoft Express shown in *Figure 82 on page 238*, the user simply enters the logic equation for the signal “pld_out” as shown. The user can either type in the logic statements or enter them using a point-and-click method, selecting various signal names and logic operators available in the window.

After PSDsoft Express has accepted and realized the logic from the equations, it synthesizes the logic statement:

pld_out = (pld_in_1 # pld_in_2) & !pld_in_3;

to be programmed into the GPLD. See the PSDsoft User’s Manual for all the steps.

Figure 92. Recommended 6-pin JTAG connections



1. For 5 V UPSD34xx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 5 V system V_{DD}.
2. For 3.3 V UPSD34xx devices, pull-up resistors and V_{CC} pin on the JTAG connector should be connected to 3.3 V system V_{CC}.
3. This signal is driven by an Open-Drain output in the JTAG equipment, allowing more than one source to activate RESET_IN.

28.6.6 Recommended JTAG connector

There is no industry standard JTAG connector. STMicroelectronics recommends a specific JTAG connector and pinout for uPSD3xxx so programming and debug equipment will easily connect to the circuit board. The user does not have to use this connector if there is a different connection scheme.

The recommended connector scheme can accept a standard 14-pin ribbon cable connector (2 rows of 7 pins on 0.1” centers, 0.025” square posts, standard keying) as shown in *Figure 93*. See the STMicroelectronics “FlashLINK, FL-101 User Manual” for more information.

31 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 206. Operating conditions (5 V devices)

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage	4.5	5.5	V
V_{CC}, AV_{CC}	Supply voltage	3.0	3.6	V
T_A	Ambient operating temperature (industrial)	–40	85	°C
	Ambient operating temperature (commercial)	0	70	°C

Table 207. Operating conditions (3.3 V devices)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}, V_{DD}, AV_{CC}	Supply voltage	3.0	3.6	V
T_A	Ambient operating temperature (industrial)	–40	85	°C
	Ambient operating temperature (commercial)	0	70	°C

Table 208. AC signal letters for timing

Letter	Meaning
A	Address
C	Clock
D	Input data
I	Instruction
L	ALE
N	$\overline{\text{RESET}}$ input or output
P	$\overline{\text{PSEN}}$ signal
Q	Output data
R	RD signal
W	WR signal
M	Output Macrocell

Note: Example: t_{AVLX} = time from address valid to ALE invalid.

Figure 98. External READ cycle (80-pin device only)

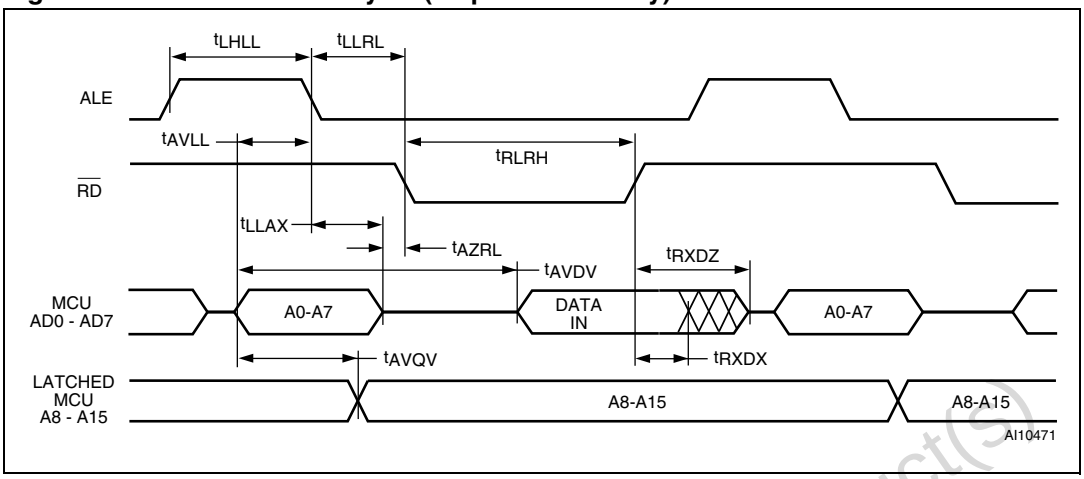


Table 214. External READ cycle AC characteristics (3 V or 5 V device)

Symbol	Parameter	40 MHz oscillator(1)		Variable oscillator $1/t_{CLCL}$ = 3 to 40 MHz		Unit
		Min	Max	Min	Max	
t_{LHLL}	ALE pulse width	17		$t_{CLCL} - 8$		ns
t_{AVLL}	Address setup to ALE	13		$t_{CLCL} - 12$		ns
t_{LLAX}	Address hold after ALE	7.5		$0.5t_{CLCL} - 5$		ns
t_{LLRL}	ALE to $\overline{RD}$	7.5		$0.5t_{CLCL} - 5$		ns
t_{RLRH}	$\overline{RD}$ pulse width(2)	40		$nt_{CLCL} - 10$		ns
t_{RXIX}	Input data hold after $\overline{RD}$	2		2		ns
t_{RHIZ}	Input data float after $\overline{RD}$		10.5		$0.5t_{CLCL} - 2$	ns
t_{AVDX}	Address to valid data in(2)		70		$mt_{CLCL} - 5$	ns
t_{AZRL}	Address float to $\overline{RD}$	–2		–2		ns
t_{AVQV}	Address valid to latched address out on Ports A and B		35.5 (3 V)		$1.5t_{CLCL} - 2$	ns
			28 (5 V)		$t_{CLCL} - 9.5$	ns

1. BUSCON register is configured for 4 PFQCLK.
2. Refer to *Table 215* for “n” and “m” values.

Table 215. n, m, and x, y values

# of PFQCLK in BUSCON register	READ cycle		WRITE cycle	
	n	m	x	y
4	2	3	2	1
5	3	4	3	2
6	4	5	4	3
7	5	6	5	4

Figure 101. Synchronous Clock mode timing – PLD

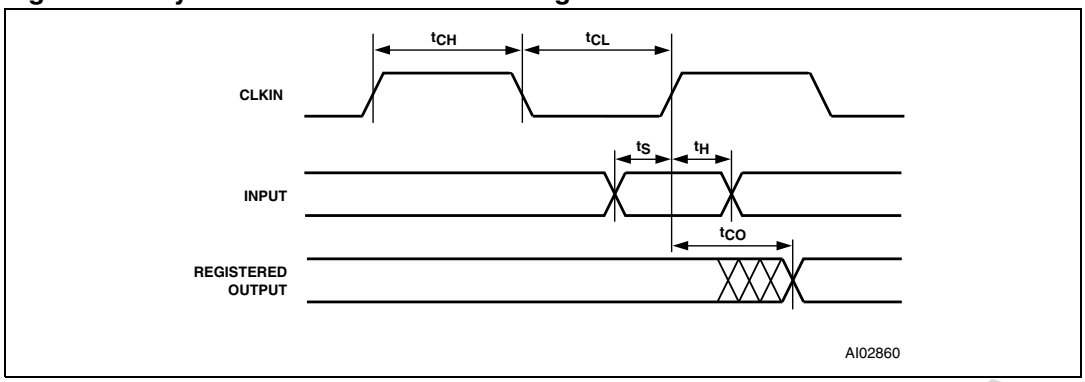


Table 222. CPLD macrocell synchronous clock mode timing (5 V PSD module)

Symbol	Parameter	Conditions	Min	Max	PT Aloc	Turbo Off	Slew rate(1)	Unit
f_{MAX}	Maximum frequency external feedback	$1/(t_S+t_{CO})$		40.0				MHz
	Maximum frequency internal feedback (f_{CNT})	$1/(t_S+t_{CO}-10)$		66.6				MHz
	Maximum frequency pipelined data	$1/(t_{CH}+t_{CL})$		83.3				MHz
t_S	Input setup time		12		+ 2	+ 10		ns
t_H	Input hold time		0					ns
t_{CH}	Clock high time	Clock input	6					ns
t_{CL}	Clock low time	Clock input	6					ns
t_{CO}	Clock to output delay	Clock input		13			– 2	ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns
t_{MIN}	Minimum clock period(2)	$t_{CH}+t_{CL}$	12					ns

1. Fast slew rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount.
2. CLKIN (PD1) $t_{CLCL} = t_{CH} + t_{CL}$.

Figure 110. External clock cycle

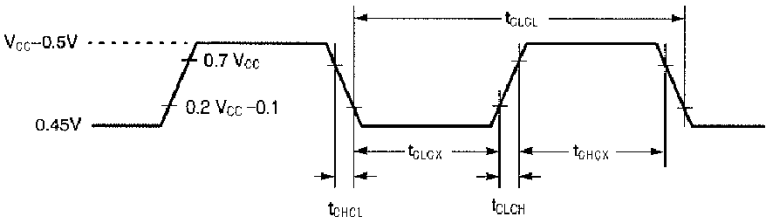


Figure 111. PSD module AC measurement I/O waveform

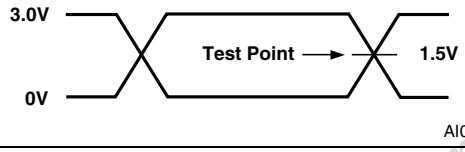


Figure 112. PSD module AC measurement load circuit

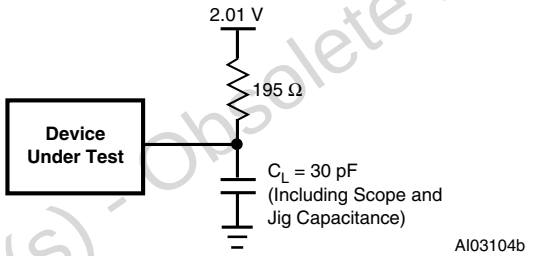


Table 236. I/O pin capacitance

Symbol	Parameter((1)	Test condition	Typ.(2)	Max.	Unit
C_{IN}	Input capacitance (for input pins)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Output capacitance (for input/output pins)(3)	V_{OUT} = 0 V	8	12	pF

1. Sampled only, not 100% tested.
2. Typical values are for T_A = 25 °C and nominal supply voltages.
3. Maximum for MCU Address and Data lines is 20 pF each.

32 Package mechanical information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.