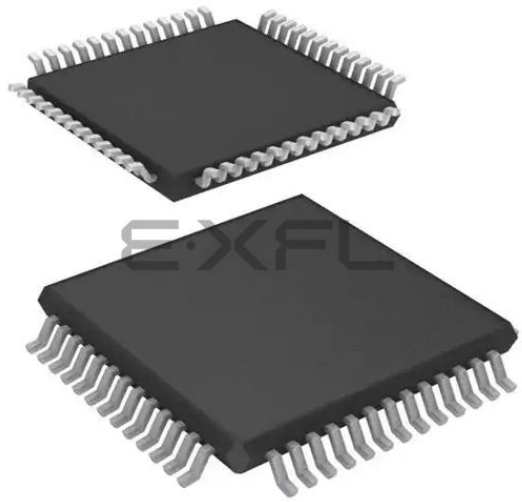

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3434ev-40t6

6 MCU module description

This following sections provide a detailed description of the MCU module system functions and peripherals, including:

- 8032 MCU registers
- Special function registers
- 8032 addressing modes
- UPSD34xx instruction set summary
- Dual data pointers
- Debug unit
- Interrupt system
- MCU clock generation
- Power saving modes
- Oscillator and external components
- I/O ports
- MCU bus interface
- Supervisory functions
- Standard 8032 timer/counters
- Serial UART interfaces
- IrDA interface
- I^2C interface
- SPI interface
- Analog to digital converter
- Programmable counter array (PCA)
- USB interface

Table 5. SFR memory map with direct address and reset value (continued)

SFR addr (hex)	SFR name	Bit name and <bit address>								Reset value (hex)	Reg. descr. with link
		7	6	5	4	3	2	1	0		
94	ADCPS	–	–	–	–	ADCCE	ADCPS[2:0]			00	Table 140
95	ADAT0	ADATA[7:0]								00	Table 141
96	ADAT1	–	–	–	–	–	–	ADATA[9:8]		00	Table 142
97	ACON	AINTF	AINTEN	ADEN	ADS[2:0]			ADST	ADSF	00	Table 138
98(1)	SCON0	SM0 <9Fh>	SM1 <9Eh>	SM2 <9Dh>	REN <9Ch>	TB8 <9Bh>	RB8 <9Ah>	TI <99h>	RI <9h8>	00	Table 65
99	SBUF0	SBUF0[7:0]								00	Section 21
9A	RESERVED										
9B	RESERVED										
9C	RESERVED										
9D	BUSCON	EPFQ	EBC	WRW1	WRW0	RDW1	RDW0	CW1	CW0	EB	Table 49
9E	RESERVED										
9F	RESERVED										
A0	RESERVED										
A1	RESERVED										
A2	PCACL0	PCACL0[7:0]								00	Table 143
A3	PCACH0	PCACH0[7:0]								00	Table 143
A4	PCACON0	EN_ALL	EN_PCA	EOVF1	PCA_IDL	–	–	CLK_SEL[1:0]		00	Table 148
A5	PCASTA	OVF1	INTF5	INTF4	INTF3	OVF0	INTF2	INTF1	INTF0	00	Table 152
A6	WDRST	WDRST[7:0]								00	Table 54
A7	IEA	EADC	ESPI	EPCA	ES1	–	–	EI2C	–	00	Table 20
A8(1)	IE	EA <AFh>	–	ET2 <ADh>	ES0 <ACh>	ET1 <ABh>	EX1 <AAh>	ET0 <A9h>	EX0 <A8h>	00	Table 18
A9	TCMMODE0	EINTF	E_COMP	CAP_PE	CAP_NE	MATCH	TOGGLE	PWM[1:0]		00	Table 154
AA	TCMMODE1	EINTF	E_COMP	CAP_PE	CAP_NE	MATCH	TOGGLE	PWM[1:0]		00	
AB	TCMMODE2	EINTF	E_COMP	CAP_PE	CAP_NE	MATCH	TOGGLE	PWM[1:0]		00	
AC	CAPCOML0	CAPCOML0[7:0]								00	Table 143
AD	CAPCOMH0	CAPCOMH0[7:0]								00	
AE	WDKEY	WDKEY[7:0]								55	Table 52
AF	CAPCOML1	CAPCOML1[7:0]								00	Table 143

9.11 Bit addressing

This mode allows setting or clearing an individual bit without disturbing the other bits within an 8-bit value of internal SRAM. Bit Addressing is only available for certain locations in 8032 DATA and SFR memory. Valid locations are DATA addresses 20h - 2Fh and for SFR addresses whose base address ends with 0h or 8h. (Example: The SFR, IE, has a base address of A8h, so each of the eight bits in IE can be addressed individually at address A8h, A9h, ...up to AFh.) For example:

```
SETB AFh        ; Set the individual EA bit (Enable All ; Interrupts) inside the SFR register,
                ; IE.
```

20.6.1 Capture mode

In Capture mode there are two options which are selected by the bit EXEN2 in T2CON. *Figure 27 on page 105* illustrates Capture mode.

If EXEN2 = 0, then Timer 2 is a 16-bit timer if C/$\overline{T2}$ = 0, or it is a 16-bit counter if C/$\overline{T2}$ = 1, either of which sets the interrupt flag bit TF2 upon overflow.

If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input pin T2X causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2X causes interrupt flag bit EXF2 in T2CON to be set. Either flag TF2 or EXF2 will generate an interrupt and the MCU must read both flags to determine the cause. Flags TF2 and EXF2 are not automatically cleared by hardware, so the firmware servicing the interrupt must clear the flag(s) upon exit of the interrupt service routine.

20.6.2 Auto-reload mode

In the Auto-reload mode, there are again two options, which are selected by the bit EXEN2 in T2CON. *Figure 28 on page 106* shows Auto-reload mode.

If EXEN2 = 0, then when Timer 2 counts up and rolls over from FFFFh it not only sets the interrupt flag TF2, but also causes the Timer 2 registers to be reloaded with the 16-bit value contained in registers RCAP2L and RCAP2H, which are preset with firmware.

If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2X will also trigger the 16-bit reload and set the interrupt flag EXF2. Again, firmware servicing the interrupt must read both TF2 and EXF2 to determine the cause, and clear the flag(s) upon exit.

Note: The UPSD34xx does not support selectable up/down counting in Auto-reload mode (this feature was an extension to the original 8032 architecture).

Table 60. T2CON: Timer 2 control register (SFR C8h, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 61. T2CON register bit definition

Bit	Symbol	R/W	Definition
7	TF2	R,W	Timer 2 flag, causes interrupt if enabled. TF2 is set by hardware upon overflow. Must be cleared by firmware. TF2 will not be set when either RCLK or TCLK =1.
6	EXF2	R,W	Timer 2 flag, causes interrupt if enabled. EXF2 is set when a capture or reload is caused by a negative transition on T2X pin and EXEN2 = 1. EXF2 must be cleared by firmware.
5	RCLK(1)	R,W	UART0 Receive Clock control. When RCLK = 1, UART0 uses Timer 2 overflow pulses for its receive clock in Modes 1 and 3. RCLK=0, Timer 1 overflow is used for its receive clock

Table 73. Baud rate of UART#1 for IrDA interface

BR3	BR2	BR1	BR0	Baud rate (kbps)
0	0	0	0	115.2
0	0	0	1	57.5
0	0	1	0	38.4
0	0	1	1	19.2
0	1	0	0	14.4
0	1	0	1	12.8
0	1	1	0	9.6
0	1	1	1	7.2
1	0	0	0	4.8
1	0	0	1	3.6
1	0	1	0	2.4
1	0	1	1	1.8
1	1	0	0	1.2

22.2 Pulse width selection

The IrDA interface has two ways to modulate the standard UART1 serial stream:

1. An IrDA data pulse will have a constant pulse width for any bit time, regardless of the selected baud rate.
2. An IrDA data pulse will have a pulse width that is proportional to the the bit time of the selected baud rate. In this case, an IrDA data pulse width is 3/16 of its bit time, as shown in *Figure 39 on page 119*.

The PULSE bit in the SFR named IRDACON determines which method above will be used.

According to the IrDA physical layer specification, for all baud rates at 115.2k bps and below, the minimum data pulse width is 1.41µs. For a baud rate of 115.2k bps, the maximum pulse width 2.23µs. If a constant pulse width is to be used for all baud rates (PULSE bit = 0), the ideal general pulse width is 1.63µs, derived from the bit time of the fastest baud rate (8.68µs bit time for 115.2k bps rate), multiplied by the proportion, 3/16.

To produce this fixed data pulse width when the PULSE bit = 0, a prescaler is needed to generate an internal reference clock, SIRClk, shown in *Figure 38 on page 119*. SIRClk is derived by dividing the oscillator clock frequency, $f_{OSC,}$ using the five bits CDIV[4:0] in the SFR named IRDACON. A divisor must be chosen to produce a frequency for SIRClk that lies between 1.34 MHz and 2.13 MHz, but it is best to choose a divisor value that produces SIRClk frequency as close to 1.83MHz as possible, because SIRClk at 1.83MHz will produce an fixed IrDA data pulse width of 1.63µs. *Table 74* provides recommended values for CDIV[4:0] based on several different values of f_{OSC}.

For reference, SIRClk of 2.13MHz will generate a fixed IrDA data pulse width of 1.41 µs, and SIRClk of 1.34MHz will generate a fixed data pulse width of 2.23 µs.

23 I²C interface

UPSD34xx devices support one serial I²C interface. This is a two-wire communication channel, having a bidirectional data signal (SDA, pin P3.6) and a clock signal (SCL, pin P3.7) based on open-drain line drivers, requiring external pull-up resistors, R_P, each with a typical value of 4.7kΩ (see *Figure 40*).

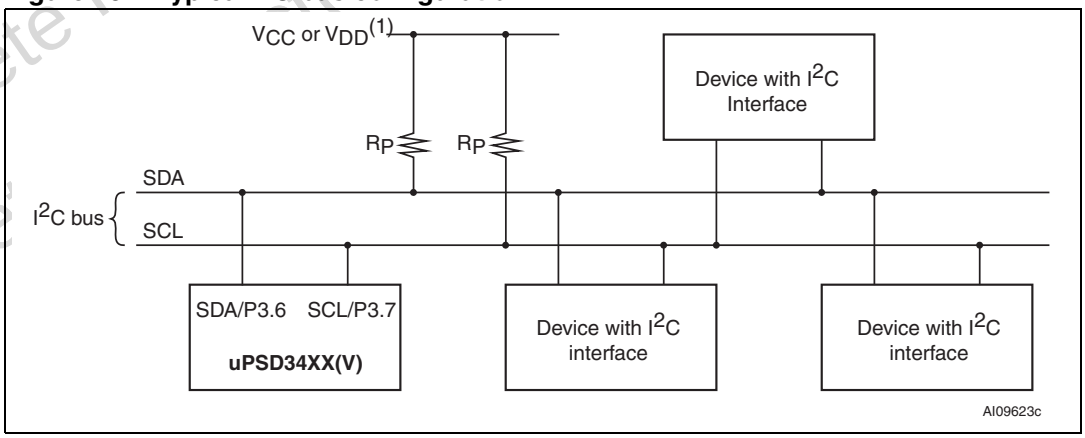
23.1 I²C interface main features

Byte-wide data is transferred, MSB first, between a Master device and a Slave device on two wires. More than one bus Master is allowed, but only one Master may control the bus at any given time. Data is not lost when another Master requests the use of a busy bus because I²C supports collision detection and arbitration. The bus Master initiates all data movement and generates the clock that permits the transfer. Once a transfer is initiated by the Master, any device addressed is considered a Slave. Automatic clock synchronization allows I²C devices with different bit rates to communicate on the same physical bus. A single device can play the role of Master or Slave, or a single device can be a Slave only. Each Slave device on the bus has a unique address, and a general broadcast address is also available. A Master or Slave device has the ability to suspend data transfers if the device needs more time to transmit or receive data.

This I²C interface has the following features:

- Serial I/O Engine (SIOE): serial/parallel conversion; bus arbitration; clock generation and synchronization; and handshaking are all performed in hardware
- Interrupt or Polled operation
- Multi-master capability
- 7-bit Addressing
- Supports standard speed I²C (SCL up to 100kHz), fast mode I²C (101KHz to 400kHz), and high-speed mode I²C (401KHz to 833kHz)

Figure 40. Typical I²C bus configuration



1. For 3.3 V system, connect R_P to 3.3 V V_{CC}. For 5.0 V system, connect R_P to 5.0 V V_{DD}.

Figure 42. I²C interface SIOE block diagram

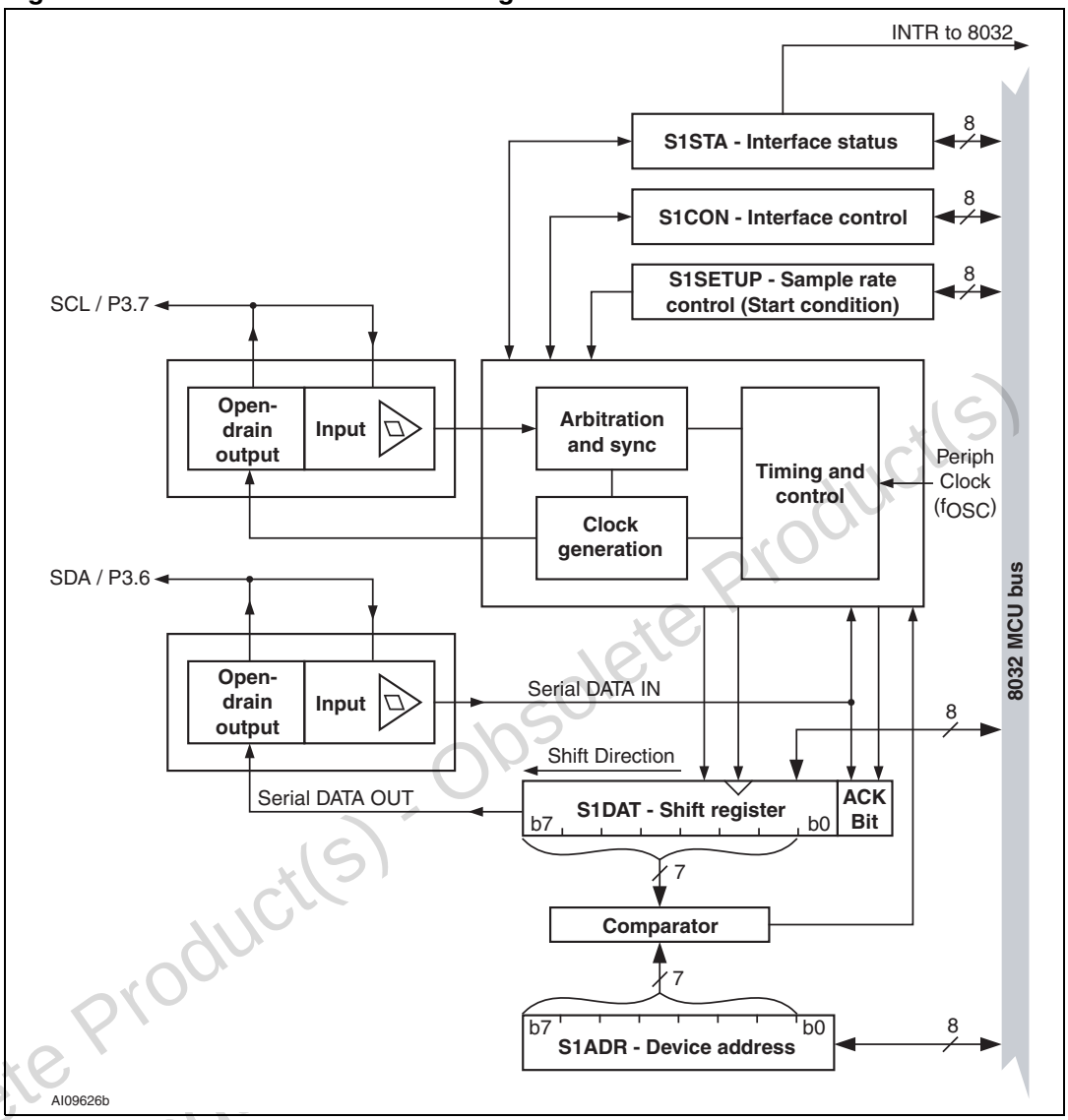
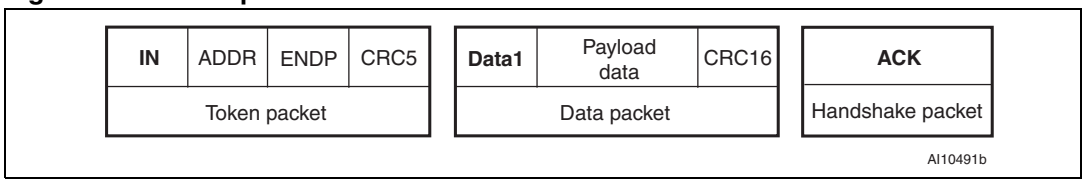


Figure 51. Interrupt transfer



- Control Transfers (see *Figure 52*)

  Control transfers are used to configure and send commands to a device. Control transfers consist of two or three stages:

  – SETUP

  This stage always consists of a data packet with eight bytes of USB CONTROL data.

  – DATA stage (optional)

  If the CONTROL data is such that the host is requesting information from the device, the SETUP stage is followed by a DATA stage. In this case, the host sends an IN token and the device responds with the requested data in the data packet.

  – STATUS stage

  This stage is essentially a handshake informing the device of a successfully completed control operation.

25.2.1 Enumeration

Enumeration is the process that takes place when a device is first connected to the USB. During enumeration, the host requests information from the device about what it is, how many endpoints it has, the power requirements, bus bandwidth requirements, and what driver to load. Once the enumeration process is complete, the device is available for use.

The enumeration process consists of a series of six steps as follows:

1. When a device is first connected to the USB, its address is zero. Upon detecting a new device connected to the USB, the host sends a Get_Descriptor request to address zero, endpoint0.
2. The device, upon receiving a Get_Descriptor request, sends data back to the host identifying what it is.
3. The host resets the device and then sends a Set_Address request. This is a unique address that identifies it from all other devices connected to the USB. This address remains in effect until the device is disconnected from the USB.
4. The host sends more Get_Descriptor requests to the device to gather more detailed information about it and then loads the specified driver.
5. The host will setup and enable the endpoints defined by the device.
6. The device is now configured and ready for use with the host communicating to the device using the assigned address and endpoints.

- USB endpoint select register (USEL)

  Endpoints share the same XDATA space for FIFOs as well as the same SFR addresses for Control and FIFO Valid Size registers. The USB endpoint select register (see *Table 124*) is used to select the desired direction and endpoint that is accessed when reading or writing to the FIFO XDATA address space. This register is also used to select the direction and Endpoint when accessing the USB endpoint control register.

Table 124. USB endpoint select register (USEL 0EFh, reset value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIR	–	–	–	–	EP[2]	EP[1]	EP[0]

Table 125. USEL register bit definition

Bit	Symbol	R/W	Definition
7	DIR	R/W	FIFO's Direction Select Bit: 0: IN FIFO select 1: OUT FIFO select
6	–	–	Reserved
5	–	–	Reserved
4	–	–	Reserved
3	–	–	Reserved
2:0	EP	R/W	Endpoint Selects Bits: 0: Endpoint0 1: Endpoint1 2: Endpoint2 3: Endpoint3 4: Endpoint4

- USB endpoint control register (UCON)

  The Endpoint selected by the USB endpoint select register (see *Table 124 on page 172*) determines the direction and FIFO (IN or OUT) that is controlled by the USB endpoint control register (see *Table 126*). The USB endpoint control register is used to control the selected Endpoint and provides some status about that Endpoint.

Table 126. USB endpoint control register (UCON 0F1h, reset value 08h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	Enable	STALL	TOGGLE	BSY

Table 127. UCON register bit definition

Bit	Symbol	R/W	Definition
7	–	–	Reserved
6	–	–	Reserved
5	–	–	Reserved
4	–	–	Reserved
3	ENABLE	R/W	Selected FIFO Enable Bit. *Note: All FIFOs for each endpoint is enabled after a reset.*
2	STALL	R/W	Stall Control Bit When this bit is set, the Endpoint returns a STALL handshake whenever it receives an IN or OUT token.
1	TOGGLE	R	Data Toggle Bit – Endpoint IN Case The state of this bit determines the type of data packet (0=DATA0 or 1=DATA1) that will be sent during the next IN transaction. This bit is managed by the USB SIE. It is only toggled when an ACK is properly received during the IN transaction. In some cases it may be necessary for firmware to clear this bit. In this case, see the Important Notes section at the end of this data sheet. – Endpoint OUT Case The state of this bit indicates the type of data packet PID that the USB SIE expects to receive with the next OUT transaction (0=DATA0, 1=DATA1). If the Data Toggle for the next OUT transaction received is not as expected, the USB SIE assumes the host is retransmitting the last packet. In this case, an ACK is sent but no interrupt is generated since the original transmission of the packet was OK. This bit is managed by the USB SIE. It is only toggled when an OUT packet is properly received. In some cases it may be necessary for firmware to clear this bit. In this case, see the Important Notes section at the end of this data sheet. *Important notes:* *1. Disabling and enabling the USB SIE using the USBEN bit the UCTL register clears the TOGGLE bit for both directions of all endpoints.* *2. Revision A silicon: See the Important Notes section at the end of the data sheet that explains the workaround for clearing this data toggle bit.* *3. Revision B silicon: Disabling and Enabling the selected FIFO using the ENABLE bit in this register clears the data toggle bit for the selected endpoint's FIFO.*

Table 144. CCON2 register bit definition (SFR 0FBh, reset value 10h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	PCA0CE	PCA0PS3	PCA0PS2	PCA0PS1	PCA0PS0

Table 145. CCON2 register bit definition

Bit	Symbol	R/W	Definition
4	PCA0CE	R/W	PCA0 Clock Enable 0 = PCA0CLK is disabled 1 = PCA0CLK is enabled (default)
3:0	PCA0PS [3:0]	R/W	PCA0 Prescaler $f_{PCA0CLK} = f_{OSC} / (2 \text{ ^ } PCA0PS[3:0])$ Divisor range: 1, 2, 4, 8, 16... 16384, 32768

Table 146. CCON3 register bit definition (SFR 0FCh, reset value 10h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	PCA1CE	PCA1PS3	PCA1PS2	PCA1PS1	PCA1PS0

Table 147. CCON3 register bit definition

Bit	Symbol	R/W	Definition
4	PCA1CE	R/W	PCA1 Clock Enable 0 = PCA1CLK is disabled 1 = PCA1CLK is enabled (default)
3:0	PCA1PS [3:0]	R/W	PCA1 Prescaler $f_{PCA1CLK} = f_{OSC} / (2 \text{ ^ } PCA1PS[3:0])$ Divisor range: 1, 2, 4, 8, 16... 16384, 32768

27.3 Operation of TCM modes

Each of the TCM in a PCA block supports four modes of operation. However, an exception is when the TCM is configured in PWM Mode with programmable frequency. In this mode, all TCM in a PCA block must be configured in the same mode or left to be not used.

27.4 Capture mode

The CAPCOM registers in the TCM are loaded with the counter values when an external pin input changes state. The user can configure the counter value to be loaded by positive edge, negative edge or any transition of the input signal. At loading, the TCM can generate an interrupt if it is enabled.

27.5 Timer mode

The TCM modules can be configured as software timers by enable the comparator. The user writes a value to the CAPCOM registers, which is then compared with the 16-bit counter. If there is a match, an interrupt can be generated to CPU.

have direct connection to the 8032 data bus allowing them to be loaded and read directly by the 8032 at runtime through OMC registers in csiop. This direct access is good for making small peripheral devices (shifters, counters, state machines, etc.) that are accessed directly by the 8032 with little overhead. There are 69 GPLD inputs which include: 8032 address and control signals, page register outputs, PSD module Port pin inputs, and GPLD feedback.

28.1.11 OMCs

There are two banks of eight OMCs inside the GPLD, MCELLAB, and MCELLBC, totalling 16 OMCs all together. Each individual OMC is a base logic element consisting of a flip-flop and some AND-OR logic (*Figure 76 on page 226*). The general structure of the GPLD with OMCs is similar in nature to a 22V10 PLD device with the familiar sum-of-products (AND-OR) construct. True and compliment versions of 69 input signals are available to the inputs of a large AND-OR array. AND-OR array outputs feed into an OR gate within each OMC, creating up to 10 product-terms for each OMC. Logic output of the OR gate can be passed on as combinatorial logic or combined with a flip-flop within in each OMC to realize sequential logic. OMC outputs can be used as a buried nodes driving internal feedback to the AND-OR array, or OMC outputs can be routed to external pins on Ports A, B, or C through the OMC Allocator.

28.1.12 OMC allocator

The OMC allocator (*Figure 77 on page 227*) will route eight of the OMCs from MCELLAB to pins on either Port A or Port B, and will route eight of the OMCs from MCELLBC to pins on either Port B or Port C, based on what is specified in PSDsoft Express.

28.1.13 IMCs

Inputs from pins on Ports A, B, and C are routed to IMCs for conditioning (clocking or latching) as they enter the chip, which is good for sampling and debouncing inputs. Alternatively, IMCs can pass port input signals directly to PLD inputs without clocking or latching (*Figure 78 on page 230*). The 8032 may read the IMCs asynchronously at any time through IMC registers in csiop.

Note: The JTAG signals TDO, TDI, TCK, and TMS on Port C do not route through IMCs, but go directly to JTAG logic.

28.1.14 I/O ports

For 80-pin UPSD34xx devices, the PSD module has 22 individually configurable I/O pins distributed over four ports (these I/O are in addition to I/O on MCU module). For 52-pin UPSD34xx devices, the PSD module has 13 individually configurable I/O pins distributed over three ports. See *Figure 84 on page 243* for I/O port pin availability on these two packages.

I/O port pins on the PSD module (Ports A, B, C, and D) are completely separate from the port pins on the MCU module (Ports 1, 3, and 4). They even have different electrical characteristics. I/O port pins on the PSD module are accessed by csiop registers, or they are controlled by PLD equations. Conversely, I/O Port pins on the MCU module are controlled by the 8032 SFR registers.

28.5.11 Data polling

Polling on the Data Polling Flag Bit (DQ7) is a method of checking whether a program or erase operation is in progress or has completed. *Figure 71* shows the Data Polling algorithm.

When the 8032 issues a program instruction sequence, the embedded algorithm within the Flash memory array begins. The 8032 then reads the location of the byte to be programmed in Flash memory to check status. The Data Polling Flag Bit (DQ7) of this location becomes the compliment of Bit D7 of the original data byte to be programmed. The 8032 continues to poll this location, comparing the Data Polling Flag Bit (DQ7) and monitoring the Error Flag Bit (DQ5). When the Data Polling Flag Bit (DQ7) matches Bit D7 of the original data, then the embedded algorithm is complete. If the Error Flag Bit (DQ5) is '1,' the 8032 should test the Data Polling Flag Bit (DQ7) again since the Data Polling Flag Bit (DQ7) may have changed simultaneously with the Error Flag Bit (DQ5) (see *Figure 71*).

The Error Flag Bit (DQ5) is set if either an internal time-out occurred while the embedded algorithm attempted to program the byte (indicating a bad Flash cell) or if the 8032 attempted to program bit to logic ’1’ when that bit was already programmed to logic ’0’ (must erase to achieve logic ’1’).

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed, to compare the byte that was written to the Flash memory with the byte that was intended to be written.

When using the Data Polling method during an erase operation, *Figure 71* still applies. However, the Data Polling Flag Bit (DQ7) is '0' until the erase operation is complete. A ’1’ on the Error Flag Bit (DQ5) indicates a time-out condition on the Erase cycle, a ’0’ indicates no error. The 8032 can read any location within the sector being erased to get the Data Polling Flag Bit (DQ7) and the Error Flag Bit (DQ5).

Table 183. MCU I/O mode port B data out register (address = csiop + offset 05h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

1. For each bit, 1 = drive port pin to logic '1,' 0 = drive port pin to logic '0'.
2. Default state of register is 00h after reset or power-up.

Table 184. MCU I/O mode port C data out register (address = csiop + offset 12h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	N/A	N/A	PC4	PC3	PC2	N/A	N/A

1. For each bit, 1 = drive port pin to logic '1,' 0 = drive port pin to logic '0'.
2. Default state of register is 00h after reset or power-up.

Table 185. MCU I/O mode port D data out register (address = csiop + offset 13h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	N/A	PD2(3)	PD1	N/A

1. For each bit, 1 = drive port pin to logic '1,' 0 = drive port pin to logic '0'.
2. Default state of register is 00h after reset or power-up.
3. Not available on 52-pin UPSD34xx devices.

Table 186. MCU I/O mode port A direction register(1) (address = csiop + offset 06h)(2)(3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

1. Port A not available on 52-pin UPSD34xx devices.
2. For each bit, 1 = out from UPSD34xx port pin1, 0 = in to PSD34xx port pin.
3. Default state for register is 00h after reset or power-up.

Table 187. MCU I/O mode port B direction in register (address = csiop + offset 07h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

1. For each bit, 1 = out from UPSD34xx port pin1, 0 = in to PSD34xx port pin.
2. Default state for register is 00h after reset or power-up.

Table 188. MCU I/O mode port C direction register (address = csiop + offset 14h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	N/A	N/A	PC4	PC3	PC2	N/A	N/A

1. For each bit, 1 = out from UPSD34xx port pin1, 0 = in to PSD34xx port pin.
2. Default state for register is 00h after reset or power-up.

Table 213. PSD module DC characteristics (with 3.3 V V_{DD})

Symb.	Parameter		Test condition (in addition to those in *Table 211 on page 271*)	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		3.0 V < V_{DD} < 3.6 V	0.7V_{DD}		V_{DD} +0.5	V
V_{IL}	Low level input voltage		3.0 V < V_{DD} < 3.6 V	–0.5		0.8	V
V_{LKO}	V_{DD} (min) for Flash Erase and Program			1.5		2.2	V
V_{OL}	Output low voltage		I_{OL} = 20 µA, V_{DD} = 3.0 V		0.01	0.1	V
			I_{OL} = 4 mA, V_{DD} = 3.0 V		0.15	0.45	V
V_{OH}	Output high voltage		I_{OH} = –20 µA, V_{DD} = 3.0 V	2.9	2.99		V
			I_{OH} = –1 mA, V_{DD} = 3.0 V	2.7	2.8		V
I_{SB}	Standby supply current for power-down mode		$\overline{CSI}$ > V_{DD} – 0.3 V(1)(2)		50	100	µA
I_{LI}	Input leakage current		V_{SS} < V_{IN} < V_{DD}	–1	±0.1	1	µA
I_{LO}	Output leakage current		0.45 < V_{IN} < V_{DD}	–10	±5	10	µA
I_{CC} (DC)(3)	Operating supply current	PLD Only	PLD_TURBO = Off, f = 0 MHz (2)		0		µA/PT
			PLD_TURBO = On, f = 0 MHz		200	400	µA/PT
		Flash memory	During Flash memory WRITE/Erase Only		10	25	mA
			Read only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC)(3)	PLD AC adder				(4)		
	Flash memory AC adder				1.0	1.5	mA/MHz
	SRAM AC adder				0.8	1.5	mA/MHz

1. Internal PD is active.
2. PLD is in non-Turbo mode, and none of the inputs are switching.
3. I_{OUT} = 0 mA.
4. Please see *Figure 96 on page 266* for the PLD current calculation.

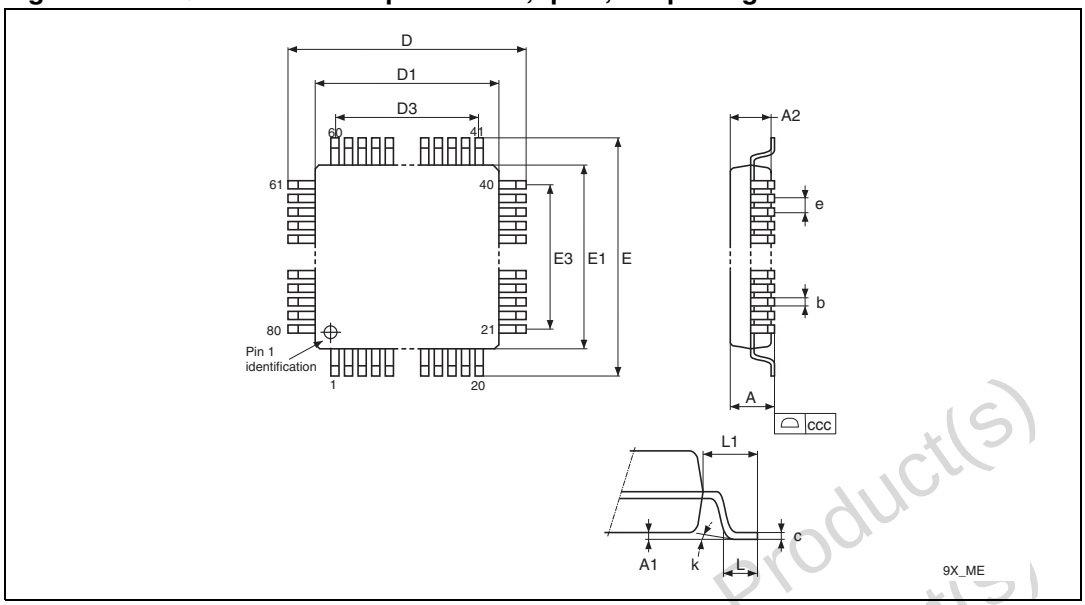
Table 224. CPLD macrocell asynchronous clock mode timing (5 V PSD module)

Symbol	Parameter	Conditions	Min	Max	PT Aloc	Turbo off	Slew rate	Unit
f_{MAXA}	Maximum frequency external feedback	$1/(t_{SA}+t_{COA})$		38.4				MHz
	Maximum frequency internal feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}–10)$		62.5				MHz
	Maximum frequency pipelined data	$1/(t_{CHA}+t_{CLA})$		71.4				MHz
t_{SA}	Input setup time		7		+ 2	+ 10		ns
t_{HA}	Input hold time		8					ns
t_{CHA}	Clock input high time		9			+ 10		ns
t_{CLA}	Clock input low time		9			+ 10		ns
t_{COA}	Clock to output delay			21		+ 10	– 2	ns
t_{ARDA}	CPLD array delay	Any macrocell		11	+ 2			ns
t_{MINA}	Minimum clock period	$1/f_{CNTA}$	16					ns

Table 225. CPLD macrocell asynchronous clock mode timing (3 V PSD module)

Symbol	Parameter	Conditions	Min	Max	PT Aloc	Turbo off	Slew rate	Unit
f_{MAXA}	Maximum frequency external feedback	$1/(t_{SA}+t_{COA})$		21.7				MHz
	Maximum frequency internal feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}–10)$		27.8				MHz
	Maximum frequency pipelined data	$1/(t_{CHA}+t_{CLA})$		33.3				MHz
t_{SA}	Input setup time		10		+ 4	+ 15		ns
t_{HA}	Input hold time		12					ns
t_{CHA}	Clock high time		17			+ 15		ns
t_{CLA}	Clock low time		13			+ 15		ns
t_{COA}	Clock to output delay			31		+ 15	– 6	ns
t_{ARD}	CPLD array delay	Any macrocell		20	+ 4			ns
t_{MINA}	Minimum clock period	$1/f_{CNTA}$	36					ns

Figure 114. LQFP80 – 80-lead plastic thin, quad, flat package outline



1. Drawing is not to scale.

Table 238. LQFP80 – 80-lead plastic thin, quad, flat package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.090	0.200		0.0035	0.0079
D	14.000			0.5512		
D1	12.000			0.4724		
D3	9.500			0.3740		
E	14.000			0.5512		
E1	12.000			0.4724		
E3	9.500			0.3740		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k		0°	7°		0°	7°
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.