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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Xstormy16
Core Size	16-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc88f52h0aute-2h

■Minimum instruction cycle time (tCYC)
- 83.3 ns (12MHz) V_{DD} = 4.5 to 5.5V
- 107 ns (9.3MHz) V_{DD} = 3.0 to 5.5V
- 500 ns (2MHz) V_{DD} = 2.5 to 5.5V

■Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units : 86 (P0n P1n, P2n, P3n, P4n, P5n, P6n, P7n, PAn PB0 to PB6, PC2, PD0 to PD5)
- Oscillation/normal withstand voltage I/O ports : 4 (PC0, PC1, PC3, PC4)
- Reset pins : 1 (RESB)
- TEST pins : 1 (TEST)
- Power pins : 8 (V_{SS}1 to 4, V_{DD}1 to 4)

■Timers
- Timer 0: 16-bit timer that supports PWM/toggle outputs
  1) 5-bit prescaler
  2) 8-bit PWM × 2, 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 1: 16-bit timer with capture registers
  1) 5-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 2: 16-bit timer with capture registers
  1) 4-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3: 16-bit timer that supports PWM/toggle outputs
  1) 8-bit prescaler
  2) 8-bit timer × 2ch or 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Timer 6: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 1
- Timer 7: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 1
  * Prescaler 0 and 1 are consisted of 4 bits and can choose their clock source from OSC0 or OSC1.
- Base timer
  1) Clock may be selected from OSC0 (32.768kHz crystal oscillator) and frequency-divided output of system clock.
  2) Interrupts can be generated in 7 timing schemes.

■Real time clock
1) Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leap year calculation function.
2) Consisted of Independent second- minute-hour-day-month-year-century counters.
3) Programmable count-clock calibration function.

■Serial interfaces

- SIO0: 8-bit synchronous SIO
  1) LSB first/MSB first mode selectable
  2) Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  3) Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  4) Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  5) Interval function (intervals specifiable in 0 to 64 tSCK units)
  6) Wakeup function
- SIO1: 8-bit synchronous SIO
  1) LSB first/MSB first mode selectable
  2) Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  3) Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  4) Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  5) Interval function (intervals specifiable in 0 to 64 tSCK units)
  6) Wakeup function
- SMIIC0: Single master I^2C/8-bit synchronous SIO
  Mode 0: Single-master mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SMIIC1: Single master I^2C/8-bit synchronous SIO
  Mode 0: Single-master mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SLIIC0: Slave I^2C/8-bit synchronous SIO
  Mode 0: I^2C slave mode communication
  Mode 1: Synchronous 8-bit serial I/O (MSB first)
  Note: usable only with the external clock source
- UART0
  1) Data length : 8 bits (LSB first)
  2) Start bits : 1 bit
  3) Stop bits : 1 bit
  4) Parity bits : None/even parity/odd parity
  5) Transfer rate : 4/8 cycle
  6) Baudrate source clock: P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or Timer 4 cycle.
  7) Full duplex communication
  Note: The “cycle” refers to one period of the baudrate clock source.
- UART2
  1) Data length : 8 bits (LSB first)
  2) Start bits : 1 bit
  3) Stop bits : 1/2 bit
  4) Parity bits : None/even parity/odd parity
  5) Transfer rate : 8 to 4096 cycle
  6) Baudrate source clock : System clock/OSC0/OSC1/P26 input signal
  7) Wakeup function
  8) Full duplex communication
  Note: The “cycle” refers to one period of the baudrate clock source.
- UART3
  1) Data length : 8 bits (LSB first)
  2) Start bits : 1 bit
  3) Stop bits : 1/2 bit
  4) Parity bits : None/even parity/odd parity
  5) Transfer rate : 8 to 4096 cycle
  6) Baudrate source clock: System clock/OSC0/OSC1/P36 input signal
  7) Wakeup function
  8) Full duplex communication
  Note: The “cycle” refers to one period of the baudrate clock source.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Released by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) OSC1, RC and OSC0 oscillators automatically stop.
  2) There are the six ways of releasing the HOLD mode.
    (1) Setting the reset pin to the low level
    (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
    (3) Having an interrupt source established at port 0
    (4) Having an interrupt source established at port 5
    (5) Having an interrupt established at SIO0 or SIO1
    (6) Having an interrupt established at UART2, UART3 or UART4
- HOLDX mode: Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0.
  1) OSC1 and RC oscillations automatically stop.
  2) OSC0 maintains the state that is established when the HOLDX mode is entered.
  3) There are seven ways of releasing the HOLDX mode.
    (1) Setting the reset pin to the low level
    (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
    (3) Having an interrupt source established at port 0
    (4) Having an interrupt source established at port 5
    (5) Having an interrupt source established at the base timer circuit
    (6) Having an interrupt established at SIO0 or SIO1
    (7) Having an interrupt established at UART2, UART3 or UATR4
    .

■On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time display.
- Single-wire communication

■Package Form

- TQFP100(14×14): Lead-free and halogen-free type

■Development Tools

- On-chip debugger: EOCUIF1 + LC88F52H0A

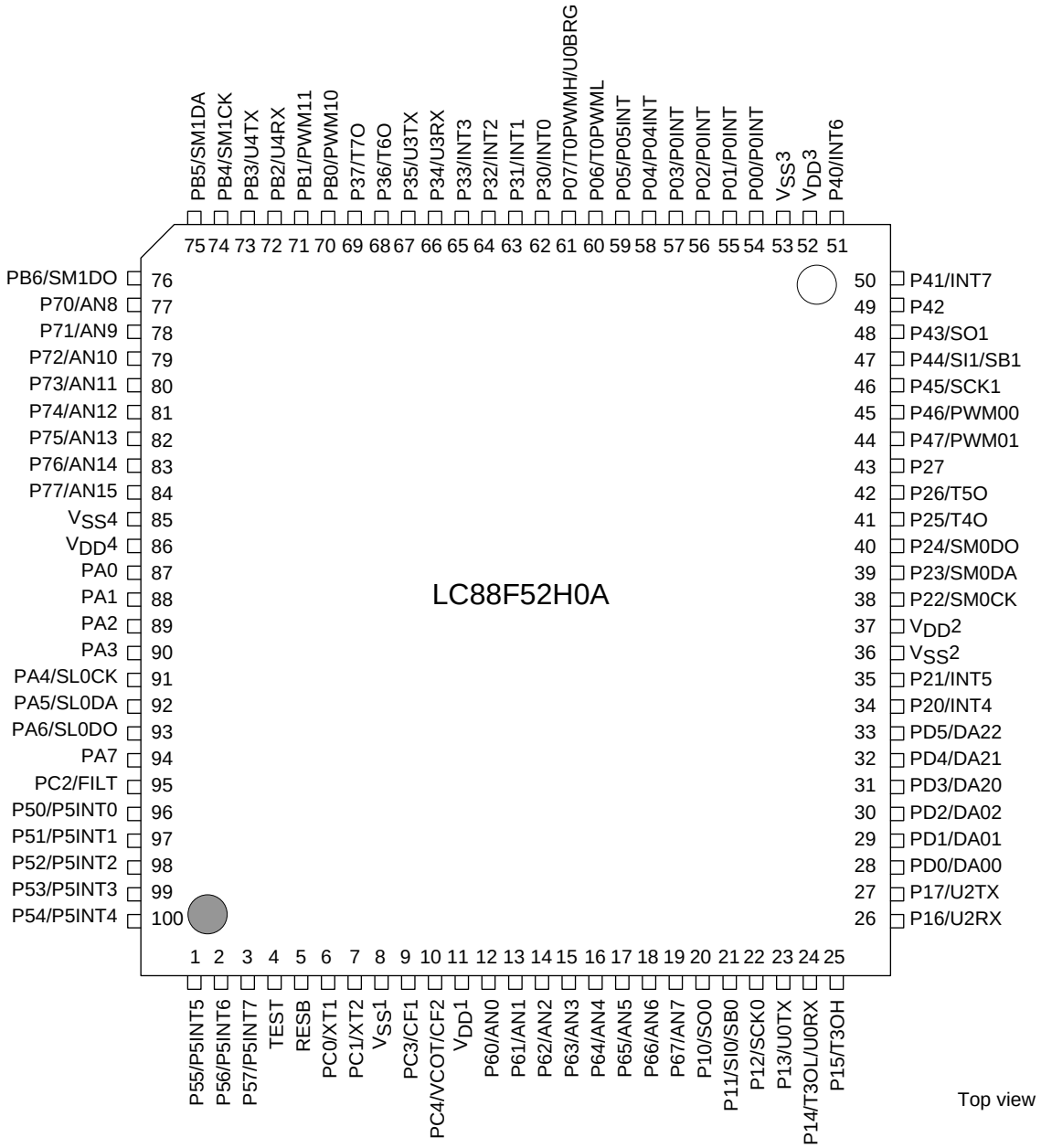
■Programming board

Package	Programming Board
TQFP100 (14 × 14)	W88F52TQ

■Flash Programming

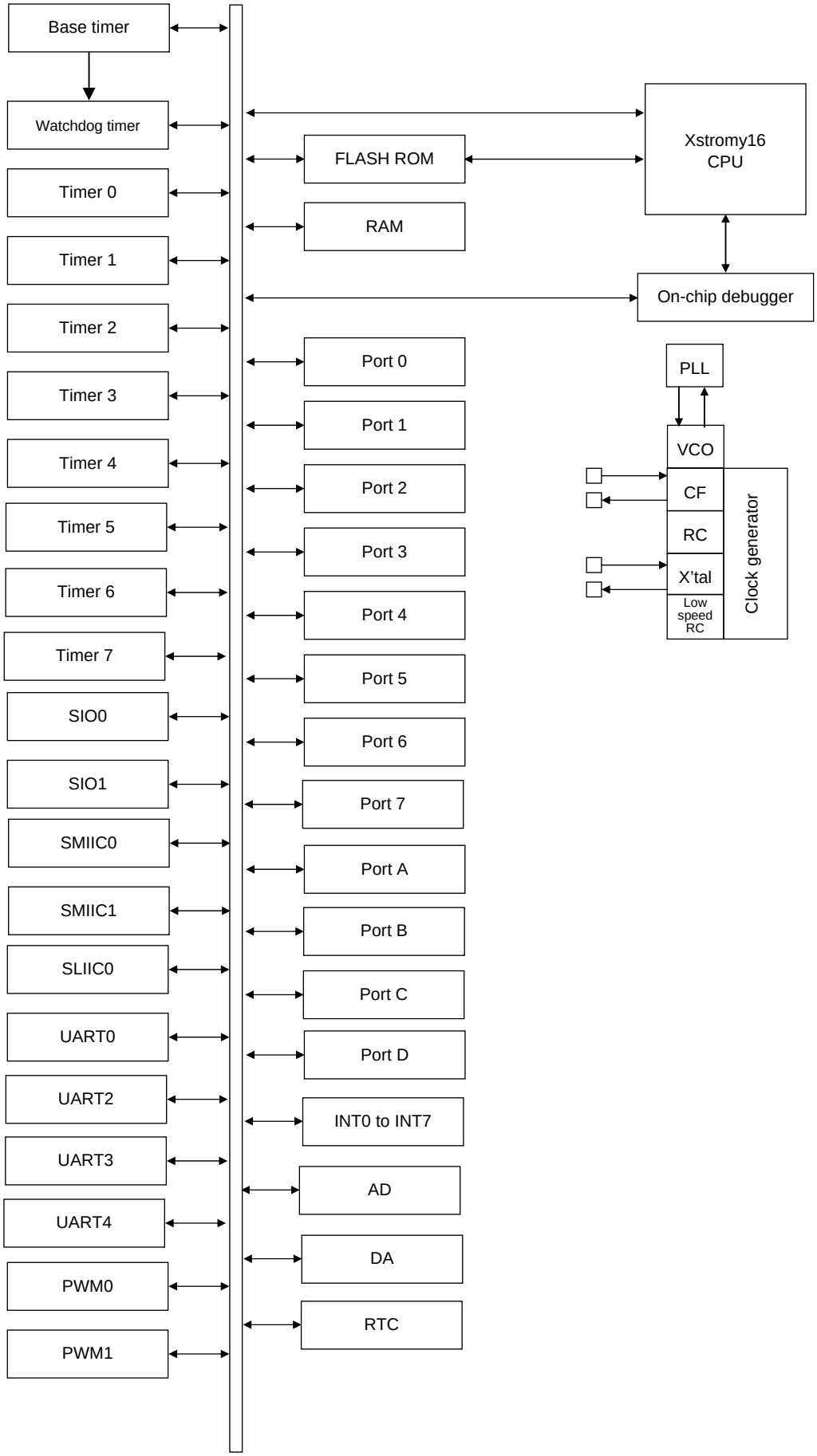
Manufacturer	Model Name	Supported Version	Device
Flash Support Group (single)	AF9708/09/09B/09C	Revision: After Rev.03.32D	88F512SN
Flash Support Group (Gang)	AF9723/23B		
	AF9833		
Our company	SKK/SKK Type-B	Application Version After 1.06 Chip Data Version After 2.22	LC88F52H0A

Pin Assignment



TQFP100 (14×14) (Lead-free and halogen-free type)

System Block Diagram



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Parameter		Symbol	Applicable Pin /Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3, 4 Ports 7, A, B P20, P21, P24 to P27 PA0 to PA4, PA6, PA7 PB0 to PB4, PB6, PB7	Per applicable pin				20	mA
		IOPL(2)	P22, P23 PA4, PA5 PB4, PB5	Per applicable pin				25	
		IOPL(3)	Ports 5, 6 PC0 to PC4	Per applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	Ports 0, 1, 3, 4 Ports 7, A, B P20, P21, P24 to P27 PA0 to PA4, PA6, PA7 PB0 to PB4, PB6, PB7	Per applicable pin				15	
		IOML(2)	P22, P23 PA4, PA5 PB4, PB5	Per applicable pin				20	
		IOML(3)	Ports 5, 6 PC0 to PC4	Per applicable pin				7.5	
	Total output current	ΣIOAL(1)	Ports 5 PC0 to PC2	Total of currents at applicable pins				15	
		ΣIOAL(2)	Port 6 PC3 to PC4	Total of currents at applicable pins				15	
		ΣIOAL(3)	Port 5, 6 PC0 to PC4	Total of currents at applicable pins				20	
		ΣIOAL(4)	Ports 1, D P20, P21	Total of currents at applicable pins				45	
		ΣIOAL(5)	P22 to P27	Total of currents at applicable pins				45	
		ΣIOAL(6)	Ports 1, 2, D	Total of currents at applicable pins				80	
		ΣIOAL(7)	Port 4	Total of currents at applicable pins				45	
		ΣIOAL(8)	Port 0, 3	Total of currents at applicable pins				45	
		ΣIOAL(9)	Port 0, 3, 4	Total of currents at applicable pins				80	
		ΣIOAL(10)	Port 7, B	Total of currents at applicable pins				45	
		ΣIOAL(11)	Port A	Total of currents at applicable pins				45	
		ΣIOAL(12)	Port 7, A, B	Total of currents at applicable pins				80	
Allowable power dissipation		Pd max	TQFP100(14×14)	Ta=-40 to +85°C				250	mW
Operating ambient temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Oscillation frequency range (Note 2-3)	FmCF(1)	PC3 (CF1), PC4 (CF2)	12MHz ceramic oscillator mode See Fig. 1.	4.5 to 5.5		12		MHz
	FmCF(2)	PC3(CF1), PC4(CF2)	8MHz ceramic oscillator mode See Fig. 1.	3.0 to 5.5		8		
	FmCF(3)	PC3(CF1), PC4(CF2)	4MHz ceramic oscillator mode See Fig. 1.	2.5 to 5.5		4		
	FmRC		Internal RC oscillation	2.5 to 5.5	0.5	1.0	2.0	
	FmSLRC		Internal low-speed RC oscillation	2.5 to 5.5	18	30	45	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillator mode See Fig. 2.	2.5 to 5.5		32.768		
	FmVCO(1)		VCO oscillator When setting VC3=1 When SELDIV=0 or 1 See Fig. 9.	2.5 to 3.8	5.0		9.0	MHz
	FmVCO(2)		VCO oscillator When setting VC3=0 When SELDIV=2 or 3 See Fig. 9.	2.5 to 3.8	5.0		12	
	FmVCO(3)		VCO oscillator When setting VC3=1 When SELDIV=0 or 1 See Fig. 9.	3.6 to 5.5	5.0		9.0	
	FmVCO(4)		VCO oscillator When setting VC3=0 When SELDIV=2 or 3 See Fig. 9.	3.6 to 5.5	9.0		12	
	FmVCO(5)		VCO oscillator When OSC0=32.768KHz SELDIV setting range=0 to 3 SELDLY setting range=0 to 3	2.5 to 5.5		Note 2-4		

Note 2-3: See Tables 1 and 2 for oscillator constant values.

Note 2-4: VCO oscillation frequency = 0.032768×(56×(SELDIV+3)+SELDLY)

Electrical Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

Parameter	Symbol	Applicable/ Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr. off leakage current)	2.5 to 5.5			1	µA
Low level input current	I_{IL}(1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr. off leakage current)	2.5 to 5.5	-1			
High level output voltage	V_{OH}(1)	Ports 0, 1, 2, 3 Ports 4, A, D P40 to P45 PB2 to PB6	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(3)		I_{OH}=-0.2mA	2.5 to 5.5	V_{DD}-0.4			
	V_{OH}(4)	Port 5, 6 PC2	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(5)		I_{OH}=-0.2mA	2.5 to 5.5	V_{DD}-0.4			
	V_{OH}(6)	P46, P47 PB0, PB1	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	V_{OH}(7)		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(8)		I_{OH}=-1.0mA	2.5 to 5.5	V_{DD}-0.4			
	V_{OH}(9)	PC0, PC1, PC3, PC4,	I_{OH}=-1.0mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(10)		I_{OH}=-0.4mA	2.5 to 5.5	V_{DD}-0.4			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 3, 4 Ports 7, D P20 to P21, P24 to P27 PA0 to PA3 PA6 to PA7 PB0 to PB3, PB6	I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(3)		I_{OL}=1.0mA	2.5 to 5.5			0.4	
	V_{OL}(4)	P22, P23, PA4, PA5, PB4, PB5	I_{OL}=11mA	4.5 to 5.5			1.5	
	V_{OL}(5)		I_{OL}=3.0mA	3.0 to 5.5			0.4	
	V_{OL}(6)		I_{OL}=1.3mA	2.5 to 5.5			0.4	
	V_{OL}(7)	Ports 5, 6 PC2	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(8)		I_{OL}=1.0mA	2.5 to 5.5			0.4	
	V_{OL}(9)	PC0, PC1, PC3, PC4	I_{OL}=1.0mA	3.0 to 5.5			0.4	
	V_{OL}(10)		I_{OL}=0.4mA	2.5 to 5.5			0.4	
Pull-up resistor	Rpu(1)	Ports 0, 1, 2, 3 Ports 4, 5, 6, 7 Ports A, B, D, PC2	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.5 to 4.5	18	55	150	
Hysteresis voltage	VHYS	RESB When ports 1, 2, 3, 4, A PnFSAn=1		2.5 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	Pins other than that under test $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.5 to 5.5		10		pF

SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK(3)	SCK0 (P12)	• See Fig. 6.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Data setup time		tsDI(2)	SI0 (P11), SB0 (P11)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Input clock	Output delay time	tdD0(3)	SO0 (P10), SB0 (P11)	• (Note 4-2-2)	2.5 to 5.5			1tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig.6.

SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK(4)	SCK1(P45)	• See Fig. 6.	2.5 to 5.5	4			tCYC
		Low level pulse width	tSCKL(4)				2			
		High level pulse width	tSCKH(4)				2			
			tSCKHA(4)		• Automatic communication mode • See Fig. 6.		6			
			tSCKHBSY(4a)		• Automatic communication mode • See Fig. 6.		23			
			tSCKHBSY(4b)		• Mode other than automatic communication mode • See Fig. 6.		4			
	Output clock	Period	tSCK(5)	SCK1(P45)	• CMOS output selected • See Fig. 6.	2.5 to 5.5	4			tSCK
		Low level pulse width	tSCKL(5)				1/2			
		High level pulse width	tSCKH(5)				1/2			
			tSCKHA(5)		• Automatic communication mode • CMOS output selected • See Fig. 6.		6			tCYC
			tSCKHBSY(5a)		• Automatic communication mode • CMOS output selected • See Fig. 6.		4		23	
			tSCKHBSY(5b)		• Mode other than automatic communication mode • See Fig. 6.		4			
Serial input	Data setup time		tsDI(3)	SI1(P44), SB1(P44)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(3)				0.03			
Serial output	Input clock	Output delay time	tdD0(4)	SO1(P43), SB1(P44)	• (Note 4-3-2)	2.5 to 5.5			1tCYC +0.05	µs
	Output clock		tdDO(5)		• (Note 4-3-2)				1tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(6)	SCK1(P45)	• See Fig. 6.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(6)				1			
		High level pulse width	tSCKH(6)				1			
			tSCKHBSY(6)				2			
Serial input	Data setup time		tsDI(4)	SI1(P44), SB1(P44)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(4)				0.03			
Serial output	Input clock	Output delay time	tdD0(6)	SO1(P43), SB1(P44)	• (Note 4-4-2)	2.5 to 5.5			1tCYC +0.05	

Note 4-4-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SMIIC0 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(7)	SM0CK(P22)	See Fig. 6.	2.5 to 5.5	4			tCYC
		Low level pulse width	tSCKL(7)				2			
		High level pulse width	tSCKH(7)				2			
	Output clock	Period	tSCK(8)	SM0CK(P22)	• CMOS output selected • See Fig. 6.		4			
		Low level pulse width	tSCKL(8)			2.5 to 5.5	1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
Serial input	Data setup time		tsDI(5)	SM0DA(P23)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(5)				0.03			
Serial output	Output delay time		tdD0(7)	SM0DO(P24), SM0DA(P23)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 6.	2.5 to 5.5			1tCYC +0.05	

Note 4-5-1: These specifications are theoretical values. Add margin depending on its use.

SMIIC0 I²C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Clock	Input clock	Period	tSCL	SM0CK(P22)	• See Fig. 8.	2.5 to 5.5	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK(P22)	• Specified as interval up to time when output state starts changing.	2.5 to 5.5	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.5 to 5.5			1	Tfilt
Bus release time between start and stop	Input		tBUF	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.5 to 5.5	2.5			Tfilt
	Output		tBUFx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK(P22) SM0DA(P23)	• When SMIIC register control bit, $I^2CSHDS=0$ • See Fig. 8.	2.5 to 5.5	2.0			Tfilt
					• When SMIIC register control bit, $I^2CSHDS=1$ • See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.1			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.5 to 5.5	1.0			Tfilt
	Output		tSU;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			

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SMIIC1 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(7)	SM1CK(PB4)	See Fig. 6.	2.5 to 5.5	4			tCYC
		Low level pulse width	tSCKL(7)				2			
		High level pulse width	tSCKH(7)				2			
	Output clock	Period	tSCK(8)	SM1CK(PB4)	• CMOS output selected • See Fig. 6.	2.5 to 5.5	4			
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
Serial input	Data setup time		tsDI(5)	SM1DA(PB5)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.5 to 5.5	0.03			µs
	Data hold time		thDI(5)				0.03			
Serial output	Output delay time		tdD0(7)	SM1DO(PB6), SM1DA(PB5)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 6.	2.5 to 5.5			1tCYC +0.05	

Note 4-7-1: These specifications are theoretical values. Add margin depending on its use.

SMIIC1 I²C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Clock	Input clock	Period	tSCL	SM1CK(PB4)	• See Fig. 8.	2.5 to 5.5	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM1CK(PB4)	• Specified as interval up to time when output state starts changing.	2.5 to 5.5	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM1CK(PB4) SM1DA(PB5)	• See Fig. 8.	2.5 to 5.5			1	Tfilt
Bus release time between start and stop	Input		tBUF	SM1CK(PB4) SM1DA(PB5)	• See Fig. 8.	2.5 to 5.5	2.5			Tfilt
	Output		tBUFx	SM1CK(PB4) SM1DA(PB5)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM1CK(PB4) SM1DA(PB5)	• When SMIIC register control bit, I^2CSHDS=0 • See Fig. 8.	2.5 to 5.5	2.0			Tfilt
					• When SMIIC register control bit, I^2CSHDS=1 • See Fig. 8.		2.5			
	Output		tHD;STAx	SM1CK(PB4) SM1DA(PB5)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.1			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU;STA	SM1CK(PB4) SM1DA(PB5)	• See Fig. 8.	2.5 to 5.5	1.0			Tfilt
	Output		tSU;STAx	SM1CK(PB4) SM1DA(PB5)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			

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Parameter		Symbol	Applicable Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Stop condition setup time	Input	tSU;STO	SM1CK(PB4) SM1DA(PB5)	• See Fig. 8.	2.5 to 5.5	1.0			Tfilt
	Output	tSU;STOx	SM1CK(PB4) SM1DA(PB5)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.9			µs
				• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.1			
Data hold time	Input	tHD;DAT	SM1CK(PB4) SM1DA(PB5)	• See Fig. 8.	2.5 to 5.5	0			Tfilt
	Output	tHD;DATx	SM1CK(PB4) SM1DA(PB5)	• Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input	tSU;DAT	SM1CK(PB4) SM1DA(PB5)	• See Fig. 8.	2.5 to 5.5	1			Tfilt
	Output	tSU;DATx	SM1CK(PB4) SM1DA(PB5)	• Specified as interval up to time when output state starts changing.		1tSCL -1.5Tfilt			
SM0CK and SM0DA pins fall time	Input	tF	SM1CK(PB4) SM1DA(PB5)	• See Fig. 8.	2.5 to 5.5			300	ns
	Output	tF	SM1CK(PB4) SM1DA(PB5)	• When SMIIC register control bits PSLW=1, P5V=1	5	20 +0.1Cb		250	
				• When SMIIC register control bits PSLW=1, P5V=0	3	20 +0.1Cb		250	
				• SM0CK, SM0DA port output FAST mode • Cb≤400pF	3 to 5.5			100	

Note 4-8-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-8-2: The value of Tfilt is determined by the values of the register SMIC1BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

250ns ≥ Tfilt > 140ns

Note 4-8-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 400pF

Note 4-8-4: The standard clock mode refers to a mode that is entered by configuring SMIC1BRG as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 1

SCL frequency setting ≤ 100kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC1BRG as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400kHz

AD Converter Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

12-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	NAD	AN0(P60) to AN7(P67), AN8(P70) to AN15(P77)		3.0 to 5.5		12		bit
Absolute accuracy	ETAD		(Note 6-1)	3.0 to 5.5			±16	LSB
Conversion time	TCAD12		Conversion time calculated	4.5 to 5.5	27		209	µs
				3.0 to 5.5	67		209	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Conversion time calculation formula: TCAD12= ((52/(AD division ratio))+2) × tCYC

8-bit AD Conversion Mode

Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	NAD	AN0(P60) to AN7(P67), AN8(P70) to AN15(P77)		3.0 to 5.5		8		bit
Absolute accuracy	ETAD		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD8		Conversion time calculated	4.5 to 5.5	17		129	µs
				3.0 to 5.5	42		129	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Conversion time calculation formula: TCAD8= ((32/(AD division ratio))+2) × tCYC

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy.
Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:
- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

DA Converter Characteristics at Ta=-40 to+85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	NDA	DA00(PD0) to DA02(PD2) DA10(PD3) to DA12(PD5)		3.0 to 5.5		8		bit
Absolute accuracy	ETDA			3.0 to 5.5			±2.0	LSB
Output resistor	DAOR			3.0 to 5.5	9.5	16.0	22.9	kΩ
Analog port output current	VDAOUT			3.0 to 5.5	V_{SS}		V_{DD}	V

Consumption Current Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$
typ: 5.0V (V_{DD}=4.5V to 5.5V), 3.3V (V_{DD}=3.0V to 4.5V, 2.2V to 4.5V)

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$	• FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		10.4	19	mA
	IDDOP(2)		• FmCF=8MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 8MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		8.50	17	
	IDDOP(3)			3.0 to 4.5		4.91	13	
	IDDOP(4)		• FmCF=4MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 4MHz • Internal RC oscillation stopped • 1/2 frequency division mode	4.5 to 5.5		4.02	6.1	
	IDDOP(5)			2.5 to 4.5		2.62	4.3	
	IDDOP(6)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	4.5 to 5.5		2.18	6.0	
	IDDOP(7)			2.2 to 4.5		1.28	4.2	
	IDDOP(8)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		72.9	195	µA
	IDDOP(9)			2.2 to 4.5		39.8	160	
	IDDOP(10)		• FmCF=0Hz (oscillation stopped) • FmVCO=11.1MHz oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to VCO • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		10.5	19.2	mA
	IDDOP(11)		• FmCF=0Hz (oscillation stopped) • FmVCO=7.34MHz oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to VCO • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		9.07	17.3	
	IDDOP(12)			3.0 to 4.5		5.23	13.8	

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

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Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$	• HALT mode • FmCF=12MHz ceramic mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		3.70	6.5	mA
	IDDHALT(2)		• HALT mode • FmCF=10MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 10MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		2.60	5.0	
	IDDHALT(3)			3.0 to 4.5		1.34	3.5	
	IDDHALT(4)		• HALT mode • FmCF=4MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 4MHz • Internal RC oscillation stopped • 1/2 frequency division mode	4.5 to 5.5		1.08	3.1	
	IDDHALT(5)			2.2 to 4.5		0.50	2.2	
	IDDHALT(6)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	4.5 to 5.5		0.53	3.0	
	IDDHALT(7)			2.2 to 4.5		0.26	2.1	
	IDDHALT(8)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		27.3	145	µA
	IDDHALT(9)			2.2 to 4.5		9.52	112	
	IDDHALT(10)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmVCO=11.1MHz oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to VCO • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		4.19	6.8	mA
	IDDHALT(11)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmVCO=7.34MHz oscillator mode FmX'tal=32.768kHz crystal oscillator mode • System clock set to VCO vInternal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		3.18	5.5	
	IIDHALT(12)			3.0 to 4.5		1.68	4.0	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open (external clock mode)	4.5 to 5.5		0.11	98	µA
	IDDHOLD(2)			2.5 to 4.5		0.04	72	
HOLDX mode consumption current	IDDHOLD(3)		HOLDX mode • CF1=V_{DD} or open (external clock mode) • FmX'tal=32.768kHz crystal oscillator mode	4.5 to 5.5		19.0	132	
	IDDHOLD(4)			2.5 to 4.5		4.91	90	

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

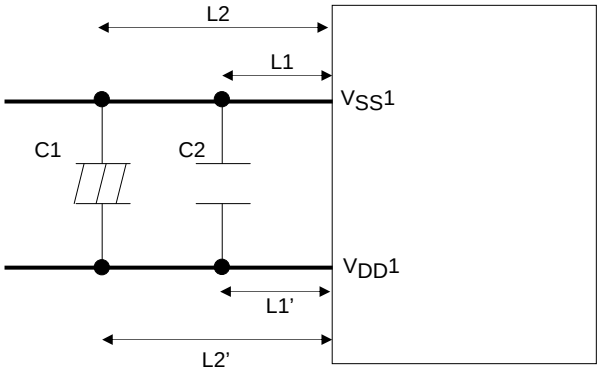
F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Microcontroller erase current current is excluded.	3.0 to 5.5			15	mA
Onboard programming time	tFW(1)		• 512-/1K-byte erase operation	3.0 to 5.5			30	ms
	tFW(2)		• 2-byte programming operation	3.0 to 5.5			60	µs

Power Pin Treatment Conditions 1 ($V_{DD}1$, $V_{SS}1$)

Connect capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins:

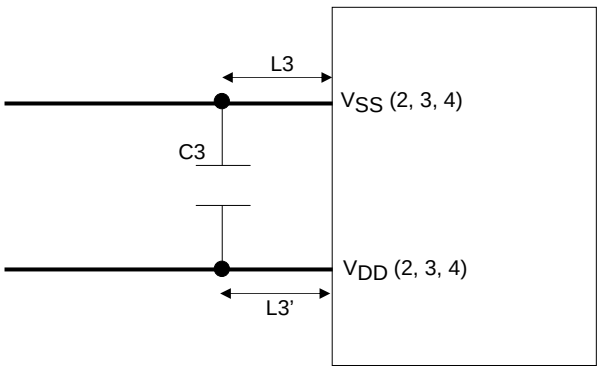
- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1µF or larger.
- The $V_{DD}1$ and $V_{SS}1$ traces must be thicker than the other traces.

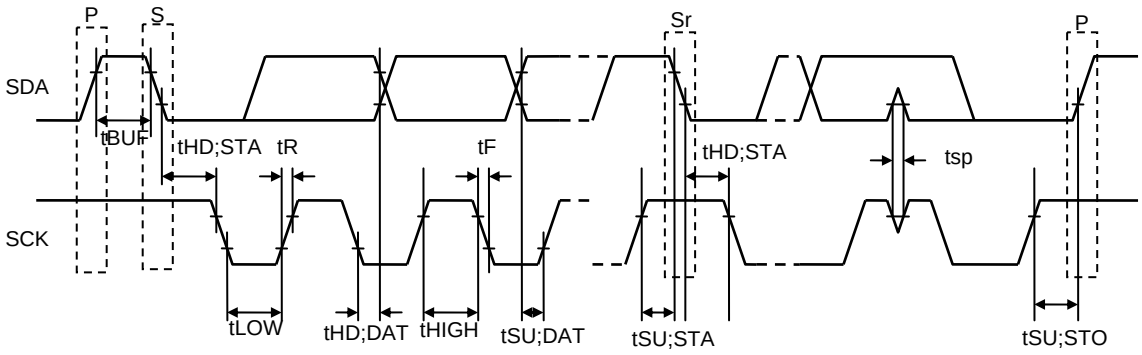


Power Pin Treatment Conditions 2 ($V_{DD}(2, 3, 4)$, $V_{SS}(2, 3, 4)$)

Connect capacitors that meet the following condition between the $V_{DD}(2, 3, 4)$ and $V_{SS}(2, 3, 4)$ pins:

- Connect among the $V_{DD}(2, 3, 4)$ and $V_{SS}(2, 3, 4)$ pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1µF or larger.
- The $V_{DD}(2, 3, 4)$ and $V_{SS}(2, 3, 4)$ traces must be thicker than the other traces.





S: Start condition
P: Stop condition
Sr: Restart condition

Figure 8 I^2C Timing

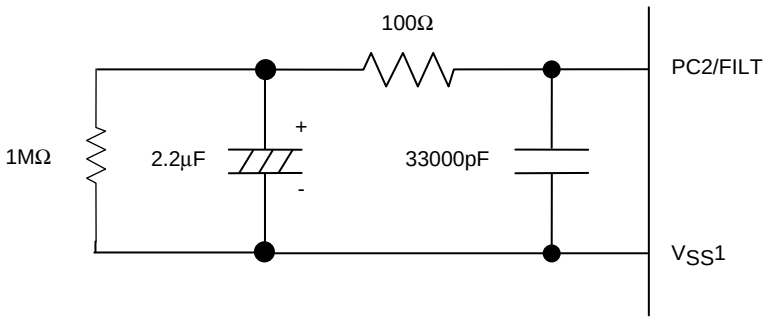


Figure 9 FILT recommended circuit
*Take at least 50ms to oscillation to stabilize after PLL is started.