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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2 DSP
Core Size	32-Bit Single-Core
Speed	62.5MHz
Connectivity	EBI/EMI, Ethernet, IrDA, FIFO, SCI, SIO
Peripherals	DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417616sfv

Item	Page	Revision (See Manual for Details)
10.2.8 Transmit/Receive Status Copy Enable Register (TRSCER)	437	Description amended

Bit:	31	30	29	. . .	19	18	17	16
	—	—	—	. . .	—	—	—	—
Initial value:	0	0	0	. . .	0	0	0	0
R/W:	R	R	R	. . .	R	R	R	R

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	RMAFCE	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R

Bits 31 to 8—Reserved These bits are always read as 0. The write value should always be 0.

Bit 7—Multicast Address Frame Receive (RMAF): Bit Copy Enable (RMAFCE)

Bit 7: RMAFCE	Description
0	Enables the RMAF bit status to be indicated in the RFS7 bit in the receive descriptor.
1	Disables occurrence of corresponding source to be indicated in the RFS7 bit in the receive descriptor.

Bits 6 to 0—Reserved: These bits are always read as 0. The write value should always be 0.

10.3.1 Descriptor List and Data Buffers Transmit Descriptor 0 (TD0)	450	Description amended

Bit 27—Transmit Frame Error (TFE): Indicates that one or other bit of the transmit frame status indicated by bits 26 to 0 is set.

Bit 27: TFE	Description
0	No error during transmission
1	An error of some kind occurred during transmission (see bits 26 to 0)

Bits 26 to 0—Transmit Frame Status 26 to 0 (TFS26 to TFS0): These bits indicate the error status during frame transmission.

- TFS26 to TFS9—Reserved
- TFS8—Teransmit Abort Detect

  Note: This bit is set to 1 wh any of Transmit Frame Status bits 4 to 0 is set. When this bit is set, the Transmit Frame Error bit (bit 27: TFE) is set to 1.
- TFS7 to TFS5—Reserved

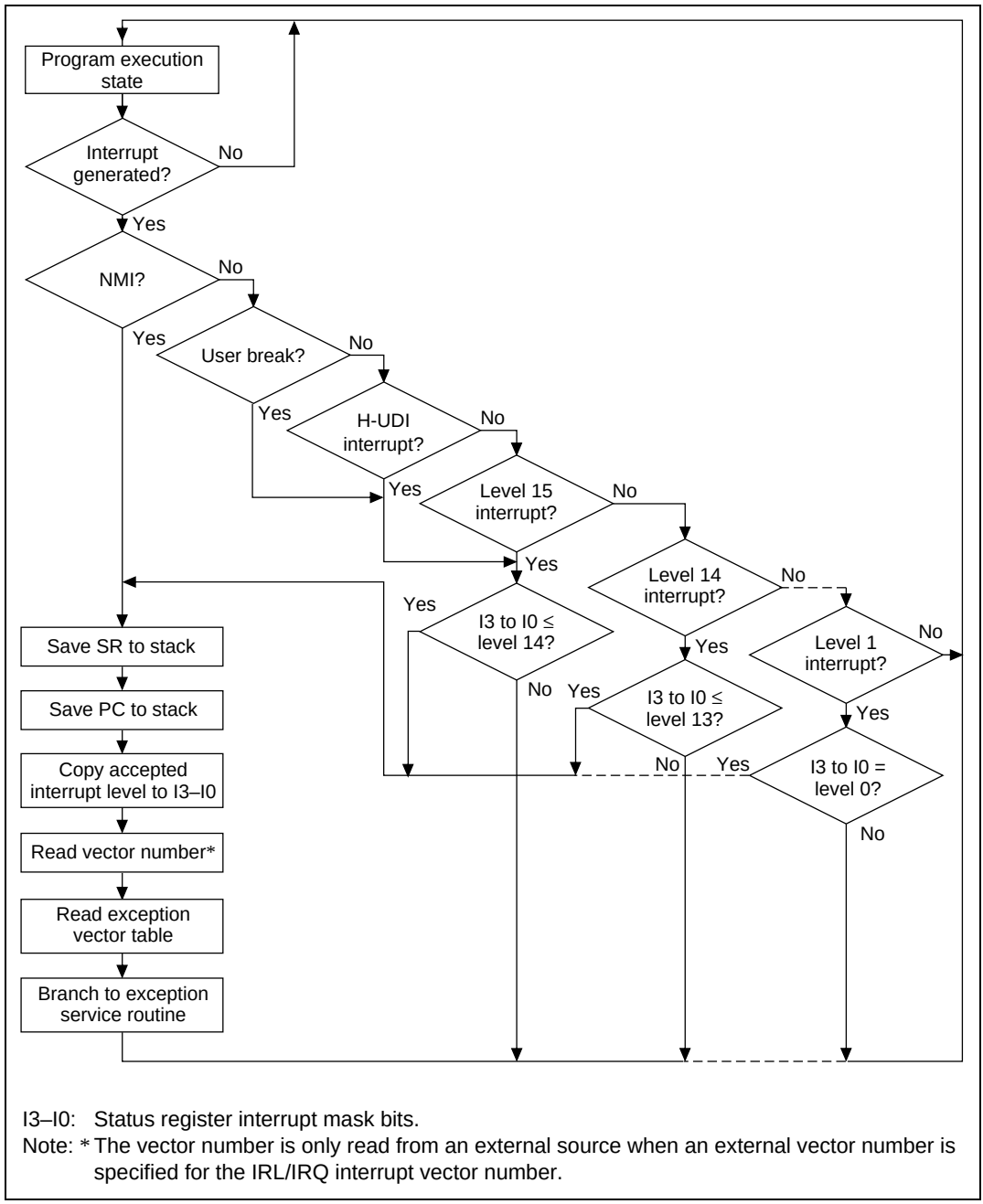
Type	Symbol	I/O	Name	Function
I/O ports	PA0–PA13*	I/O	General port	General input/output port pins
				Input or output can be specified bit by bit
	PB0–PB15	I/O	General port	General input/output port pins
				Input or output can be specified bit by bit

Note: * PA3 cannot be used; CKPO is valid instead.

1.3.3 Pin Multiplexing

Table 1.3 Pin Multiplexing

No.	Function 1	Function 2	Function 3	Function 4	Type
12	$PLLV_{CC}$				Clocks
9	$PLLV_{SS}$				
11	PLLCAP1				
10	PLLCAP2				
19	EXTAL				
21	XTAL				
23	CKIO				
24	$\overline{\text{CKPREQ}}$/CKM				
25	$\overline{\text{CKPACK}}$				9 pins
8	$\overline{\text{RES}}$				System control
13	MD4				
14	MD3				
15	MD2				
16	MD1				
17	MD0				6 pins
5	NMI				Interrupts
1	$\overline{\text{IRL3}}$				
2	$\overline{\text{IRL2}}$				
3	$\overline{\text{IRL1}}$				
4	$\overline{\text{IRL0}}$				
27	$\overline{\text{IVECF}}$				6 pins



I3–I0: Status register interrupt mask bits.

Note: * The vector number is only read from an external source when an external vector number is specified for the IRL/IRQ interrupt vector number.

Figure 5.8 Interrupt Sequence Flowchart

Section 6 User Break Controller (UBC)

6.1 Overview

The user break controller (UBC) provides functions that simplify program debugging. When break conditions are set in the UBC, a user break interrupt is generated according to the conditions of the bus cycle generated by the CPU or on-chip DMAC (DMAC or E-DMAC).

This function makes it easy to design a sophisticated self-monitoring debugger, enabling programs to be debugged with the chip alone, without using an in-circuit emulator.

6.1.1 Features

The UBC has the following features:

- The following can be set as break conditions:
  - Number of break channels: Four (channels A, B, C, and D)

    User break interrupts can be generated on independent or sequential conditions for channels A, B, C, and D.
  - Sequential break settings
    - Channel A → channel B → channel C → channel D
    - Channel B → channel C → channel D
    - Channel C → channel D
  1. Address: 32-bit masking capability, individual address setting possible (cache bus (CPU), internal bus (DMAC, E-DMAC), X/Y bus)
  2. Data (channels C and D only,): 32-bit masking capability, individual address setting possible (cache bus (CPU), internal bus (DMAC, E-DMAC), X/Y bus)
  3. Bus master: CPU cycle/on-chip DMAC (DMAC, E-DMAC) cycle
  4. Bus cycle: Instruction fetch/data access
  5. Read/write
  6. Operand cycle: Byte/word/longword
- User break interrupt generation on occurrence of break condition

  A user-written user break interrupt exception routine can be executed.
- Processing can be stopped before or after instruction execution in an instruction fetch cycle.
- Break with specification of number of executions (channels C and D only)

  Settable number of executions: maximum $2^{12} - 1$ (4095)
- PC trace function

Section 7 Bus State Controller (BSC)

7.1 Overview

The bus state controller (BSC) manages the address spaces and outputs control signals to allow optimum memory accesses to the five spaces. This enables memories like DRAM, and SDRAM, and peripheral chips, to be linked directly.

7.1.1 Features

The BSC has the following features:

- Address space is managed as five spaces
  - Maximum linear 32 Mbytes for each of the address spaces CS0 to CS4
  - Memory type (DRAM, synchronous DRAM, burst ROM, etc.) can be specified for each space.
  - Bus width (8, 16, or 32 bits) can be selected for each space.
  - Wait state insertion can be controlled for each space.
  - Control signals are output for each space.
- Cache
  - Cache area and cache-through area can be selected by access address.
  - In cache access, in the event of a cache access miss 16 bytes are read consecutively in 4-byte units to fill the cache. Write-through mode/write-back mode can be selected for writes.
  - In cache-through access, access is performed according to access size.
- Refresh
  - Supports $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh (auto-refresh) and self-refresh.
  - Refresh interval can be set by the refresh counter and clock selection.
  - Intensive refreshing by means of refresh count setting (1, 2, 4, 6, or 8)
- Direct interface to DRAM
  - Row/column address multiplex output.
  - Burst transfer during reads, fast page mode for consecutive accesses.
  - TP cycle generation to secure $\overline{\text{RAS}}$ precharge time.
  - EDO mode
- Direct interface to synchronous DRAM
  - Row/column address multiplex output.

9.2.15 CRC Error Frame Counter Register (CEFCR)

Bit:	31	30	29	. . .	19	18	17	16
	—	—	—	. . .	—	—	—	—
Initial value:	0	0	0	. . .	0	0	0	0
R/W:	R	R	R	. . .	R	R	R	R

Bit:	15	14	13	12	11	10	9	8
	CEFC15	CEFC14	CEFC13	CEFC12	CEFC11	CEFC10	CEFC9	CEFC8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	CEFC7	CEFC6	CEFC5	CEFC4	CEFC3	CEFC2	CEFC1	CEFC0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CEFCR is a 16-bit counter that indicates the number of times a frame with a CRC error was received. When the value in this register reaches H'FFFF (65,535), the count is halted. The counter value is cleared to 0 by a write to this register (the write value is immaterial).

Bits 31 to 16—Reserved: These bits are always read as 0. The write value should always be 0.

Bits 15 to 0—CRC Error Frame Count 15 to 0 (CEFC15 to CEFC0): These bits indicate the count of CRC error frames received.

Note: When the Permit Receive CRC Error Frame bit (PRCEF) is set to 1 in the EtherC Mode Register (ECMR), CEFCR is not incremented by reception of a frame with a CRC error.

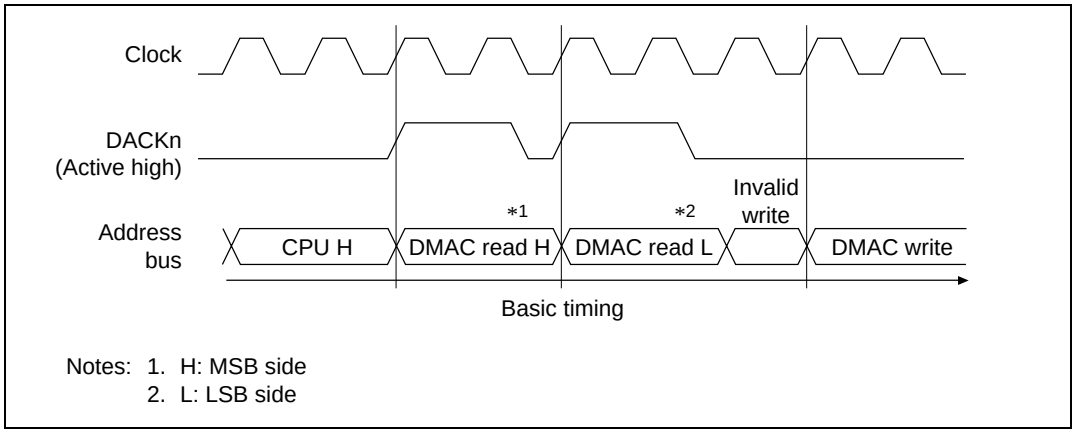


Figure 11.16 DACKn Output in Ordinary Space Accesses (AM = 0, Longword Access to 16-Bit External Device)

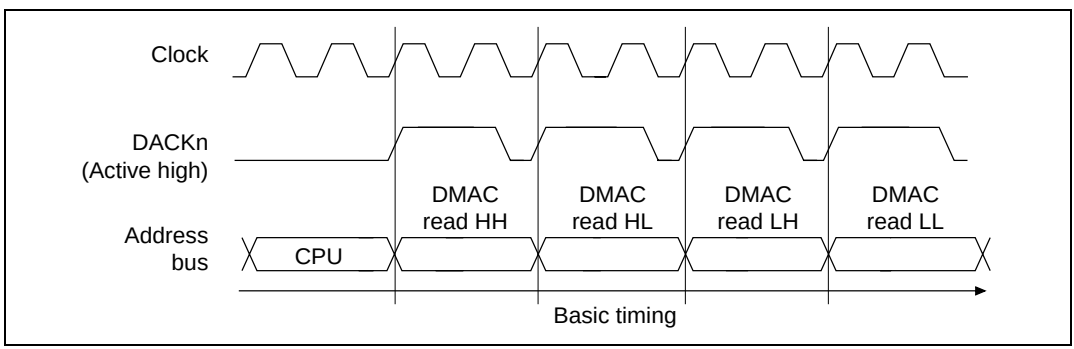


Figure 11.17 DACKn Output in Ordinary Space Accesses (AM = 0, Longword Access to 8-Bit External Device)

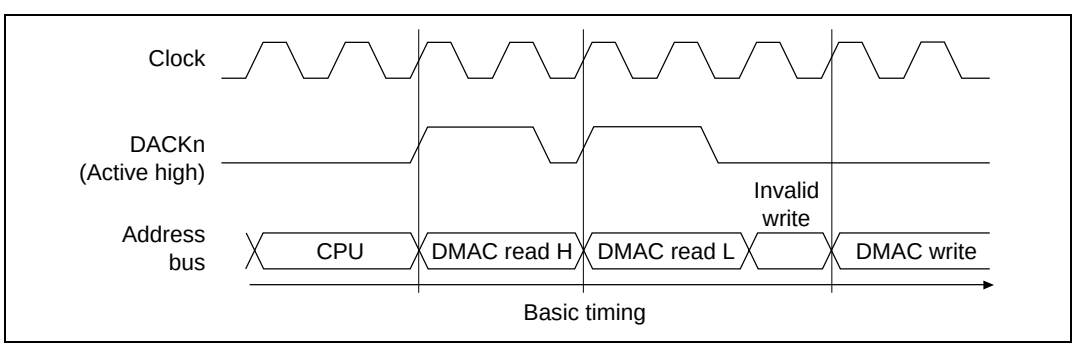


Figure 11.18 DACKn Output in Ordinary Space Accesses (AM = 0, Word Access to 8-Bit External Device)

11.3.8 DMA Transfer End

The DMA transfer ending conditions vary when channels end individually and when both channels end together.

Conditions for Channels Ending Individually: When either of the following conditions is met, the transfer will end in the relevant channel only:

The DMA transfer count register (TCR) value becomes 0.
The DMA enable bit (DE) of the DMA channel control register (CHCR) is cleared to 0.

- Transfer end when TCR = 0

  When the TCR value becomes 0, the DMA transfer for that channel ends and the transfer-end flag bit (TE) is set in CHCR. If the IE (interrupt enable) bit has already been set, a DMAC interrupt (DEI) request is sent to the CPU. For 16-byte transfer, set the number of transfers × 4. Operation is not guaranteed if an incorrect value is set.

  A 16-byte transfer is valid only in auto-request mode or in external request mode with edge detection. When using an external request with level detection or on-chip peripheral module request, do not specify a 16-byte transfer.
- Transfer end when DE = 0 in CHCR

  When the DMA enable bit (DE) in CHCR is cleared, DMA transfers in the affected channel are halted. The TE bit is not set when this happens.

Conditions for Both Channels Ending Simultaneously: Transfers on both channels end when either of the following conditions is met:

The NMIF (NMI flag) bit or AE (address error flag) bit in DMAOR is set to 1.
The DMA master enable (DME) bit is cleared to 0 in DMAOR.

- Transfer end when NMIF = 1 or AE = 1 in DMAOR

  When an NMI interrupt or DMAC address error occurs and the NMIF or AE bit is set to 1 in DMAOR, all channels stop their transfers. The DMA source address register (SAR), destination address register (DAR), and transfer count register (TCR) are all updated by the transfer immediately preceding the halt. When this transfer is the final transfer, TE = 1 and the transfer ends. To resume transfer after NMI interrupt exception handling or address error exception handling, clear the appropriate flag bit. When the DE bit is then set to 1, the transfer on that channel will restart. To avoid this, keep its DE bit at 0. In dual address mode, DMA transfer will be halted after the completion of the following write cycle even when the address error occurs in the initial read cycle. SAR, DAR and TCR are updated by the final transfer.

Bit 4—Break Detect (BRK): Indicates that a receive data break signal has been detected.

Bit 4: BRK	Description
0	A break signal has not been received (Initial value) [Clearing conditions] • In a reset or in standby mode • When 0 is written to BRK after reading BRK = 1
1	A break signal has been received [Setting condition] When data with a framing error is received, and a framing error also occurs in the next receive data (all space “0”)

Note: When a break is detected, transfer to SCFRDR of the receive data (H'00) following detection is halted. When the break ends and the receive signal returns to mark “1”, receive data transfer is resumed.

Bit 3—Framing Error (FER): Indicates a framing error in the data read from the receive FIFO data register (SCFRDR).

Bit 3: FER	Description
0	There is no framing error in the receive data read from SCFRDR (Initial value) [Clearing conditions] • In a reset or in standby mode • When there is no framing error in SCFRDR read data
1	There is a framing error in the receive data read from SCFRDR [Setting condition] When there is a framing error in SCFRDR read data

Bit 2—Parity Error (PER): In asynchronous mode, indicates a parity error in the data read from the receive FIFO data register (SCFRDR).

Bit 2: PER	Description
0	There is no parity error in the receive data read from SCFRDR (Initial value) [Clearing conditions] • In a reset or in standby mode • When there is no parity error in SCFRDR read data
1	There is a parity error in the receive data read from SCFRDR [Setting condition] When there is a parity error in SCFRDR read data

Table 14.3 Examples of Bit Rates and SCBRR Settings in Asynchronous Mode

	Pϕ (MHz)											
	2			2.097152			2.4576			3		
Bit Rate (Bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	–0.04	1	174	–0.26	1	212	0.03
150	1	103	0.16	1	108	0.21	1	127	0.00	1	155	0.16
300	0	207	0.16	0	217	0.21	0	255	0.00	1	77	0.16
600	0	103	0.16	0	108	0.21	0	127	0.00	0	155	0.16
1200	0	51	0.16	0	54	–0.70	0	63	0.00	0	77	0.16
2400	0	25	0.16	0	26	1.14	0	31	0.00	0	38	0.16
4800	0	12	0.16	0	13	–2.48	0	15	0.00	0	19	–2.34
9600	0	6	–6.99	0	6	–2.48	0	7	0.00	0	9	–2.34
19200	0	2	8.51	0	2	13.78	0	3	0.00	0	4	–2.34
31250	0	1	0.00	0	1	4.86	0	1	22.88	0	2	0.00
38400	0	1	–18.62	0	1	–14.67	0	1	0.00	—	—	—

	Pϕ (MHz)											
	3.6864			4			4.9152			5		
Bit Rate (Bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	64	0.70	2	70	0.03	2	86	0.31	2	88	–0.25
150	1	191	0.00	1	207	0.16	1	255	0.00	2	64	0.16
300	1	95	0.00	1	103	0.16	1	127	0.00	1	129	0.16
600	0	191	0.00	0	207	0.16	0	255	0.00	1	64	0.16
1200	0	95	0.00	0	103	0.16	0	127	0.00	0	129	0.16
2400	0	47	0.00	0	51	0.16	0	63	0.00	0	64	0.16
4800	0	23	0.00	0	25	0.16	0	31	0.00	0	32	–1.36
9600	0	11	0.00	0	12	0.16	0	15	0.00	0	15	1.73
19200	0	5	0.00	0	6	–6.99	0	7	0.00	0	7	1.73
31250	—	—	—	0	3	0.00	0	4	–1.70	0	4	0.00
38400	0	2	0.00	0	2	8.51	0	3	0.00	0	3	1.73

Table 14.11 Receive Error Conditions

Receive Error	Abbreviation	Condition	Data Transfer
Overrun error	ORER	Next serial receive operation is completed while there are 16 receive data bytes in SCFRDR	Receive data is not transferred from SCRSR to SCFRDR
Framing error	FER	Stop bit is 0	Receive data is transferred from SCRSR to SCFRDR
Parity error	PER	Received data parity differs from that (even or odd) set in SCSMR	Receive data is transferred from SCRSR to SCFRDR

Figure 14.9 shows an example of the operation for reception in asynchronous mode.

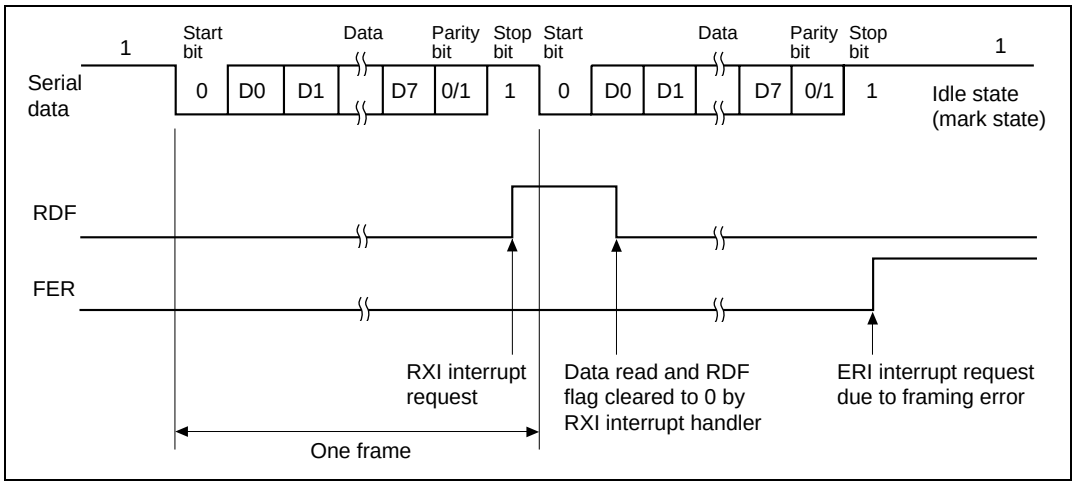


Figure 14.9 Example of SCIF Receive Operation (Example with 8-Bit Data, Parity, One Stop Bit, LSB-First Transfer)

5. When modem control is enabled, the $\overline{\text{RTS}}$ signal is output when SCFRDR is empty. When $\overline{\text{RTS}}$ is 0, reception is possible. When $\overline{\text{RTS}}$ is 1, this indicates that SCFRDR is full and reception is not possible.

   Figure 14.10 shows an example of the operation when modem control is used.

14.3.5 Use of Transmit/Receive FIFO Buffers

The SCIF has independent 16-stage FIFO buffers for transmission and reception. The configuration of these buffers is shown in figure 14.23.

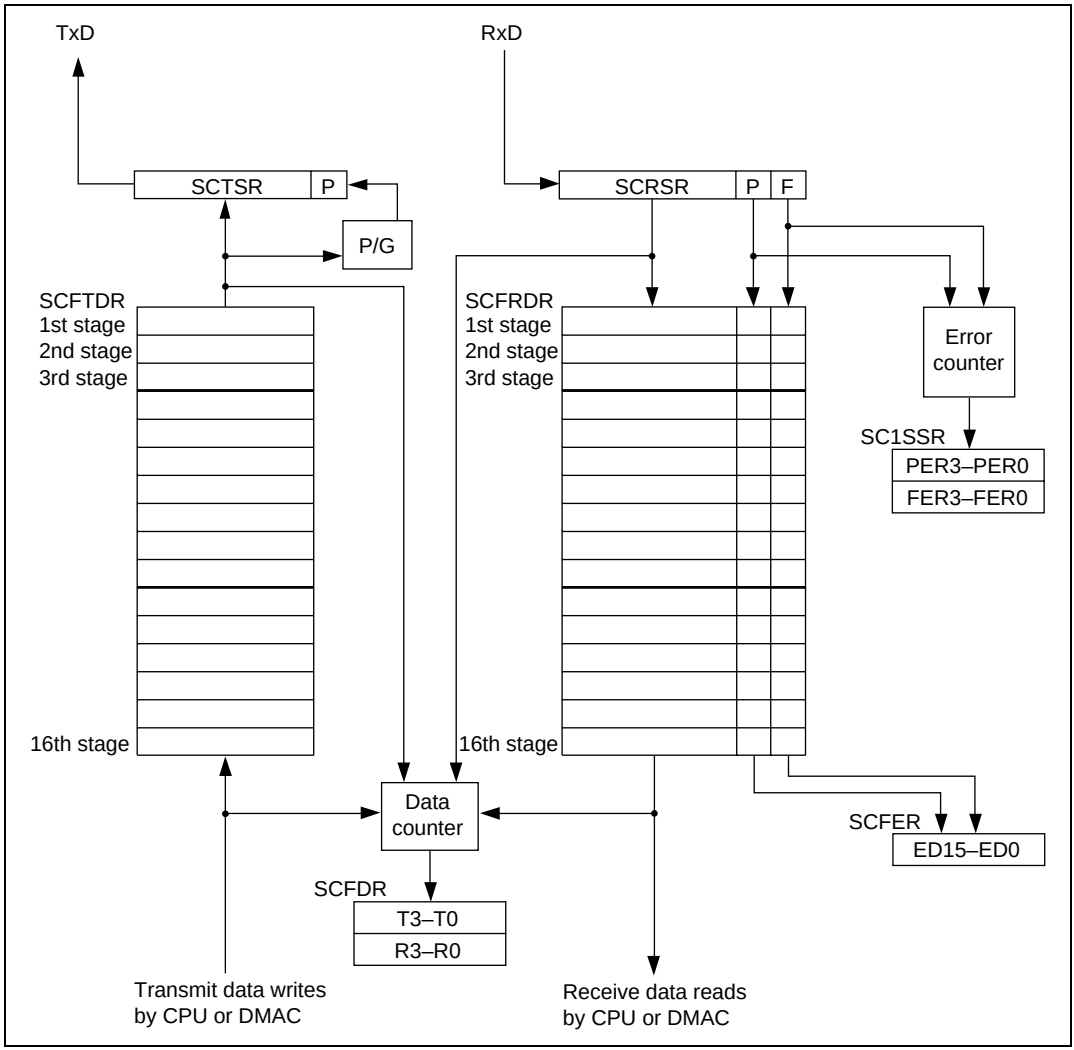


Figure 14.23 Transmit/Receive FIFO Configuration

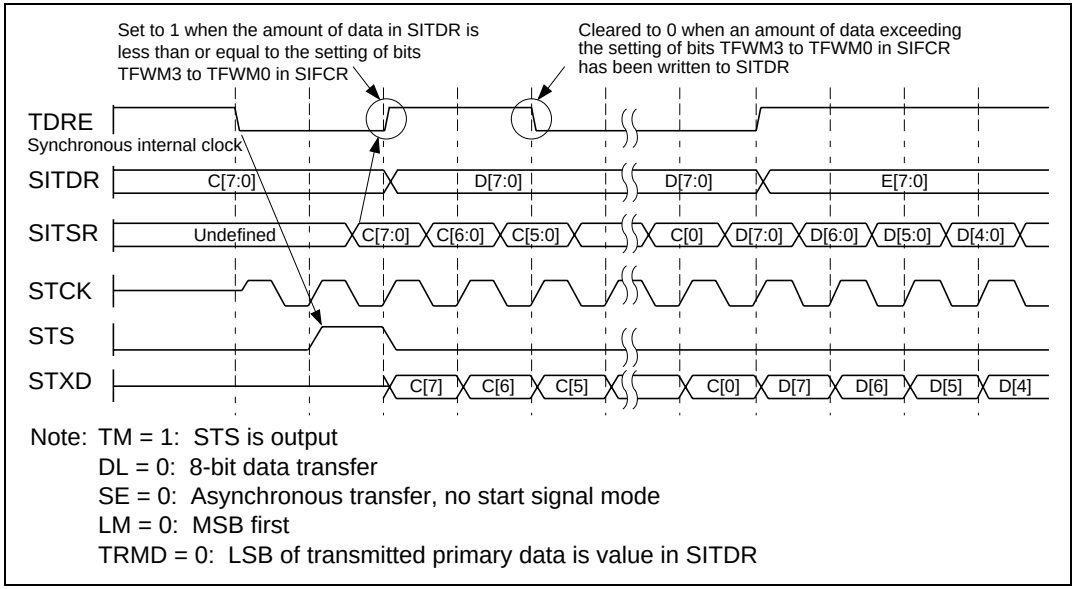


Figure 15.9 Transmission: Continuous Transfer Mode (TM = 1 Mode)/MSB First

Figure 15.10 shows interval transfer mode when TM is cleared to 0 in SICTR and with LSB first.

Figure 15.11 shows continuous transfer mode when TM is cleared to 0 in SICTR and with LSB first.

Figure 15.12 shows interval transfer mode when TM is set to 1 in SICTR and with LSB first.

Figure 15.13 shows continuous transfer mode when TM is set to 1 in SICTR and with LSB first.

Item	Channel 0	Channel 1	Channel 2
DMAC activation	TGR compare match or input capture	—	—
Interrupt sources	5 sources • Compare match or input capture 0A • Compare match or input capture 0B • Compare match or input capture 0C • Compare match or input capture 0D • Overflow	4 sources • Compare match or input capture 1A • Compare match or input capture 1B • Overflow • Underflow	4 sources • Compare match or input capture 2A • Compare match or input capture 2B • Overflow • Underflow

Note: — : Not possible

17.1.3 Pin Configuration

Table 17.2 shows the pin configuration of the TPU.

Table 17.2 Pin Configuration

Channel	Name	Abbreviation	I/O	Function
All	Clock input A	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input)
	Clock input B	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input)
	Clock input C	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input)
	Clock input D	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	Input capture/output compare match A0	TIOCA0	I/O	TGR0A input capture input/output compare output/PWM output pin
	Input capture/output compare match B0	TIOCB0	I/O	TGR0B input capture input/output compare output/PWM output pin
	Input capture/output compare match C0	TIOCC0	I/O	TGR0C input capture input/output compare output/PWM output pin
	Input capture/output compare match D0	TIOCD0	I/O	TGR0D input capture input/output compare output/PWM output pin
1	Input capture/output compare match A1	TIOCA1	I/O	TGR1A input capture input/output compare output/PWM output pin
	Input capture/output compare match B1	TIOCB1	I/O	TGR1B input capture input/output compare output/PWM output pin
2	Input capture/output compare match A2	TIOCA2	I/O	TGR2A input capture input/output compare output/PWM output pin
	Input capture/output compare match B2	TIOCB2	I/O	TGR2B input capture input/output compare output/PWM output pin

Pin No.	Pin Name	Input/Output	Bit No.
62	D20	Input	269
		Output	268
		Output enable	267
63	D21	Input	266
		Output	265
		Output enable	264
64	D22	Input	263
		Output	262
		Output enable	261
65	D23	Input	260
		Output	259
		Output enable	258
68	D24	Input	257
		Output	256
		Output enable	255
70	D25	Input	254
		Output	253
		Output enable	252
71	D26	Input	251
		Output	250
		Output enable	249
72	D27	Input	248
		Output	247
		Output enable	246
73	D28	Input	245
		Output	244
		Output enable	243
74	D29	Input	242
		Output	241
		Output enable	240

21.2 Register Descriptions

21.2.1 Standby Control Register 1 (SBYCR1)

Bit:	7	6	5	4	3	2	1	0
	SBY	HIZ	MSTP5 (UBC)	MSTP4 (DMAC)	MSTP3 (DSP)	—	MSTP1 (FRT)	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R/W	R

Standby control register 1 (SBYCR1) is an 8-bit read/write register that sets the power-down mode. SBYCR is initialized to H'00 by a reset.

Bit 7—Standby (SBY): Specifies transition to standby mode. To enter the standby mode, halt the WDT (set the TME bit in WTCSR to 0) and set the SBY bit.

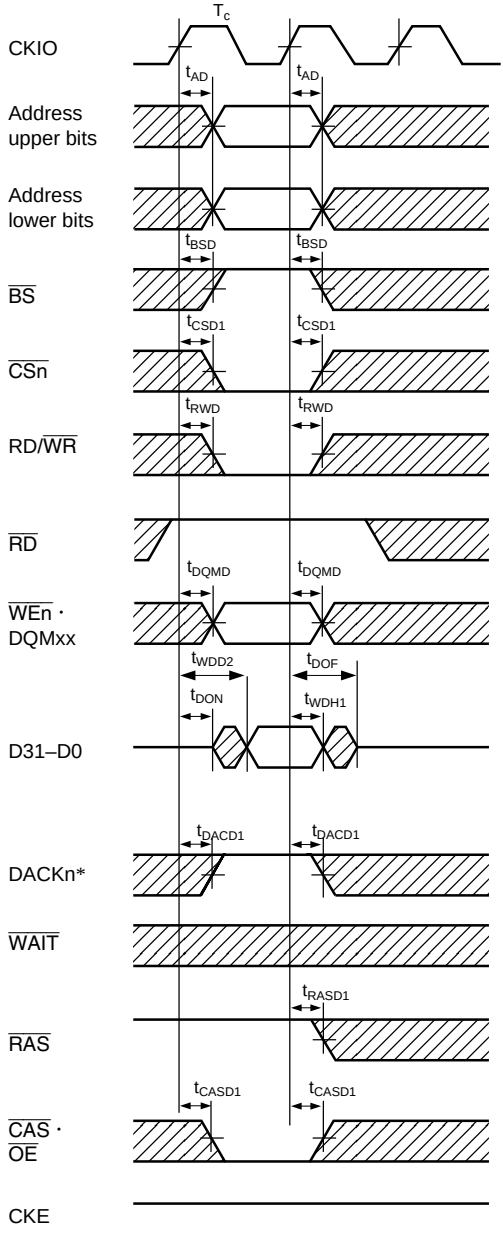
Bit 7: SBY	Description	
0	Executing a SLEEP instruction puts the chip into sleep mode	(Initial value)
1	Executing a SLEEP instruction puts the chip into standby mode	

Bit 6—Port High Impedance (HIZ): Selects whether output pins are set to high impedance or retain the output state in standby mode. When HIZ = 0 (initial state), the specified pin retains its output state. When HIZ = 1, the pin goes to the high-impedance state. See Appendix B.1, Pin States during Resets, Power-Down States and Bus Release State, for which pins are controlled.

Bit 6: HIZ	Description	
0	Pin state retained in standby mode	(Initial value)
1	Pin goes to high impedance in standby mode	

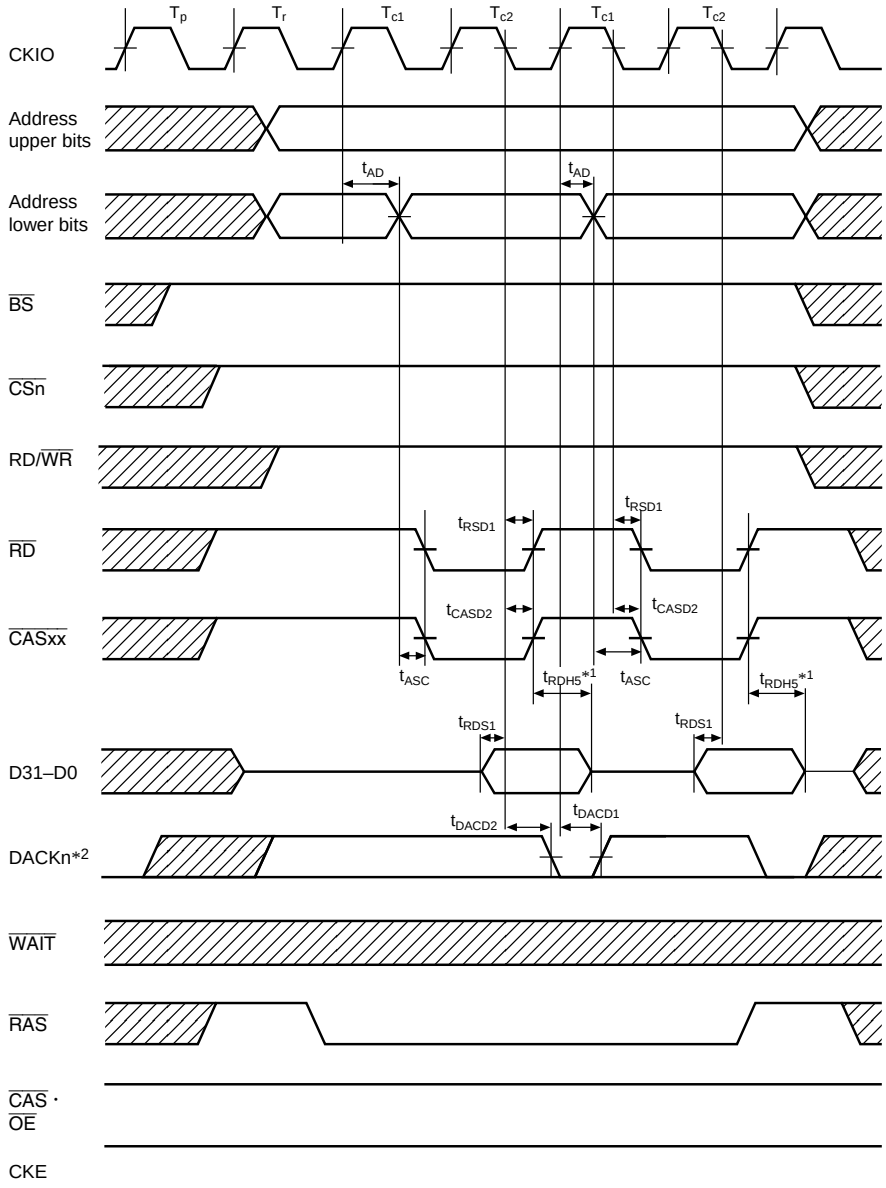
Bit 5—Module Stop 5 (MSTP5): Specifies halting the clock supply to the user break controller (UBC). When the MSTP5 bit is set to 1, the supply of the clock to the UBC is halted. When the clock halts, the UBC registers retain their pre-halt state. Do not set this bit while the UBC is running.

Bit 5: MSTP5	Description	
0	UBC running	(Initial value)
1	Clock supply to UBC halted	



Note: * DACKn waveform when active-high is specified

Figure 22.25 Synchronous DRAM Write Cycle (Bank Active, Same Row Access, Iϕ:Eϕ = 1:1)



Notes: 1. t_{RDH5} is measured from the rise of $\overline{RD}$ or $\overline{CASxx}$, whichever comes first.
2. DACKn waveform when active-high is specified

Figure 22.37 DRAM Burst Read Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Wait)

Address	Register Name	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF FD74	MALR	—	—	—	—	—	—	—	—	EtherC
H'FFFF FD75		—	—	—	—	—	—	—	—	
H'FFFF FD76		MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	
H'FFFF FD77		MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	
H'FFFF FD78	RFLR	—	—	—	—	—	—	—	—	
H'FFFF FD79		—	—	—	—	—	—	—	—	
H'FFFF FD7A		—	—	—	—	RFL11	RFL10	RFL9	RFL8	
H'FFFF FD7B		RFL7	RFL6	RFL5	RFL4	RFL3	RFL2	RFL1	RFL0	
H'FFFF FD7C	PSR	—	—	—	—	—	—	—	—	
H'FFFF FD7D		—	—	—	—	—	—	—	—	
H'FFFF FD7E		—	—	—	—	—	—	—	—	
H'FFFF FD7F		—	—	—	—	—	—	—	LMON	
H'FFFF FD80	TROCR	—	—	—	—	—	—	—	—	
H'FFFF FD81		—	—	—	—	—	—	—	—	
H'FFFF FD82		TROC15	TROC14	TROC13	TROC12	TROC11	TROC10	TROC9	TROC8	
H'FFFF FD83		TROC7	TROC6	TROC5	TROC4	TROC3	TROC2	TROC1	TROC0	
H'FFFF FD84	CDCR	—	—	—	—	—	—	—	—	
H'FFFF FD85		—	—	—	—	—	—	—	—	
H'FFFF FD86		COLDC15	COLDC14	COLDC13	COLDC12	COLDC11	COLDC10	COLDC9	COLDC8	
H'FFFF FD87		COLDC7	COLDC6	COLDC5	COLDC4	COLDC3	COLDC2	COLDC1	COLDC0	
H'FFFF FD88	LCCR	—	—	—	—	—	—	—	—	
H'FFFF FD89		—	—	—	—	—	—	—	—	
H'FFFF FD8A		LCC15	LCC14	LCC13	LCC12	LCC11	LCC10	LCC9	LCC8	
H'FFFF FD8B		LCC7	LCC6	LCC5	LCC4	LCC3	LCC2	LCC1	LCC0	
H'FFFF FD8C	CNDCR	—	—	—	—	—	—	—	—	
H'FFFF FD8D		—	—	—	—	—	—	—	—	
H'FFFF FD8E		CNDC15	CNDC14	CNDC13	CNDC12	CNDC11	CNDC10	CNDC9	CNDC8	
H'FFFF FD8F		CNDC7	CNDC6	CNDC5	CNDC4	CNDC3	CNDC2	CNDC1	CNDC0	
H'FFFF FD90	IFLCR	—	—	—	—	—	—	—	—	
H'FFFF FD91		—	—	—	—	—	—	—	—	
H'FFFF FD92		IFLC15	IFLC14	IFLC13	IFLC12	IFLC11	IFLC10	IFLC9	IFLC8	
H'FFFF FD93		IFLC7	IFLC6	IFLC5	IFLC4	IFLC3	IFLC2	IFLC1	IFLC0	