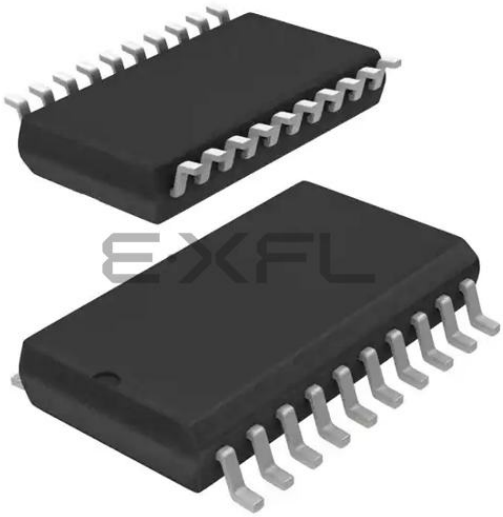

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	240 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f262kpf-g-sne2

Clock supervisor counter

■ Built-in clock supervisor counter function

Programmable port input voltage level

■ CMOS input level / hysteresis input level

Dual operation Flash memory

■ The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

■ Protects the content of the Flash memory

(Continued)

Part number / Parameter	MB95F262H	MB95F263H	MB95F264H	MB95F262K	MB95F263K	MB95F264K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-24P-M07 LCC-32P-M19 FPT-20P-M09 FPT-20P-M10					

MB95280H Series

Part number / Parameter	MB95F282H	MB95F283H	MB95F284H	MB95F282K	MB95F283K	MB95F284K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected by software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 12 • CMOS I/O : 11 • N-ch open drain : 1			• I/O ports (Max) : 13 • CMOS I/O : 11 • N-ch open drain : 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-internal CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. • The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	5 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	1 channel					
	• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	6 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					

(Continued)

2. Packages and Corresponding Products

Package \ Part number	MB95F262H	MB95F262K	MB95F263H	MB95F263K	MB95F264H	MB95F264K	MB95F272H	MB95F272K	MB95F273H	MB95F273K	MB95F274H	MB95F274K
DIP-24P-M07	O	O	O	O	O	O	X	X	X	X	X	X
FPT-20P-M09	O	O	O	O	O	O	X	X	X	X	X	X
FPT-20P-M10	O	O	O	O	O	O	X	X	X	X	X	X
DIP-16P-M06	X	X	X	X	X	X	X	X	X	X	X	X
FPT-16P-M06	X	X	X	X	X	X	X	X	X	X	X	X
DIP-8P-M03	X	X	X	X	X	X	O	O	O	O	O	O
FPT-8P-M08	X	X	X	X	X	X	O	O	O	O	O	O
LCC-32P-M19	O	O	O	O	O	O	X	X	X	X	X	X

Package \ Part number	MB95F282H	MB95F282K	MB95F283H	MB95F283K	MB95F284H	MB95F284K
DIP-24P-M07	X	X	X	X	X	X
FPT-20P-M09	X	X	X	X	X	X
FPT-20P-M10	X	X	X	X	X	X
DIP-16P-M06	O	O	O	O	O	O
FPT-16P-M06	O	O	O	O	O	O
DIP-8P-M03	X	X	X	X	X	X
FPT-8P-M08	X	X	X	X	X	X
LCC-32P-M19	O	O	O	O	O	O

O: Available

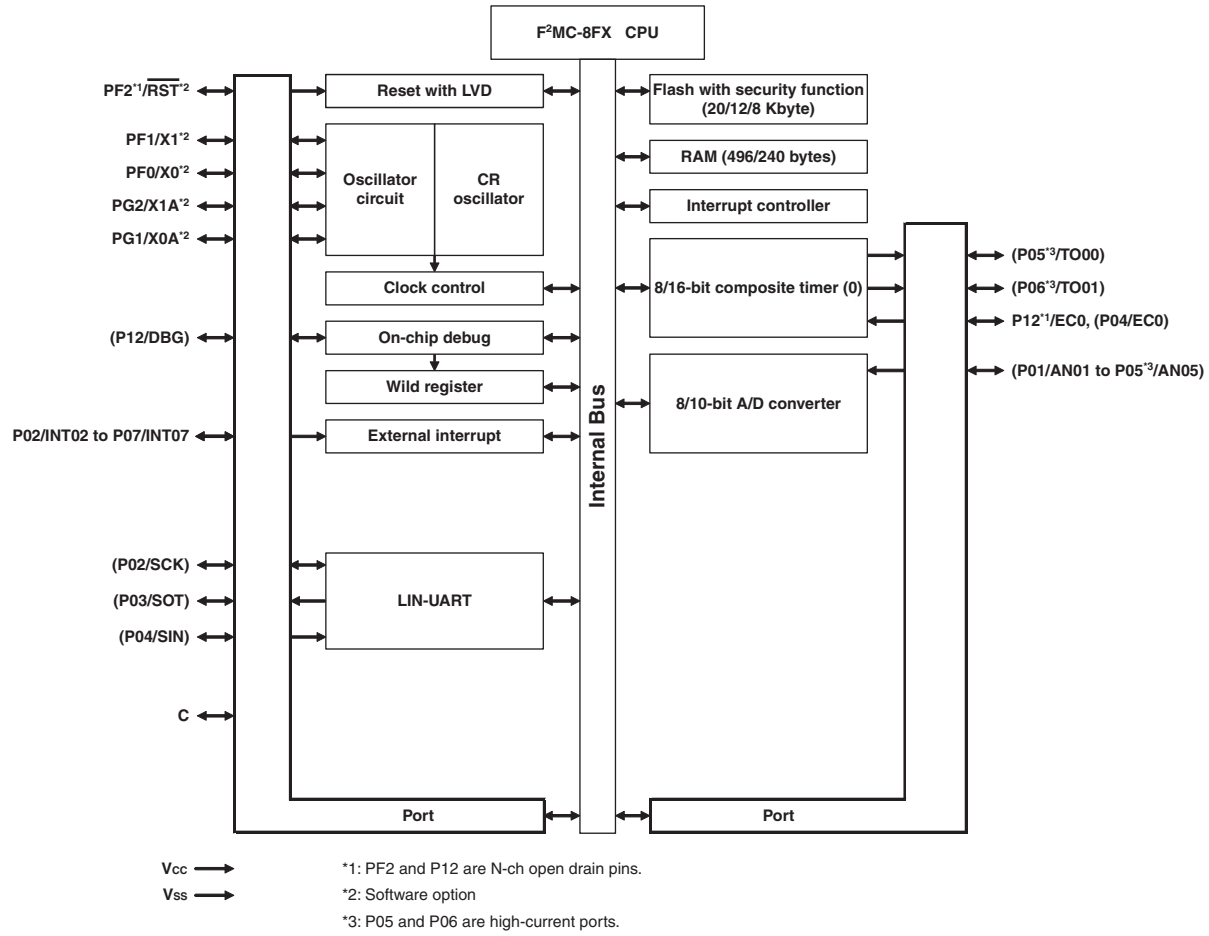
X: Unavailable

5. Pin Description (MB95260H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	Vss	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	Vcc	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.
9	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin
16	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

(Continued)

16. Block Diagram (MB95280H Series)



Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FE6_H$, $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000011_B
$0FE9_H$	CMCR	Clock monitoring control register	R/W	00000000_B
$0FEA_H$	CMDR	Clock monitoring data register	R/W	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (Upper)	R/W	$XXXXXXXX_B$
$0FEC_H$	WDTL	Watchdog timer selection ID register (Lower)	R/W	$XXXXXXXX_B$
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$ to $0FFF_H$	—	(Disabled)	—	—

R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

19. I/O Map (MB95270H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	—	(Disabled)	—	—
0017_H	—	(Disabled)	—	—
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	—	(Disabled)	—	—
$002B_H$	—	(Disabled)	—	—
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	—	(Disabled)	—	—
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	—	(Disabled)	—	—
0039_H	—	(Disabled)	—	—
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	—	(Disabled)	—	—

(Continued)

21. Interrupt Source Table (MB95260H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
—	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (Upper)	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
—	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (Lower)	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

22. Interrupt Source Table (MB95270H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
—	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
—	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
—	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
—					
—	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
—	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
—	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
—	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
—	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
—	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
—	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

24. Electrical Characteristics

24.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} - 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} - 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} - 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	- 2	+ 2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63*4
	I_{OL2}		15		P05, P06, P62 and P63*4
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current= operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	- 15	mA	Other than P05, P06, P62 and P63*4
	I_{OH2}		- 15		P05, P06, P62 and P63*4
"H" level average current	I_{OHAV1}	—	- 4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OHAV2}		- 8		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	- 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	- 50	mA	Total average output current= operating current ´ operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	- 40	+ 85	°C	
Storage temperature	Tstg	- 55	+ 150	°C	

(Continued)

24.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P04	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04	*1	V_{SS} - 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	V_{SS} - 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} - 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	PF2, P12	—	V_{SS} - 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P05, P06, P12, P62, P63, PF2*2	I_{OH} = - 4 mA	V_{CC} - 0.5	—	—	V	
	V_{OH2}	P05, P06, P62, P63*2	I_{OH} = - 8 mA	V_{CC} - 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05, P06, P62, P63*2	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P05, P06, P62, P63*2	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	- 5	—	+ 5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00 to P07, PG1, PG2*3*4	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

24.4 AC Characteristics

24.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1 : open	1	—	12	MHz	When the main external clock is used
		X0, X1	*1	1	—	32.5	MHz	
	F_{CRH}	—	—	9.7	10	10.3	MHz	When the main CR clock is used*2 3.3 V ≤ Vcc ≤ 5.5 V(-40 °C ≤ T_A ≤ + 40 °C) 2.4 V ≤ Vcc < 3.3 V(0 °C ≤ T_A ≤ + 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.55	10	10.45	MHz	When the main CR clock is used*2 3.3 V ≤ Vcc ≤ 5.5 V (+ 40 °C < T_A ≤ + 85 °C)
				7.64	8	8.36	MHz	
				0.955	1	1.045	MHz	
				9.5	10	10.5	MHz	When the main CR clock is used*2 2.4 V≤ Vcc < 3.3 V (-40 °C ≤ T_A < 0 °C, + 40 °C < T_A ≤ + 85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
				9.7	10	10.3	MHz	When the main CR clock is used*3 2.4 V ≤ Vcc ≤ 5.5 V(0 °C ≤ T_A ≤ + 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.5	10	10.5	MHz	When the main CR clock is used*3 2.4 V ≤ Vcc ≤ 5.5 V (-40 °C ≤ T_A < 0 °C, ＋40 °C < T_A ≤＋85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1 : open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*1	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used

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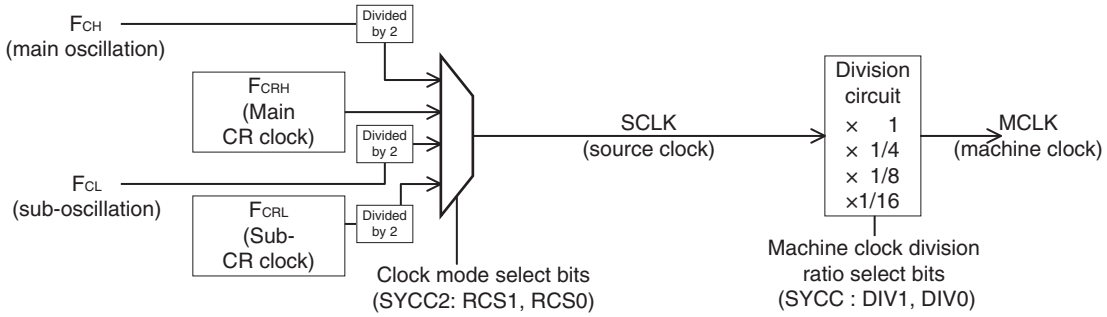
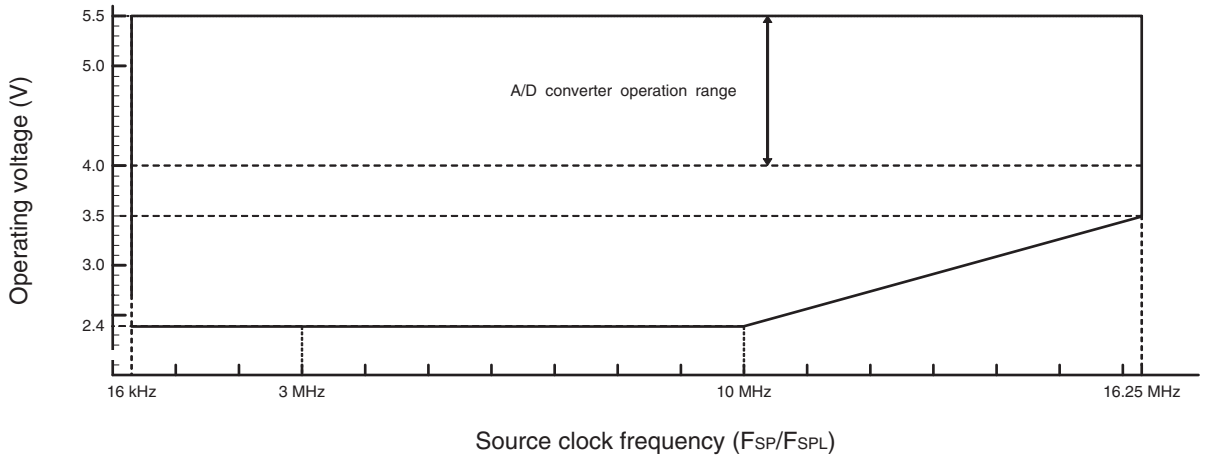
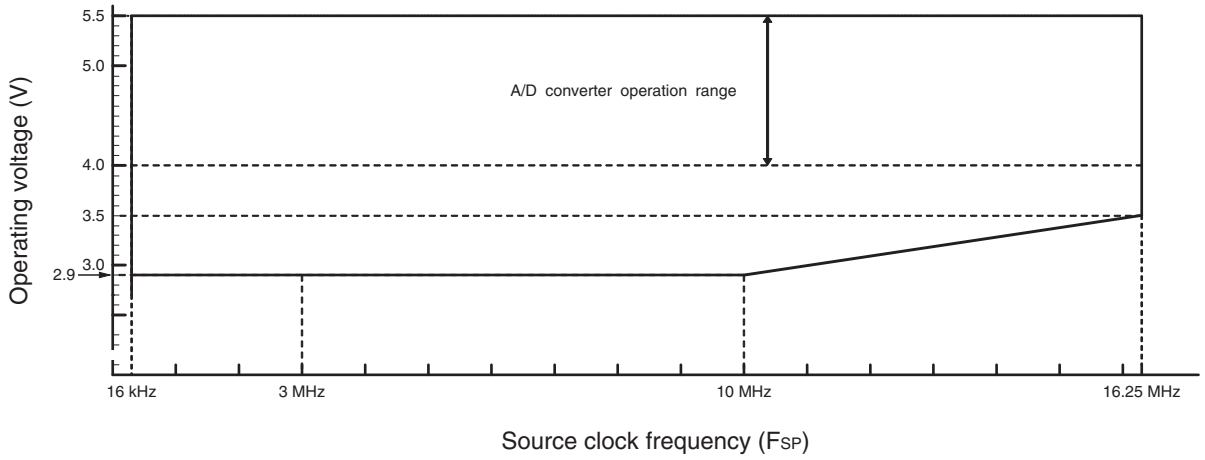
Schematic diagram of the clock generation block



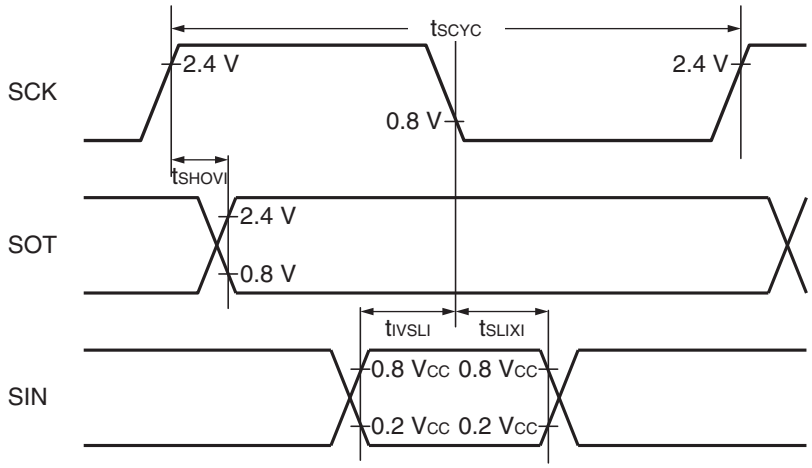
Operating voltage - Operating frequency (When T_A = -40°C to + 85°C)
MB95260H/270H/280H (without the on-chip debug function)



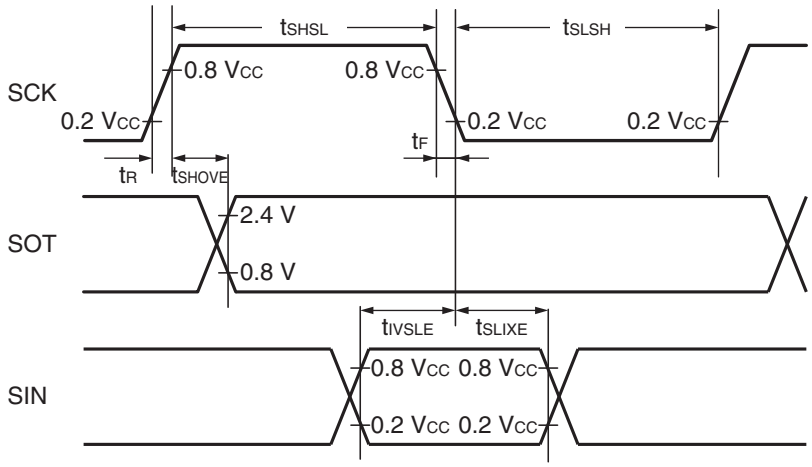
Operating voltage - Operating frequency (When T_A = -40°C to + 85°C)
MB95260H/270H/280H (with the on-chip debug function)



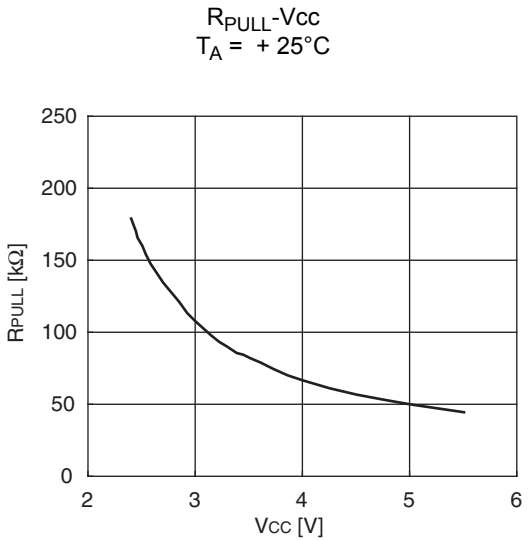
Internal shift clock mode



External shift clock mode



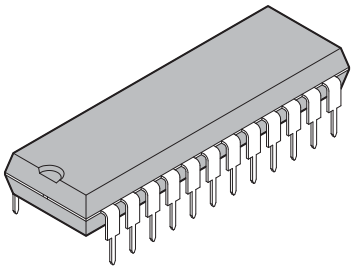
Pull-up



26. Mask Options

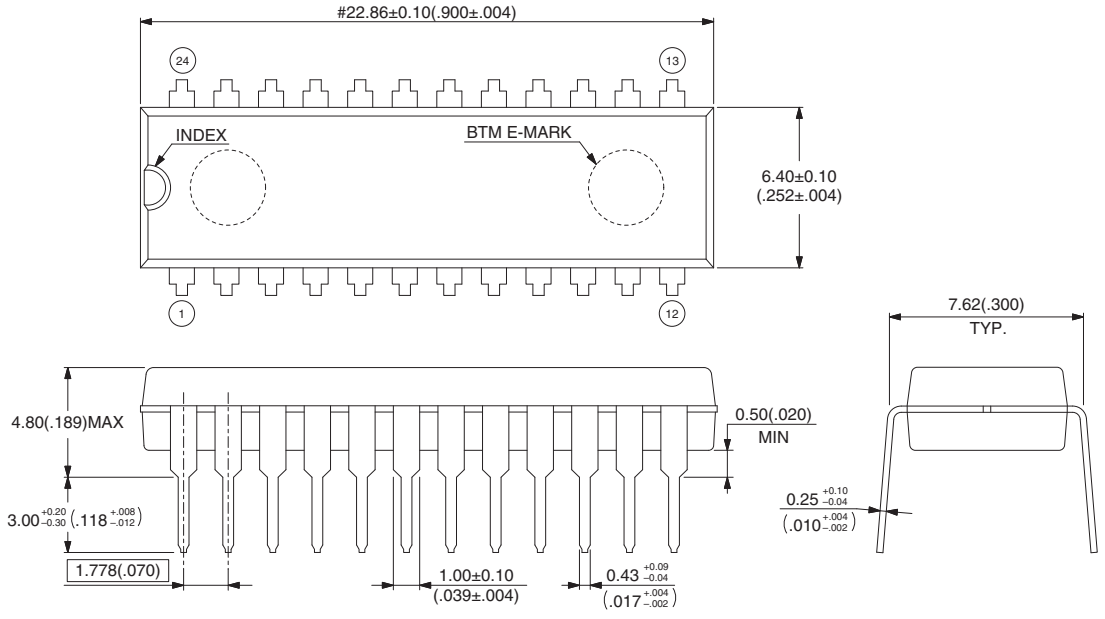
No.	Part Number	MB95F262H MB95F263H MB95F264H MB95F272H MB95F273H MB95F274H MB95F282H MB95F283H MB95F284H	MB95F262K MB95F263K MB95F264K MB95F272K MB95F273K MB95F274K MB95F282K MB95F283K MB95F284K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

28. Package Dimension

24-pin plastic SDIP		
 (DIP-24P-M07)	Lead pitch	1.778 mm
	Package width × package length	6.40 mm × 22.86 mm
	Sealing method	Plastic mold
	Mounting height	4.80 mm Max

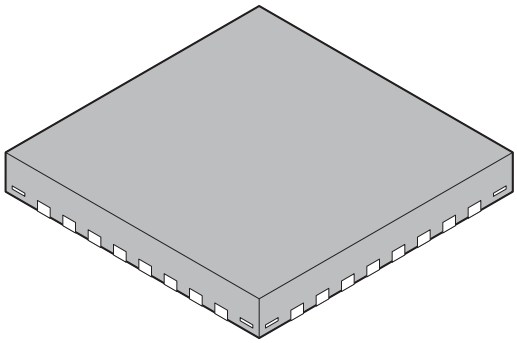
24-pin plastic SDIP
(DIP-24P-M07)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.

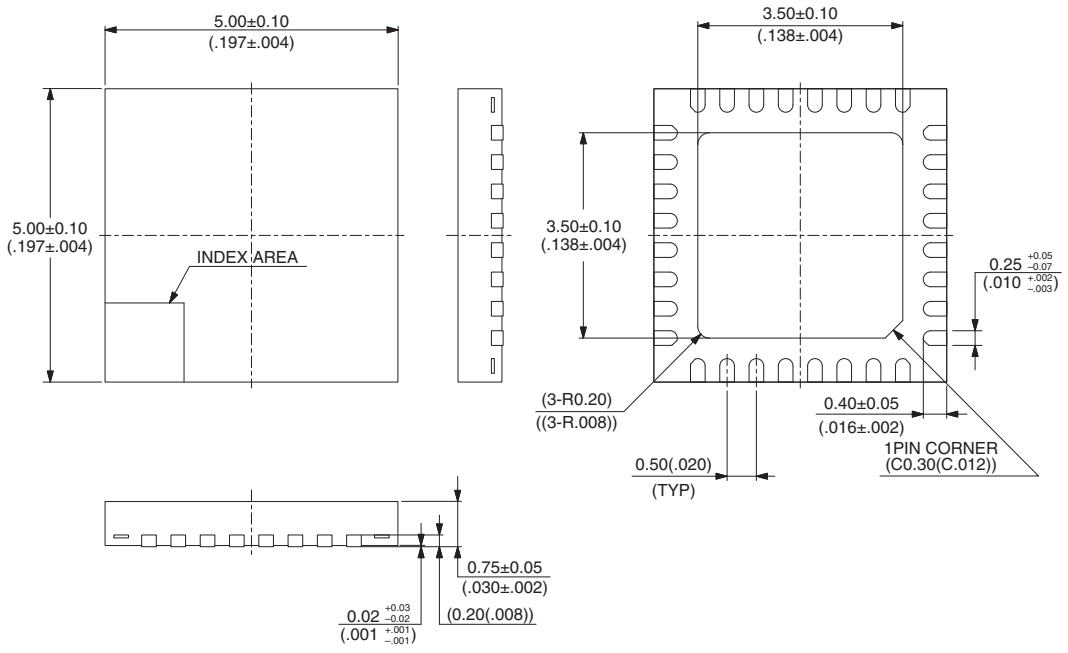


Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

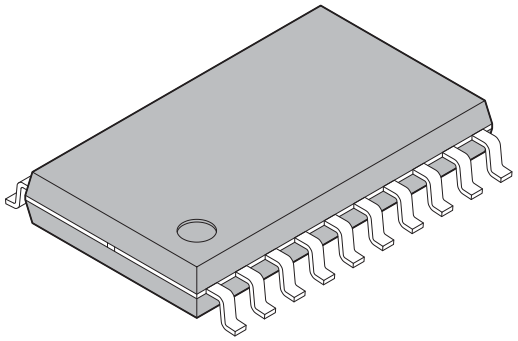
32-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g
(LCC-32P-M19)		

32-pin plastic QFN
(LCC-32P-M19)



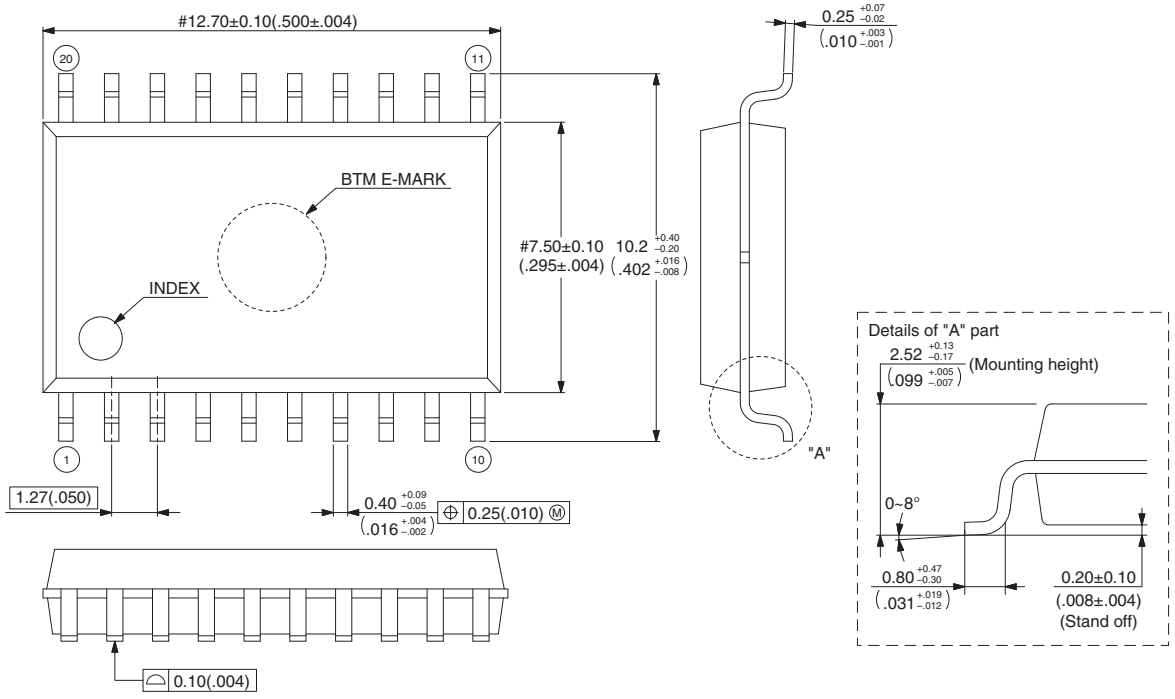
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

20-pin plastic SOP		
 (FPT-20P-M09)	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 12.70 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.65 mm Max

20-pin plastic SOP
(FPT-20P-M09)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)