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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f263kpft-g-sne2

(Continued)

Part number / Parameter	MB95F262H	MB95F263H	MB95F264H	MB95F262K	MB95F263K	MB95F264K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-24P-M07 LCC-32P-M19 FPT-20P-M09 FPT-20P-M10					

MB95270H Series

Part number / Parameter	MB95F272H	MB95F273H	MB95F274H	MB95F272K	MB95F273K	MB95F274K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected by software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 4 • CMOS I/O : 3 • N-ch open drain : 1			• I/O ports (Max) : 5 • CMOS I/O : 3 • N-ch open drain : 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-internal CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	No LIN-UART					
8/10-bit A/D converter	2 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	1 channel					
	• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	2 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-8P-M03 FPT-8P-M08					

(Continued)

Part number / Parameter	MB95F282H	MB95F283H	MB95F284H	MB95F282K	MB95F283K	MB95F284K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	LCC-32P-M19 DIP-16P-M06 FPT-16P-M06					

5. Pin Description (MB95260H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	Vss	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	Vcc	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.
9	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin
16	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

(Continued)

8. Pin Description (MB95270H Series, 8 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	V_{SS}	—	Power supply pin (GND)
2	V_{CC}	—	Power supply pin
3	C	—	Capacitor connection pin
4	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This pin is a dedicated reset pin in MB95F272H/F273H/F274H.
5	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
6	P05	E	General-purpose I/O port High-current pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
7	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
8	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

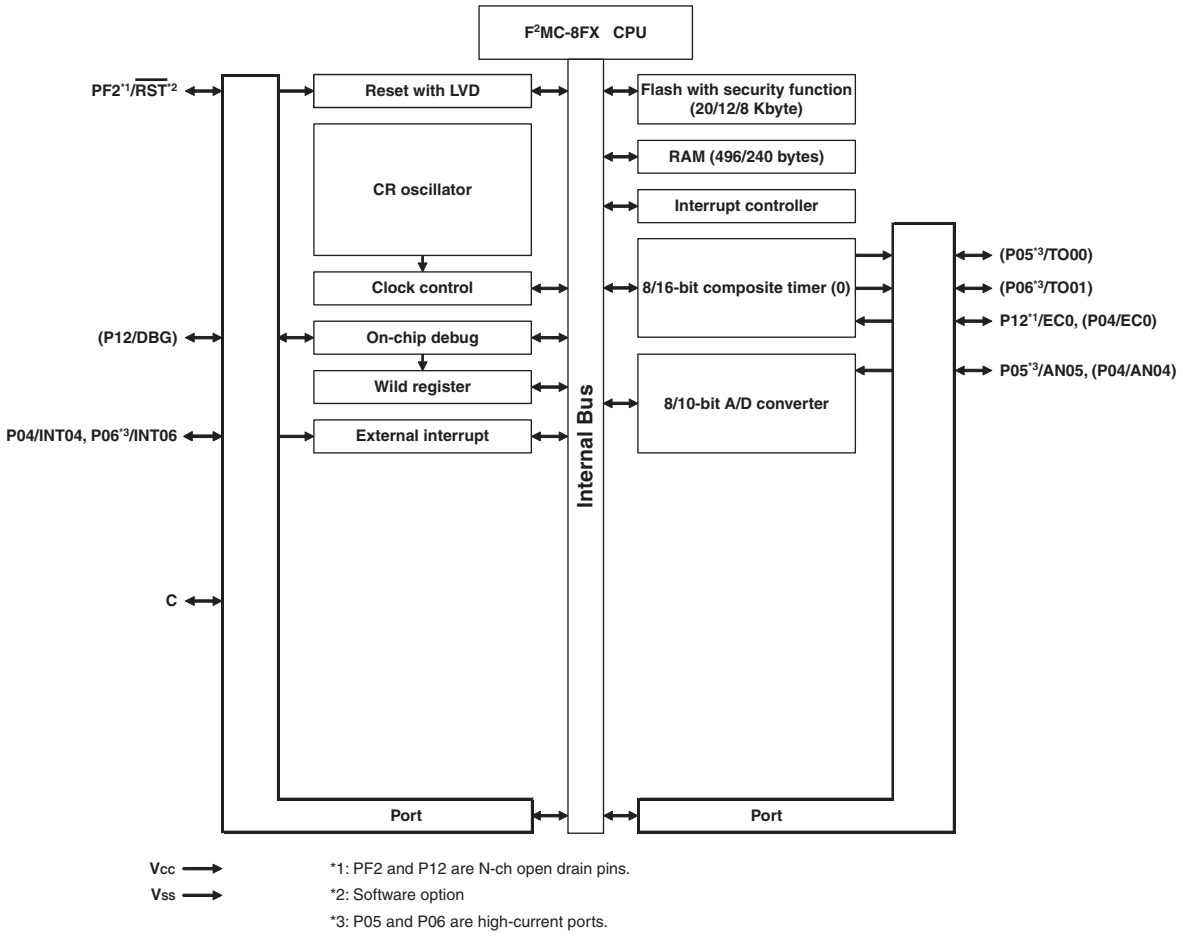
*: For the I/O circuit types, see “11. I/O Circuit Type”.

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
21	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
24	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
25	NC	—	It is an internally connected pin. Always leave it unconnected.
26	NC	—	It is an internally connected pin. Always leave it unconnected.
27	NC	—	It is an internally connected pin. Always leave it unconnected.
28	NC	—	It is an internally connected pin. Always leave it unconnected.
29	NC	—	It is an internally connected pin. Always leave it unconnected.
30	NC	—	It is an internally connected pin. Always leave it unconnected.
31	NC	—	It is an internally connected pin. Always leave it unconnected.
32	NC	—	It is an internally connected pin. Always leave it unconnected.

*: For the I/O circuit types, see “11. I/O Circuit Type”.

15. Block Diagram (MB95270H Series)



Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

Address	Register abbreviation	Register name	R/W	Initial value
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$

(Continued)

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(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CCTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz Time-base timer mode T_A = + 25°C	—	1.1	3	mA	
	I_{CCH}		V_{CC} = 5.5 V Substop mode T_A = + 25°C	—	3.5	22.5	µA	Main stop mode for single external clock selection
	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	37	54	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	0.5	0.6	mA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

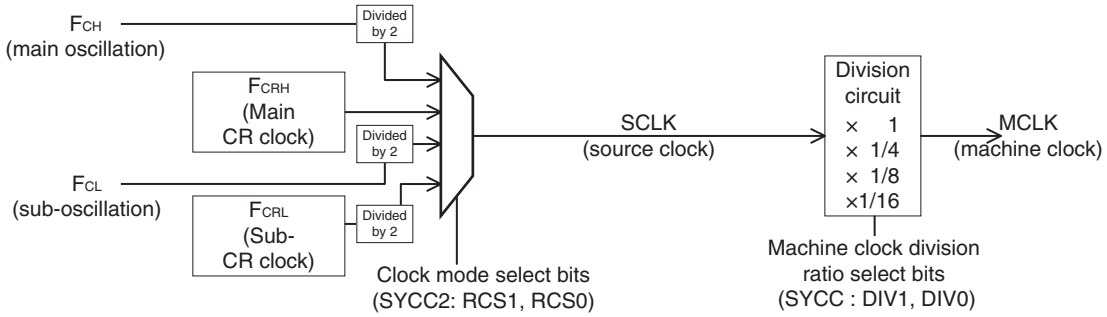
*1: The input level of P04 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2: P62 and P63 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.

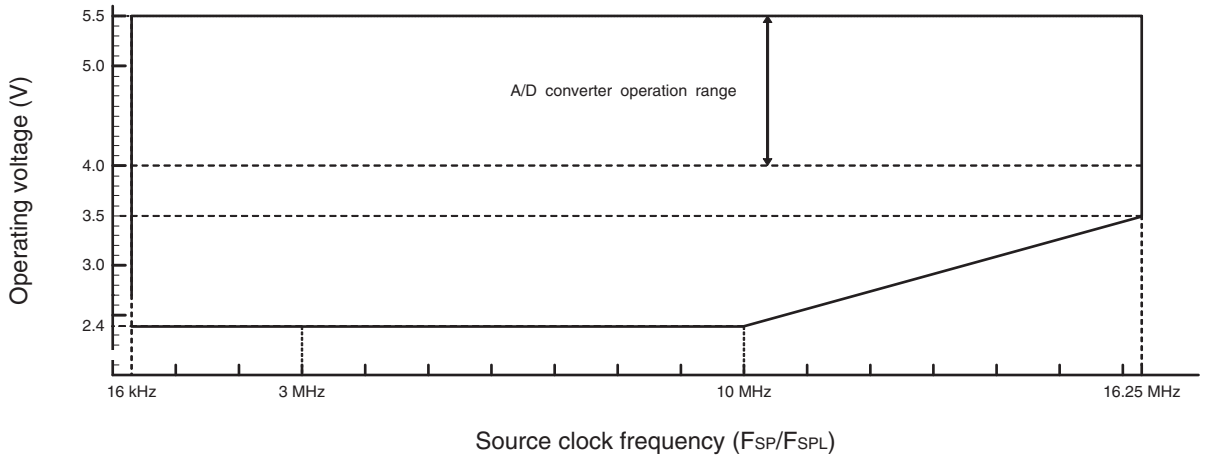
*3: P00 is only available on MB95F262H/F262K/F263H/F263K/F264H/F264K. P01, P02, P03, P07, PG1 and PG2 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K.

*4:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See “24.4. AC Characteristics: 24.4.1. Clock Timing” for F_{CH} and F_{CL}.
- See “24.4. AC Characteristics: 24.4.2. Source Clock / Machine Clock” for F_{MP} and F_{MPL}.

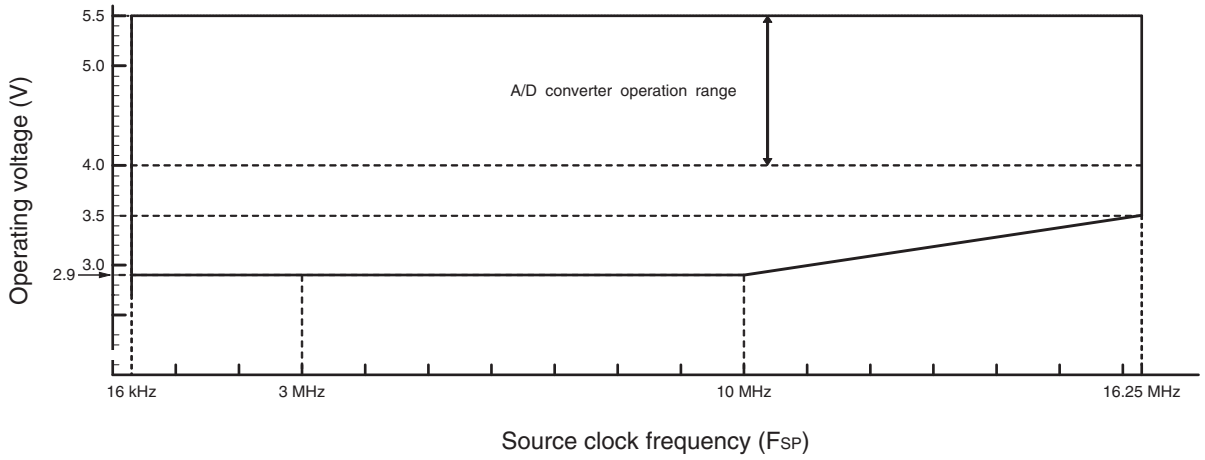
Schematic diagram of the clock generation block



Operating voltage - Operating frequency (When T_A = -40°C to + 85°C)
MB95260H/270H/280H (without the on-chip debug function)



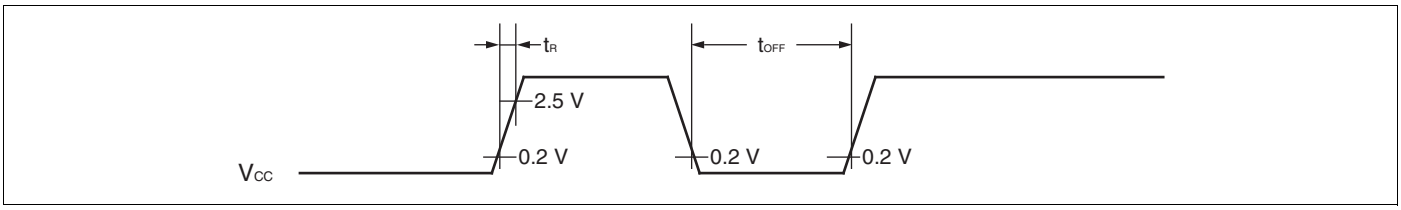
Operating voltage - Operating frequency (When T_A = -40°C to + 85°C)
MB95260H/270H/280H (with the on-chip debug function)



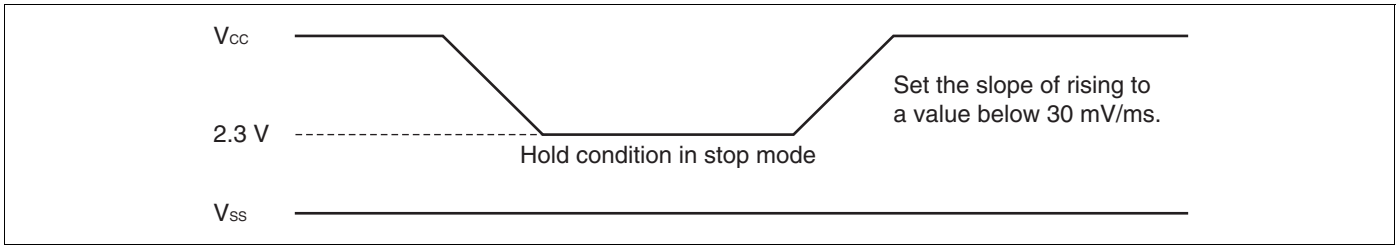
24.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

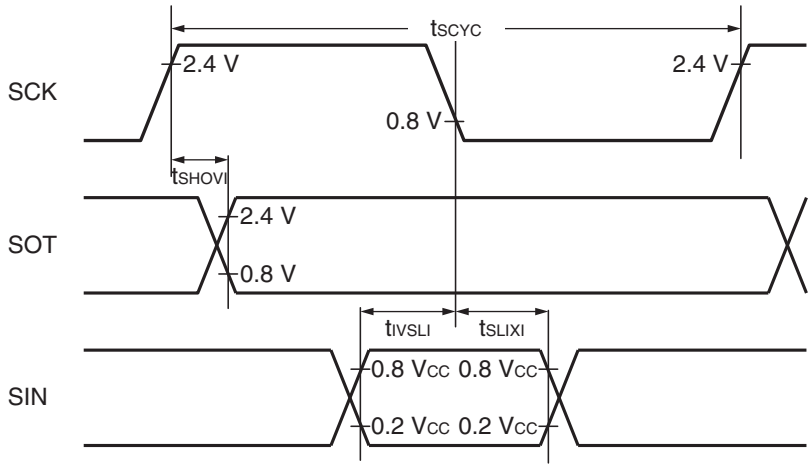
Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



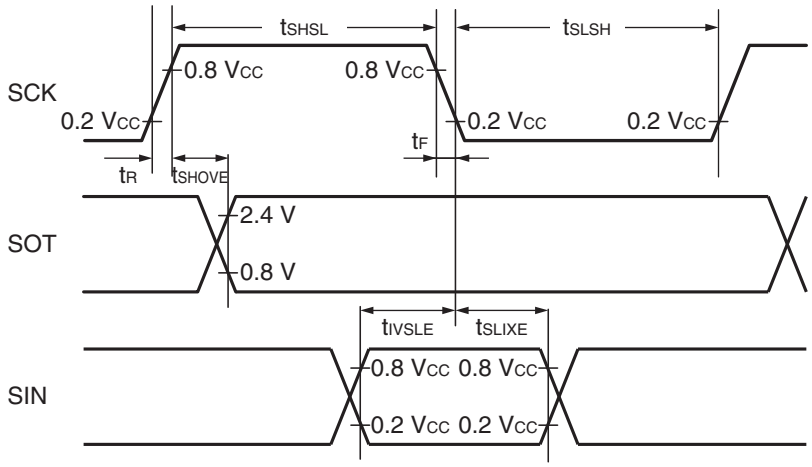
Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



Internal shift clock mode



External shift clock mode



*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

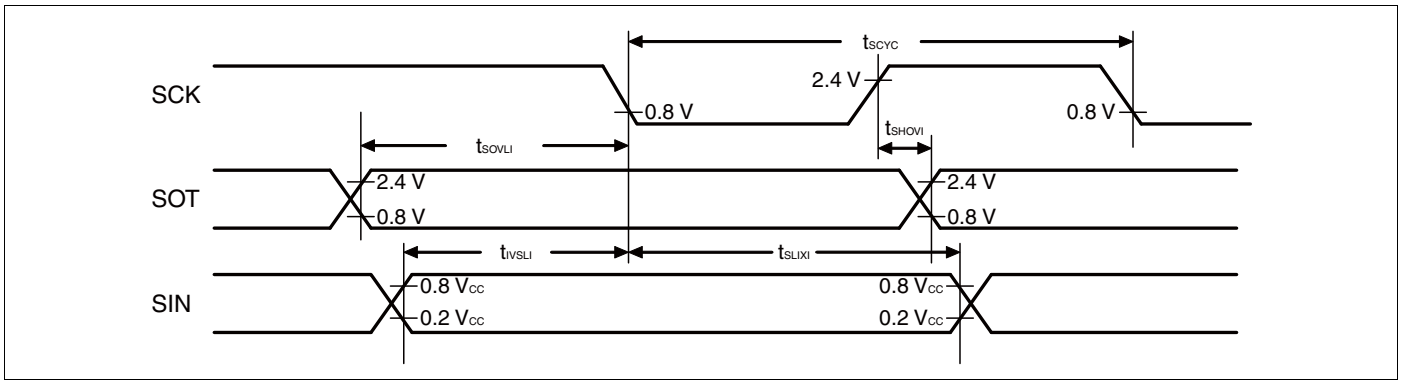
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

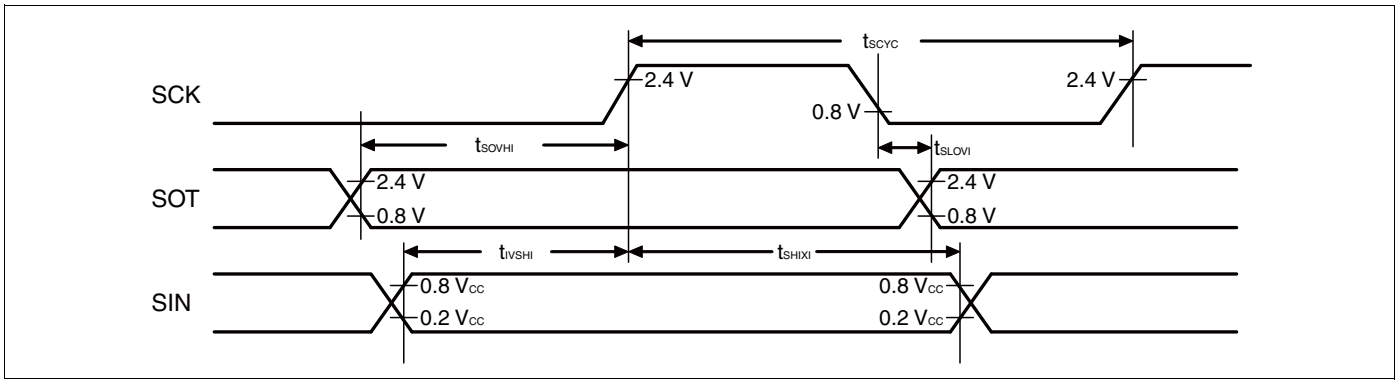
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1:There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.

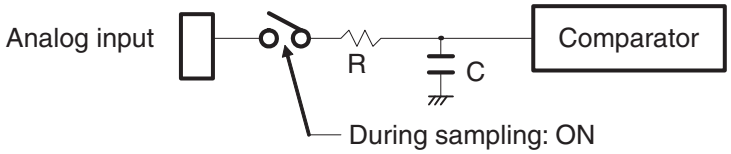


24.5.2 Notes on Using the A/D Converter

External impedance of analog input and its sampling time

The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

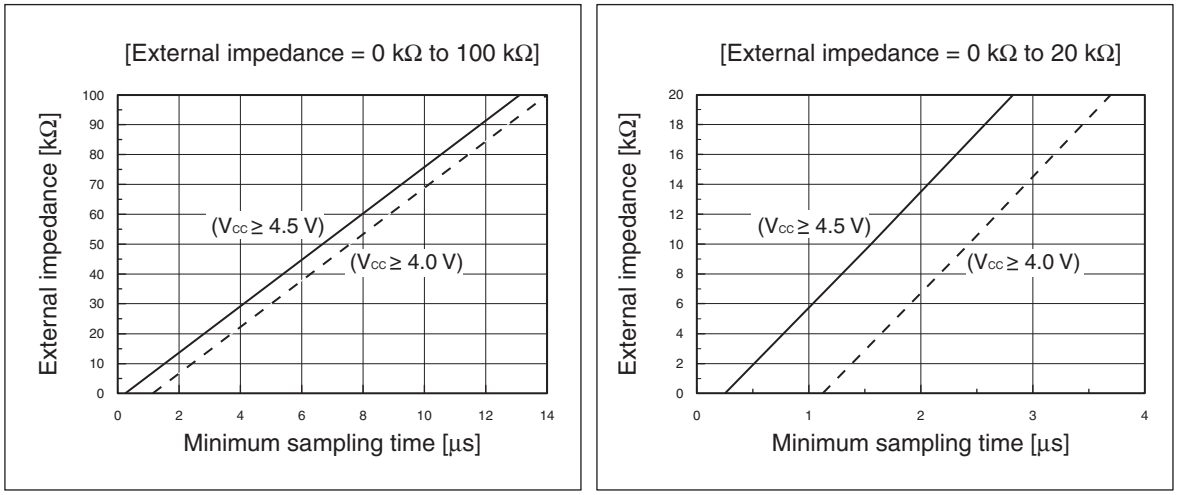
Analog input equivalent circuit



$4.5\ V \le V_{CC} \le 5.5\ V$: R ≈ 1.95 kΩ (Max), C ≈ 17 pF (Max)
$4.0\ V \le V_{CC} < 4.5\ V$: R ≈ 8.98 kΩ (Max), C ≈ 17 pF (Max)

Note: The values are reference values.

Relationship between external impedance and minimum sampling time



A/D conversion error

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

24.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of writing 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of writing 00_H prior to erasure is excluded.
Byte writing time	—	21	6100*2	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = + 85°C

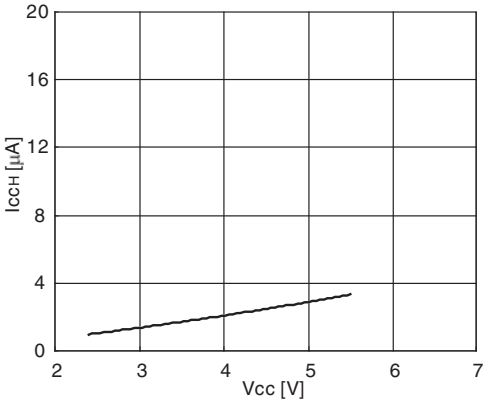
*1: T_A = + 25°C, V_{CC} = 5.0 V, 100000 cycles

*2: T_A = + 85°C, V_{CC} = 3.0 V, 100000 cycles

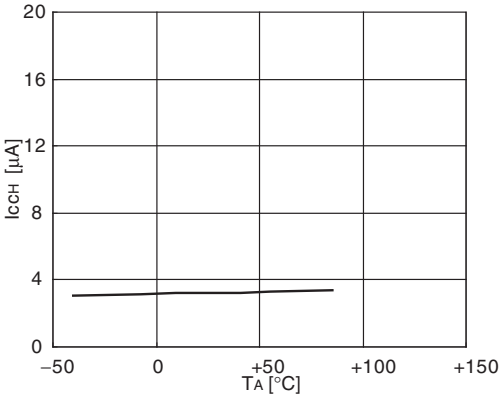
*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being + 85°C) .

(Continued)

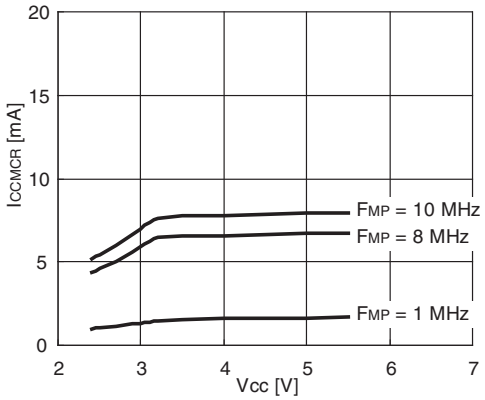
I_{CCH} - Vcc
T_A = + 25°C F_{MPL} = (stop)
Substop mode with the external clock stopping



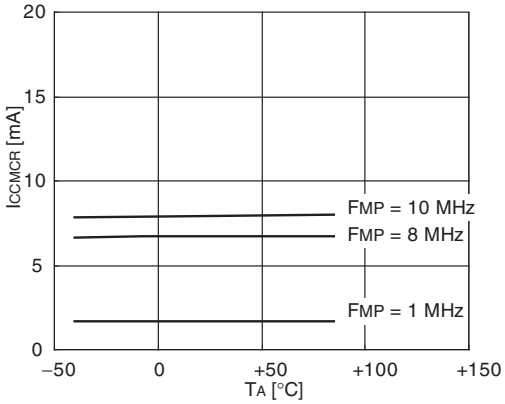
I_{CCH} - T_A
Vcc = 5.5 V F_{MPL} = (stop)
Substop mode with the external clock stopping



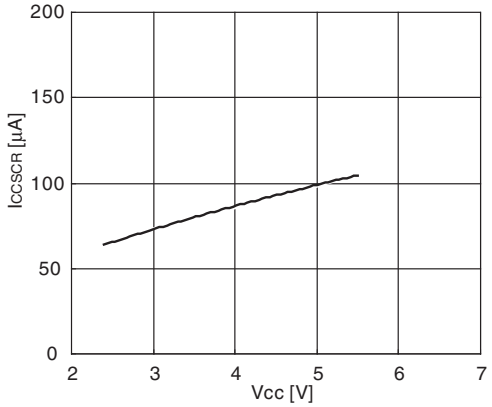
I_{CCMCR} - Vcc
T_A = + 25°C F_{MP} = 1, 8, 10 MHz (no division)
Main clock mode
with the main CR clock operating



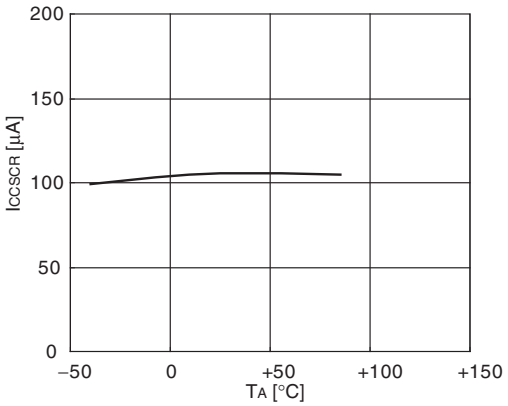
I_{CCMCR} - T_A
Vcc = 5.5 V F_{MP} = 1, 8, 10 MHz (no division)
Main clock mode
with the main CR clock operating

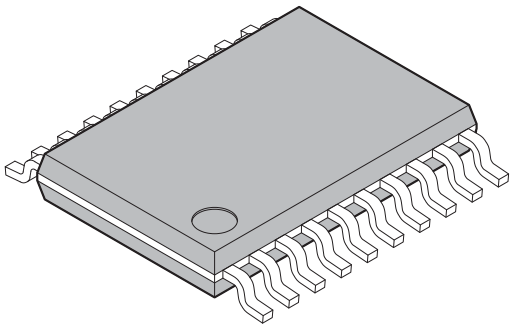


I_{CCSCR} - Vcc
T_A = + 25°C F_{MPL} = 50 kHz (divided by 2)
Subclock mode with
the sub-CR clock operating



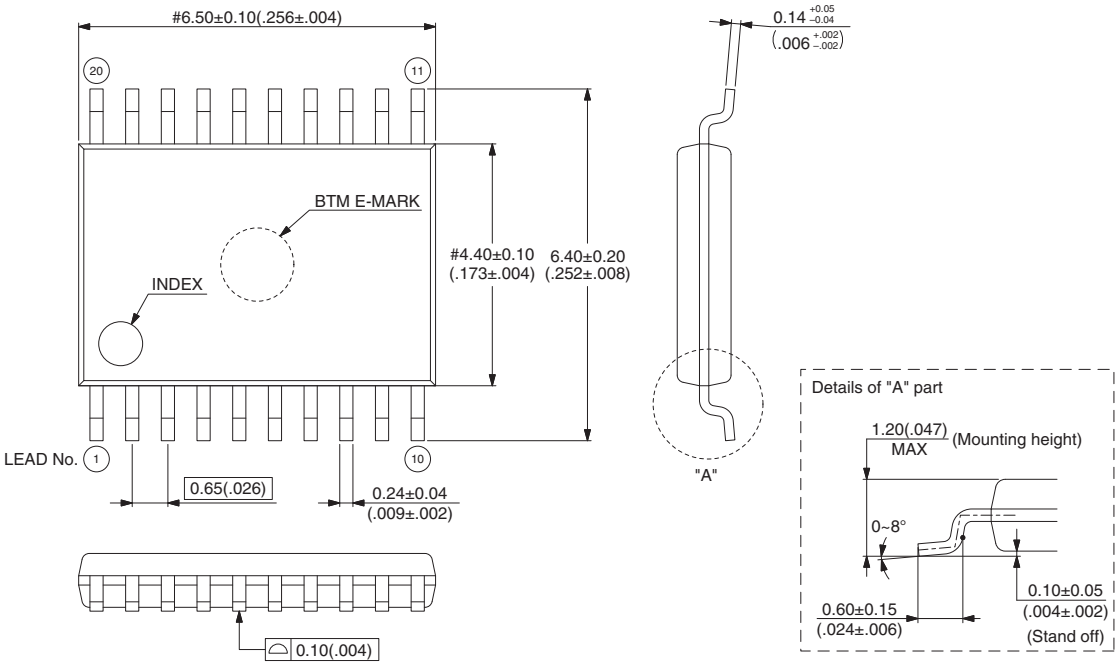
I_{CCSCR} - T_A
Vcc = 5.5 V F_{MPL} = 50 kHz (divided by 2)
Subclock mode with
the sub-CR clock operating



20-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.08 g
(FPT-20P-M10)		

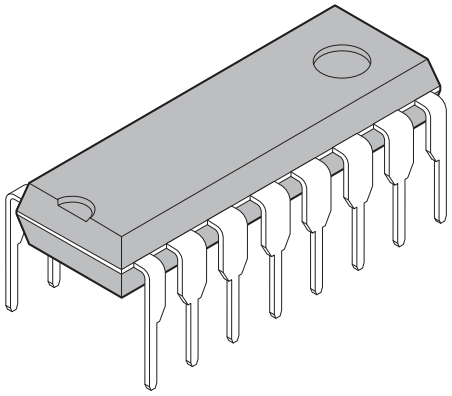
20-pin plastic TSSOP
(FPT-20P-M10)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.

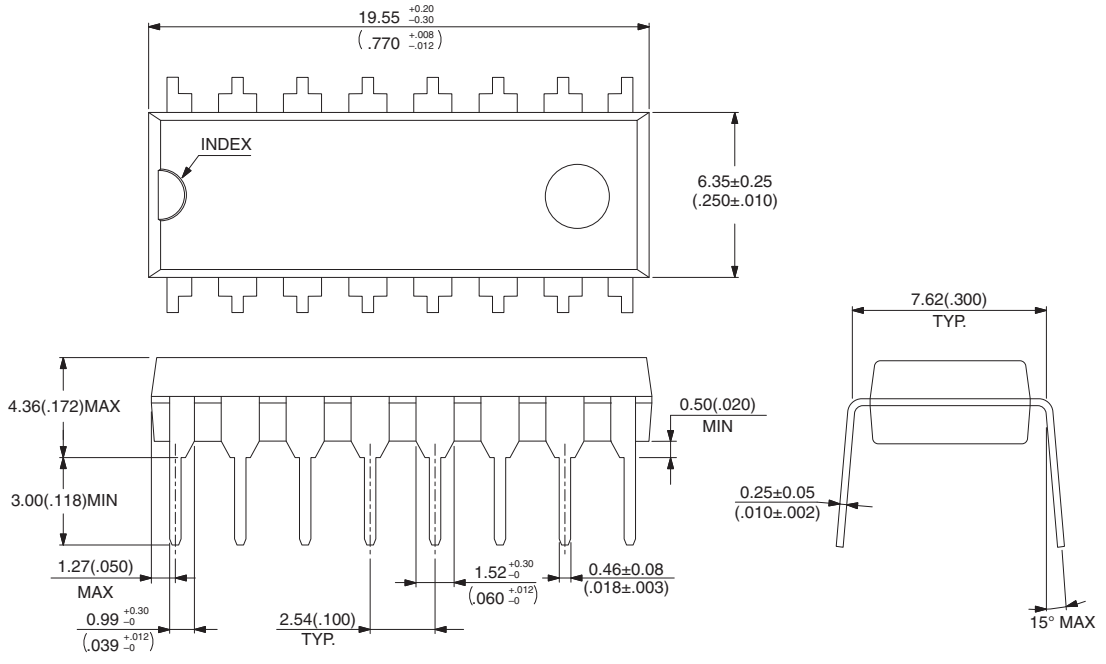


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

16-pin plastic DIP	Lead pitch	2.54 mm
	Sealing method	Plastic mold
(DIP-16P-M06)		

16-pin plastic DIP
(DIP-16P-M06)



Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

Document History

Document Title: MB95260H/270H/280H Series New 8FX 8-bit Microcontrollers Document Number: 002-07516				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	07/04/2011	Migrated to Cypress and assigned document number 002-07516. No change to document contents or format.
*A	5199019	AKIH	04/04/2016	Updated to Cypress format.