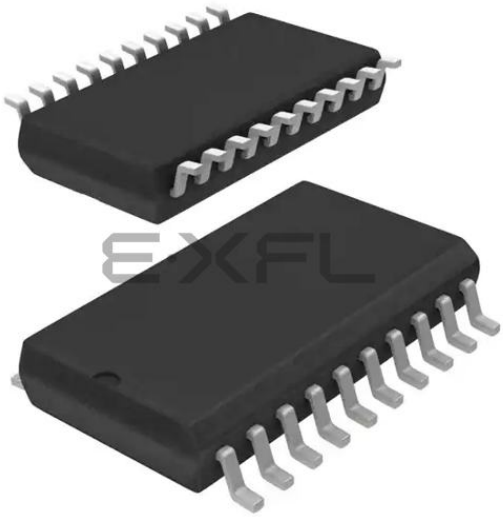

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f264kpf-g-sne2

(Continued)

Part number / Parameter	MB95F282H	MB95F283H	MB95F284H	MB95F282K	MB95F283K	MB95F284K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	LCC-32P-M19 DIP-16P-M06 FPT-16P-M06					

3. Differences among Products and Notes on Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “24. Electrical Characteristics”.

Package

For details of information on each package, see “2. Packages and Corresponding Products” and “28. Package Dimension”.

Operating voltage

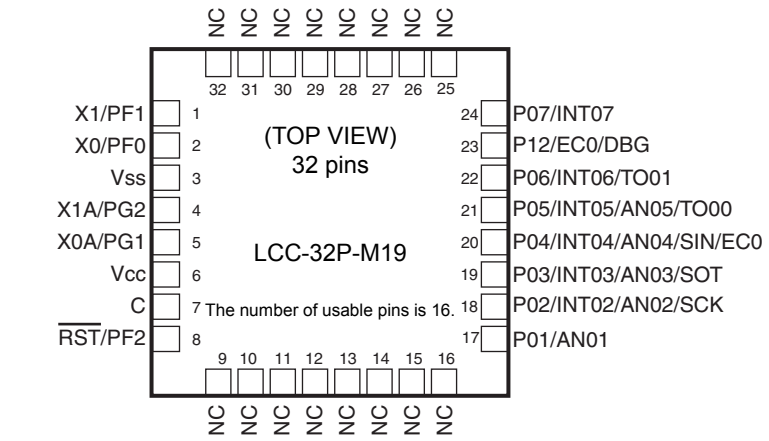
The operating voltage varies, depending on whether the on-chip debug function is used or not.

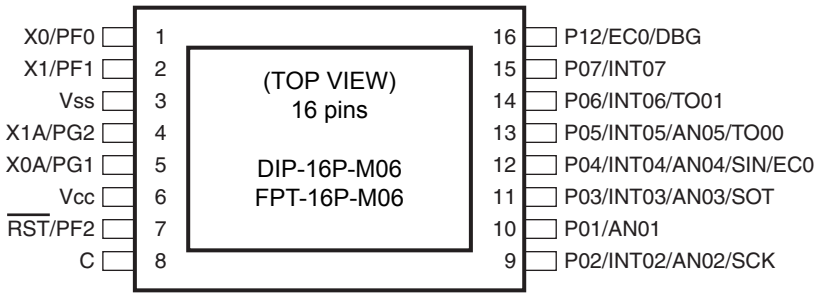
For details of the operating voltage, see “24. Electrical Characteristics”.

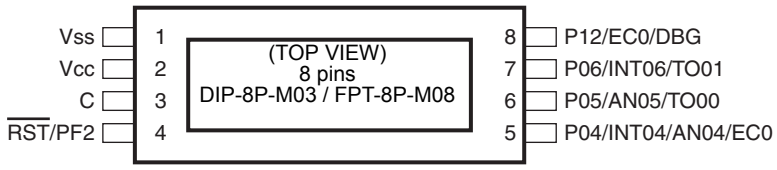
On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and 1 serial-wire be connected to an evaluation tool. In addition, if the Flash memory data has to be updated, the PF2/$\overline{RST}$ pin must also be connected to the same evaluation tool.

(Continued)


NC NC NC NC NC NC NC NC
32 31 30 29 28 27 26 25
X1/PF1 1
X0/PF0 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
C 7
RST/PF2 8
(TOP VIEW)
32 pins
LCC-32P-M19
The number of usable pins is 16.
24 P07/INT07
23 P12/EC0/DBG
22 P06/INT06/TO01
21 P05/INT05/AN05/TO00
20 P04/INT04/AN04/SIN/EC0
19 P03/INT03/AN03/SOT
18 P02/INT02/AN02/SCK
17 P01/AN01
9 10 11 12 13 14 15 16
NC NC NC NC NC NC NC NC


X0/PF0 1
X1/PF1 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
RST/PF2 7
C 8
(TOP VIEW)
16 pins
DIP-16P-M06
FPT-16P-M06
16 P12/EC0/DBG
15 P07/INT07
14 P06/INT06/TO01
13 P05/INT05/AN05/TO00
12 P04/INT04/AN04/SIN/EC0
11 P03/INT03/AN03/SOT
10 P01/AN01
9 P02/INT02/AN02/SCK


Vss 1
Vcc 2
C 3
RST/PF2 4
(TOP VIEW)
8 pins
DIP-8P-M03 / FPT-8P-M08
8 P12/EC0/DBG
7 P06/INT06/TO01
6 P05/AN05/TO00
5 P04/INT04/AN04/EC0

5. Pin Description (MB95260H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	Vss	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	Vcc	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.
9	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin
16	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

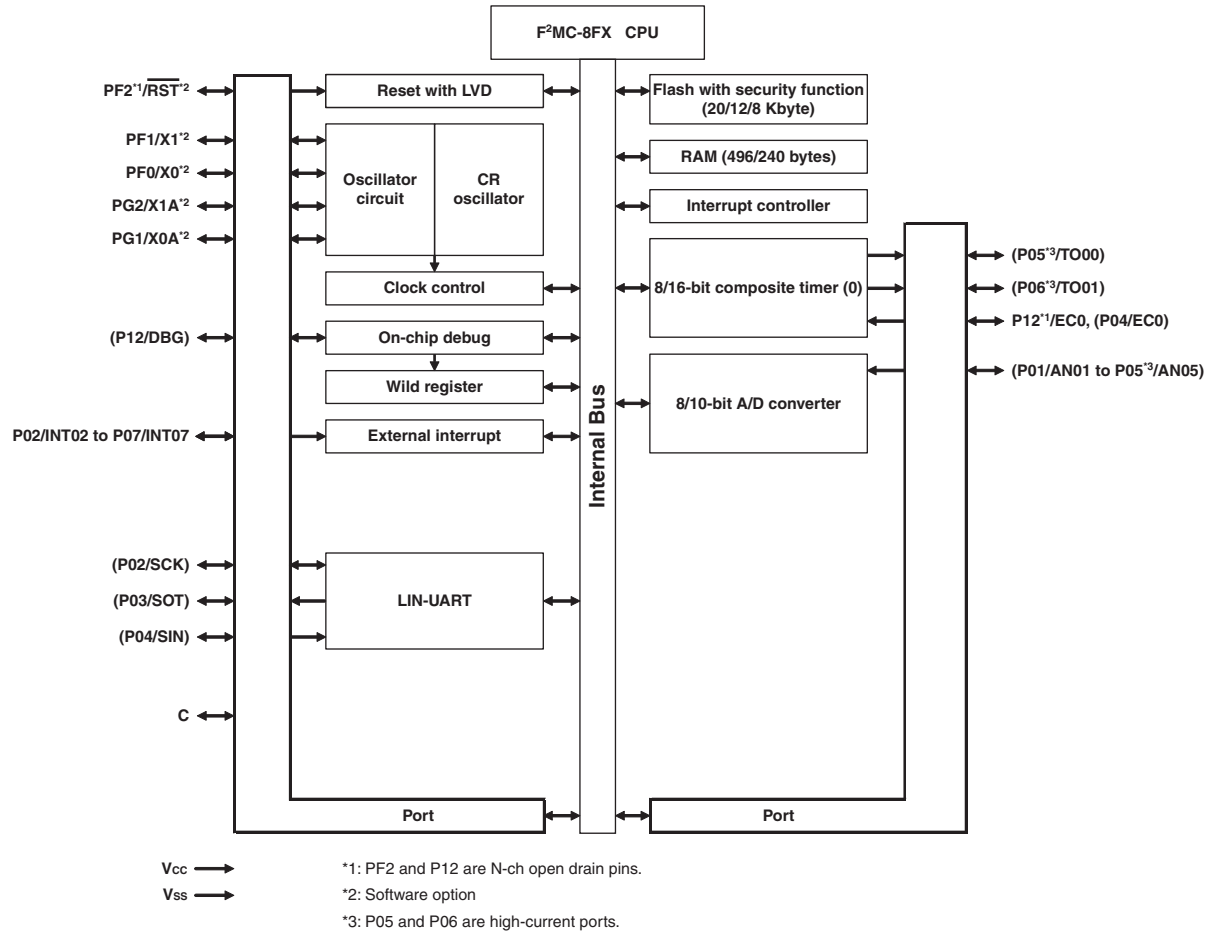
(Continued)

10. Pin Description (MB95280H Series, 16 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This pin is a dedicated reset pin in MB95F282H/F283H/F284H.
8	C	—	Capacitor connection pin
9	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
10	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
11	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
12	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

(Continued)

16. Block Diagram (MB95280H Series)



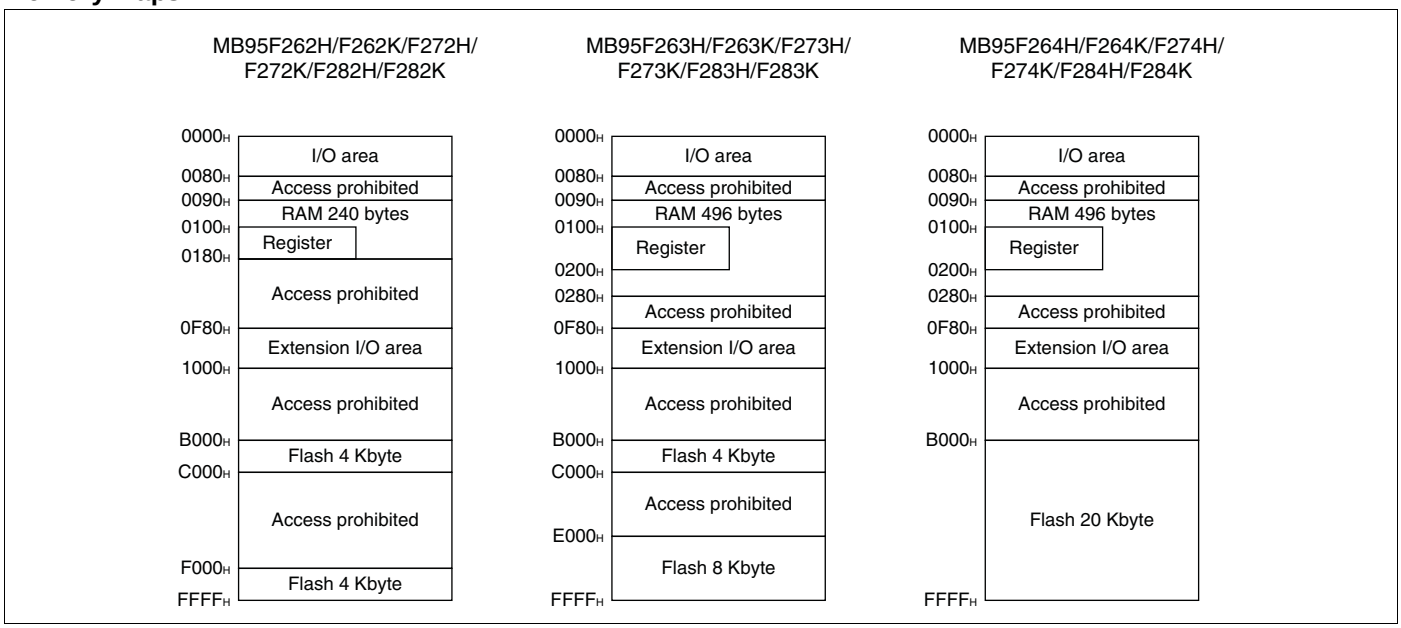
Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

17. CPU Core

Memory Space

The memory space of the MB95260H/270H/280H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95260H/270H/280H Series are shown below.

Memory Maps



Address	Register abbreviation	Register name	R/W	Initial value
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$

(Continued)

20. I/O Map (MB95280H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$000XXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	—	(Disabled)	—	—
0017_H	—	(Disabled)	—	—
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	—	(Disabled)	—	—
0039_H	—	(Disabled)	—	—
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	$0000XXXX_B$
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F80_H$	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	—	(Disabled)	—	—
$0F98_H$	—	(Disabled)	—	—
$0F99_H$	—	(Disabled)	—	—
$0F9A_H$	—	(Disabled)	—	—
$0F9B_H$	—	(Disabled)	—	—
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$

(Continued)

23. Interrupt Source Table (MB95280H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
—	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
—	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
—	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
—	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

24. Electrical Characteristics

24.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} - 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} - 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} - 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	- 2	+ 2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63*4
	I_{OL2}		15		P05, P06, P62 and P63*4
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current= operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	- 15	mA	Other than P05, P06, P62 and P63*4
	I_{OH2}		- 15		P05, P06, P62 and P63*4
"H" level average current	I_{OHAV1}	—	- 4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OHAV2}		- 8		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	- 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	- 50	mA	Total average output current= operating current ´ operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	- 40	+ 85	°C	
Storage temperature	Tstg	- 55	+ 150	°C	

(Continued)

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

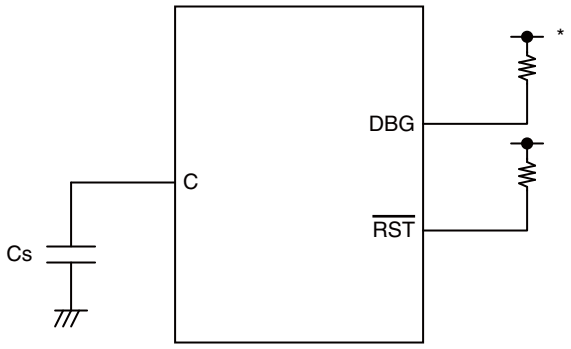
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	-40	+ 85	°C	Other than on-chip debug mode	
		+ 5	+ 35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Except during Flash memory programming and erasing
				—	33.5	39.5	mA	During Flash memory programming and erasing
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = + 25°C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = + 25°C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25°C	—	5	30	µA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode	—	8.6	—	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = + 25°C	—	110	410	µA	

(Continued)

24.4 AC Characteristics

24.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1 : open	1	—	12	MHz	When the main external clock is used
		X0, X1	*1	1	—	32.5	MHz	
	F_{CRH}	—	—	9.7	10	10.3	MHz	When the main CR clock is used*2 3.3 V ≤ Vcc ≤ 5.5 V(-40 °C ≤ T_A ≤ + 40 °C) 2.4 V ≤ Vcc < 3.3 V(0 °C ≤ T_A ≤ + 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.55	10	10.45	MHz	When the main CR clock is used*2 3.3 V ≤ Vcc ≤ 5.5 V (+ 40 °C < T_A ≤ + 85 °C)
				7.64	8	8.36	MHz	
				0.955	1	1.045	MHz	
				9.5	10	10.5	MHz	When the main CR clock is used*2 2.4 V≤ Vcc < 3.3 V (-40 °C ≤ T_A < 0 °C, + 40 °C < T_A ≤ + 85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
				9.7	10	10.3	MHz	When the main CR clock is used*3 2.4 V ≤ Vcc ≤ 5.5 V(0 °C ≤ T_A ≤ + 40 °C)
				7.76	8	8.24	MHz	
				0.97	1	1.03	MHz	
				9.5	10	10.5	MHz	When the main CR clock is used*3 2.4 V ≤ Vcc ≤ 5.5 V (-40 °C ≤ T_A < 0 °C, ＋40 °C < T_A ≤＋85 °C)
				7.6	8	8.4	MHz	
				0.95	1	1.05	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1 : open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*1	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used

(Continued)

24.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

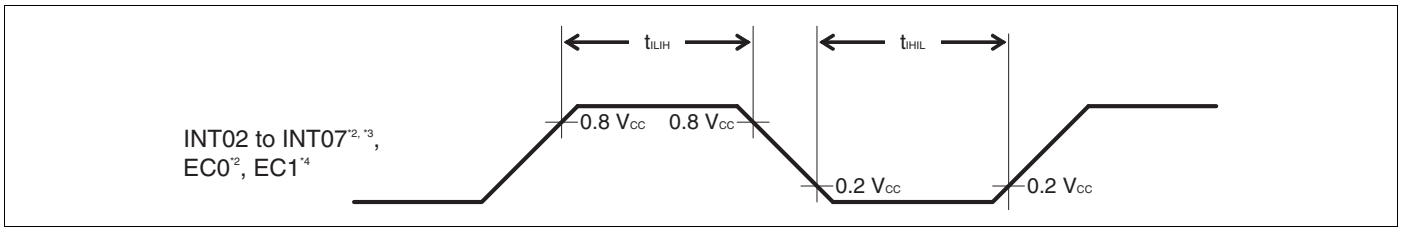
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT02 to INT07*2,*3, EC0*2, EC1*4	2 t_{MCLK}*1	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*1	—	ns

*1: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.

*2: INT04, INT06 and EC0 are available in all products.

*3: INT02, INT03, INT05 and INT07 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H /F283K/F284H/F284K.

*4: EC1 is only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 - t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑→ SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.

24.5.3 Definitions of A/D Converter Terms

Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.

Linearity error (unit: LSB)

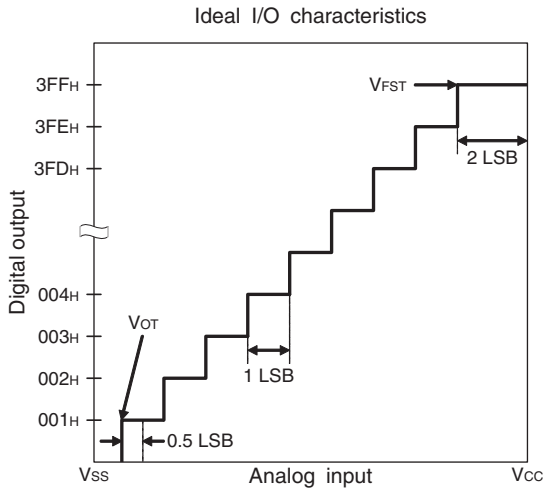
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") of the same device.

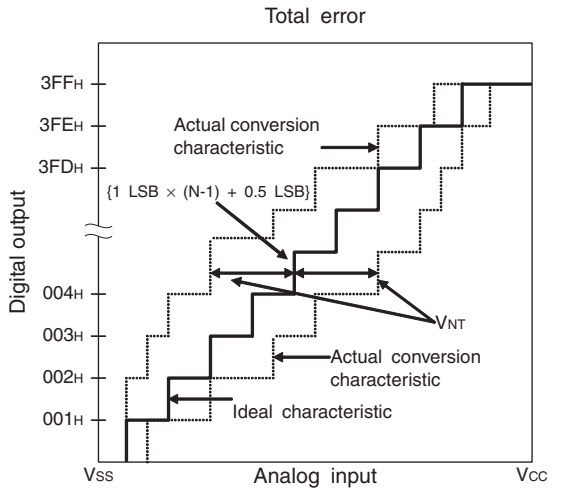
Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (V)$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

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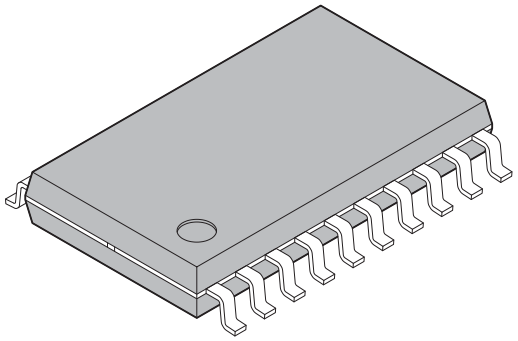
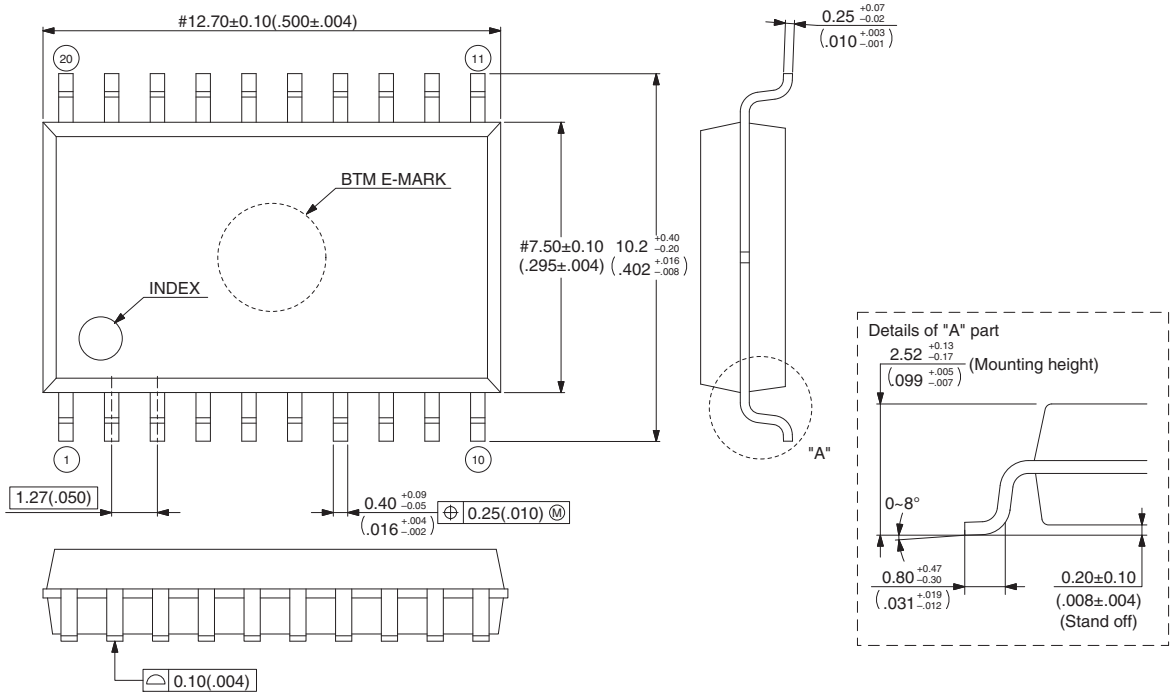
20-pin plastic SOP		
 (FPT-20P-M09)	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 12.70 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.65 mm Max

20-pin plastic SOP
(FPT-20P-M09)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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