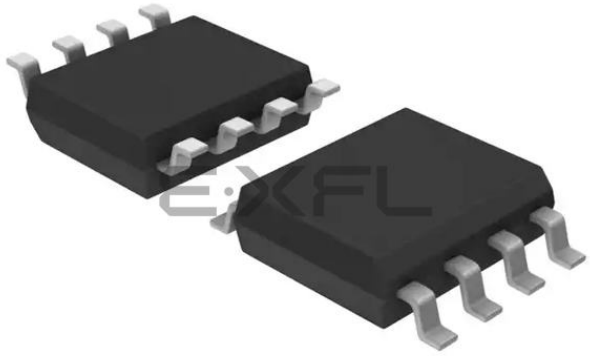

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 2x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f274kpf-g-sne2

Clock supervisor counter

■ Built-in clock supervisor counter function

Programmable port input voltage level

■ CMOS input level / hysteresis input level

Dual operation Flash memory

■ The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

■ Protects the content of the Flash memory

(Continued)

Part number / Parameter	MB95F262H	MB95F263H	MB95F264H	MB95F262K	MB95F263K	MB95F264K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	DIP-24P-M07 LCC-32P-M19 FPT-20P-M09 FPT-20P-M10					

7. Pin Description (MB95260H Series, 20 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.
9	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
10	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
11	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
12	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin
13	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
14	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
15	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

(Continued)

9. Pin Description (MB95280H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	Vss	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	Vcc	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin This is a dedicated reset pin in MB95F282H/F283H/F284H.
9	NC	—	It is an internally connected pin. Always leave it unconnected.
10	NC	—	It is an internally connected pin. Always leave it unconnected.
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	NC	—	It is an internally connected pin. Always leave it unconnected.
16	NC	—	It is an internally connected pin. Always leave it unconnected.
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
20	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F81_H$	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (Upper)	R/W	$1XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (Lower)	R/W	$000XXXXX_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H to $006B_H$	—	(Disabled)	—	—
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register upper	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register lower	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	$0000XXXX_B$
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—

(Continued)

22. Interrupt Source Table (MB95270H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
—	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
—	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
—	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
—					
—	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
—	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
—	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
—	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
—	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
—	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
—	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

24. Electrical Characteristics

24.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} - 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} - 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} - 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	- 2	+ 2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63*4
	I_{OL2}		15		P05, P06, P62 and P63*4
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current= operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	- 15	mA	Other than P05, P06, P62 and P63*4
	I_{OH2}		- 15		P05, P06, P62 and P63*4
"H" level average current	I_{OHAV1}	—	- 4	mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
	I_{OHAV2}		- 8		P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	- 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	- 50	mA	Total average output current= operating current ´ operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	- 40	+ 85	°C	
Storage temperature	Tstg	- 55	+ 150	°C	

(Continued)

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

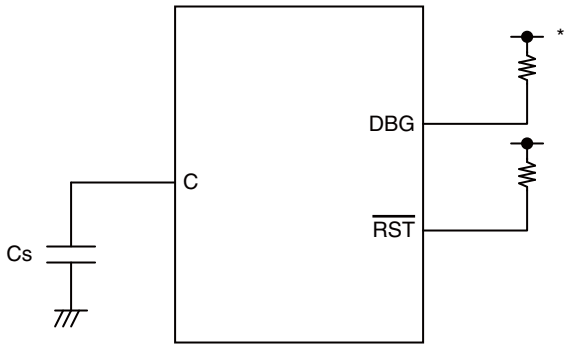
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	-40	+ 85	°C	Other than on-chip debug mode	
		+ 5	+ 35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*4	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Except during Flash memory programming and erasing
				—	33.5	39.5	mA	During Flash memory programming and erasing
				—	15	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = + 25°C	—	65	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = + 25°C	—	10	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25°C	—	5	30	µA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode	—	8.6	—	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = + 25°C	—	110	410	µA	

(Continued)

24.4.2 Source Clock / Machine Clock

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			100	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 10 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	10	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			100	—	16000	ns	When the main CR clock is used Min: F_{SP} = 10 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	10	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC : DIV1 and DIV0) . This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC : DIV1 and DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

24.4.3 External Reset

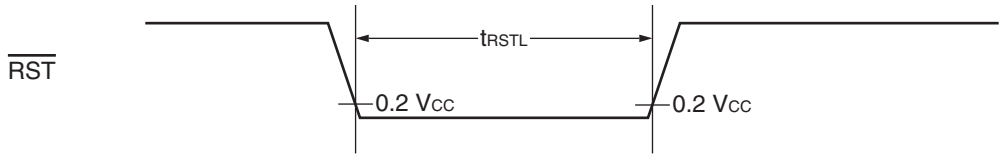
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, sub-sleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

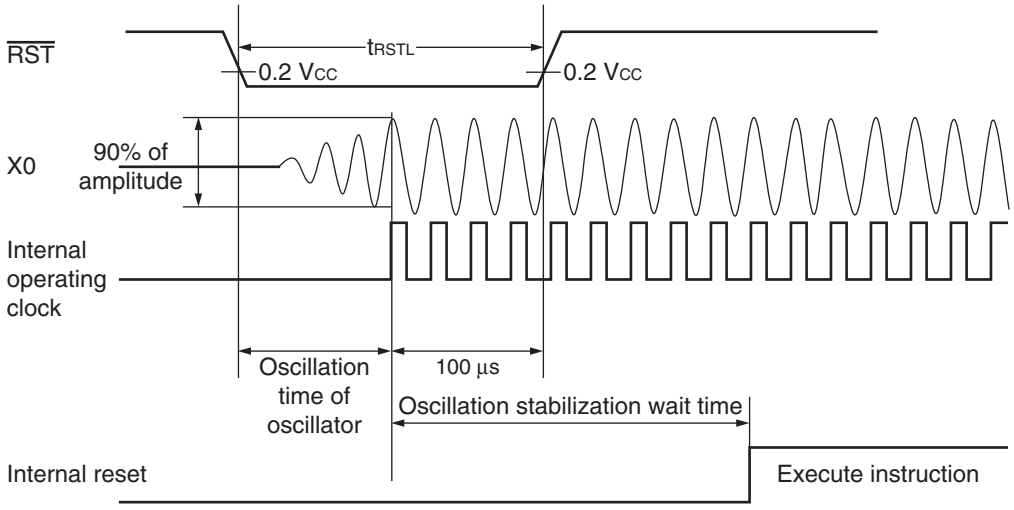
*1 : See "24.4.2. Source Clock / Machine Clock" for t_{MCLK}.

*2 : The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

In normal operation



In stop mode, subclock mode,



*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

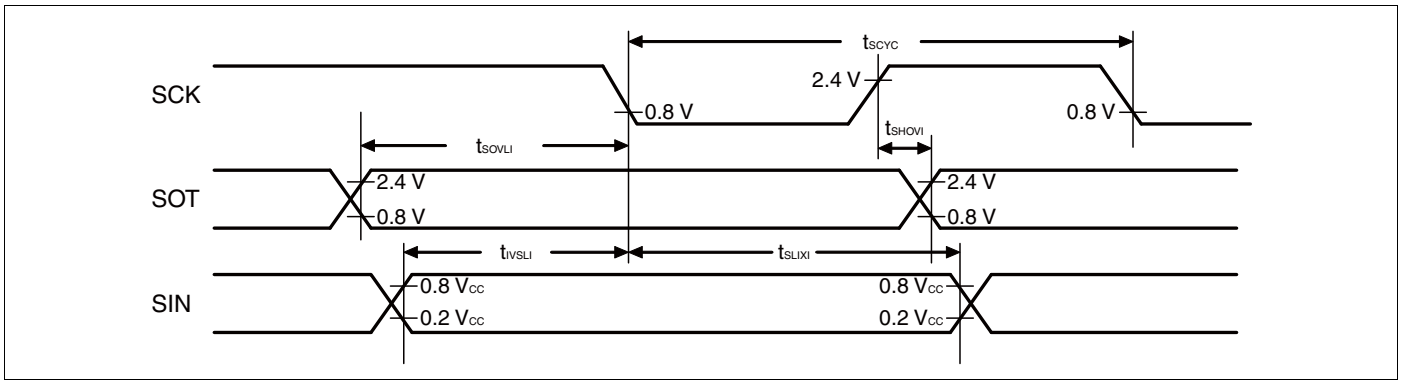
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		- 95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

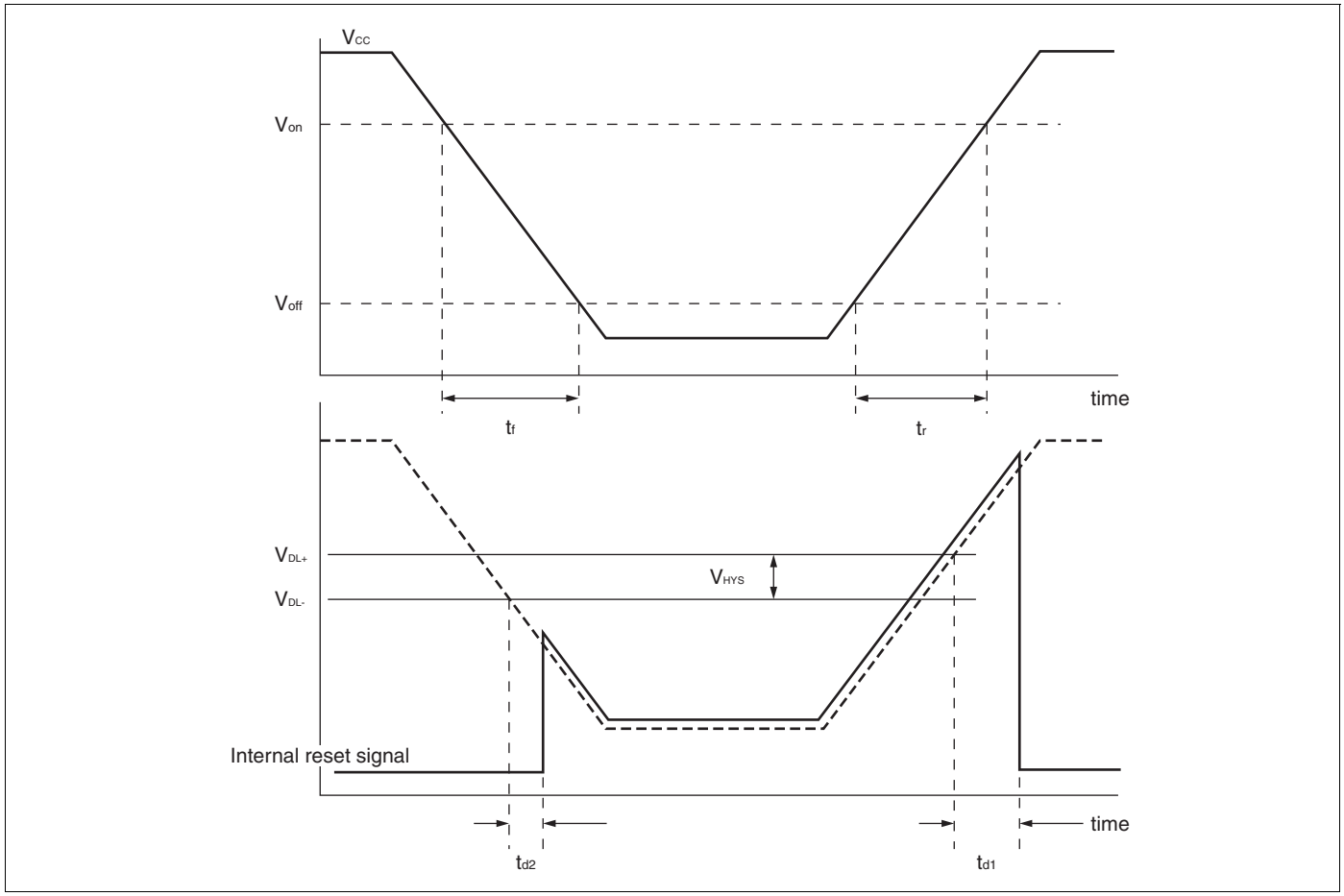
*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK}.



24.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	



24.5 A/D Converter

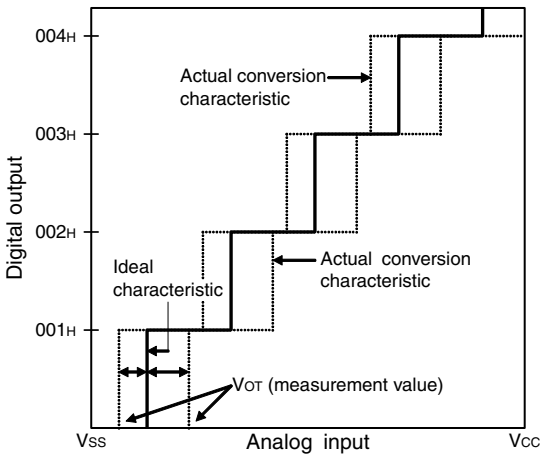
24.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to + 85°C)

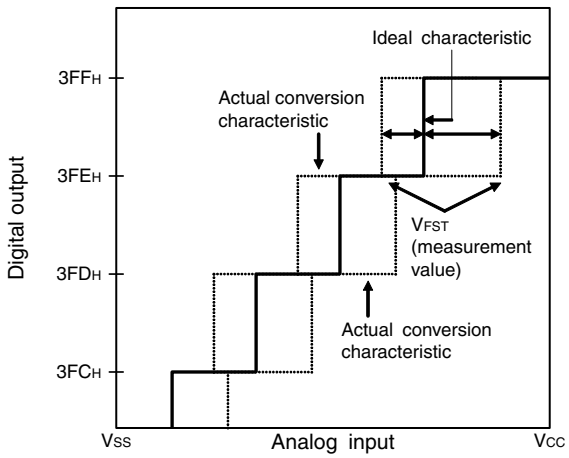
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		- 3	—	+ 3	LSB	
Linearity error		- 2.5	—	+ 2.5	LSB	
Differential linear error		- 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} - 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} - 4.5 LSB	V_{CC} - 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	- 0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(Continued)

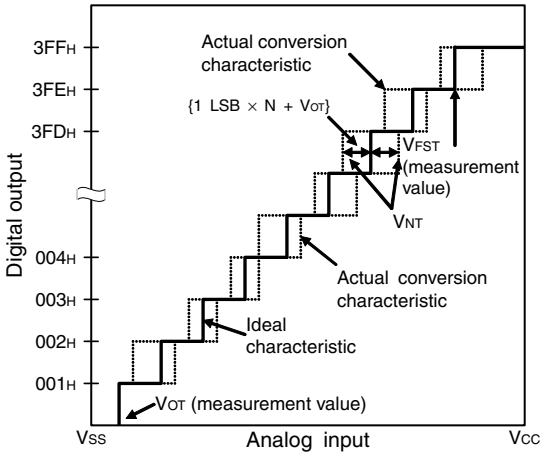
Zero transition error



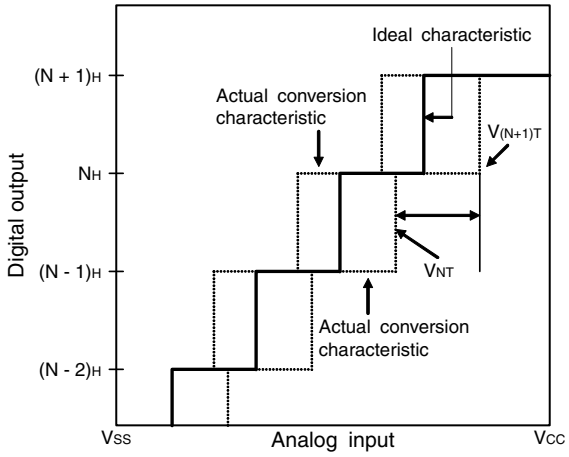
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

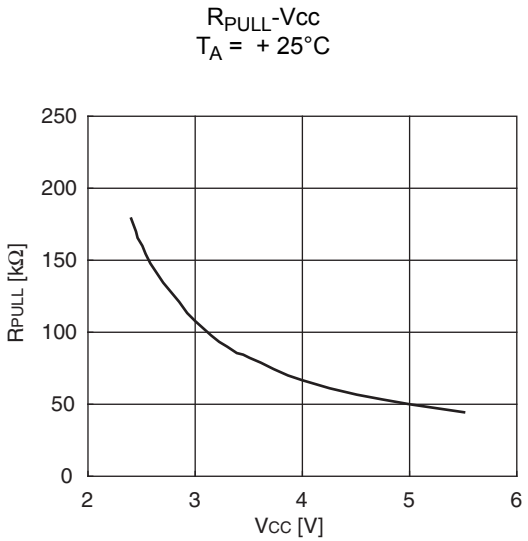
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

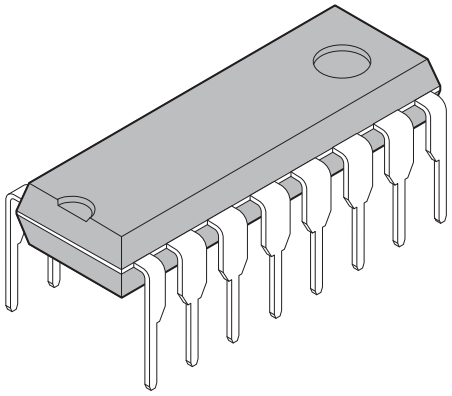
Pull-up



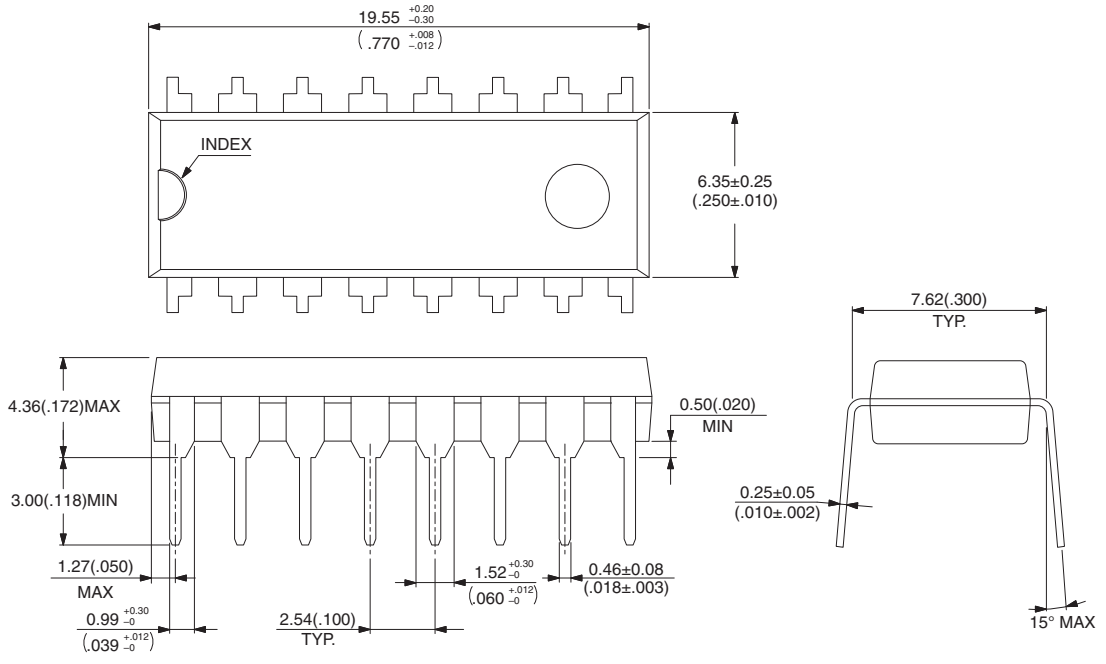
27. Ordering Information

Part Number	Package
MB95F262HWQN-G-SNE1 MB95F262HWQN-G-SNERE1 MB95F262KWQN-G-SNE1 MB95F262KWQN-G-SNERE1 MB95F263HWQN-G-SNE1 MB95F263HWQN-G-SNERE1 MB95F263KWQN-G-SNE1 MB95F263KWQN-G-SNERE1 MB95F264HWQN-G-SNE1 MB95F264HWQN-G-SNERE1 MB95F264KWQN-G-SNE1 MB95F264KWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F262HP-G-SH-SNE2 MB95F262KP-G-SH-SNE2 MB95F263HP-G-SH-SNE2 MB95F263KP-G-SH-SNE2 MB95F264HP-G-SH-SNE2 MB95F264KP-G-SH-SNE2	24-pin plastic SDIP (DIP-24P-M07)
MB95F262HPF-G-SNE2 MB95F262KPF-G-SNE2 MB95F263HPF-G-SNE2 MB95F263KPF-G-SNE2 MB95F264HPF-G-SNE2 MB95F264KPF-G-SNE2	20-pin plastic SOP (FPT-20P-M09)
MB95F262HPFT-G-SNE2 MB95F262KPFT-G-SNE2 MB95F263HPFT-G-SNE2 MB95F263KPFT-G-SNE2 MB95F264HPFT-G-SNE2 MB95F264KPFT-G-SNE2	20-pin plastic TSSOP (FPT-20P-M10)
MB95F282HWQN-G-SNE1 MB95F282HWQN-G-SNERE1 MB95F282KWQN-G-SNE1 MB95F282KWQN-G-SNERE1 MB95F283HWQN-G-SNE1 MB95F283HWQN-G-SNERE1 MB95F283KWQN-G-SNE1 MB95F283KWQN-G-SNERE1 MB95F284HWQN-G-SNE1 MB95F284HWQN-G-SNERE1 MB95F284KWQN-G-SNE1 MB95F284KWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F282HPH-G-SNE2 MB95F282KPH-G-SNE2 MB95F283HPH-G-SNE2 MB95F283KPH-G-SNE2 MB95F284HPH-G-SNE2 MB95F284KPH-G-SNE2	16-pin plastic DIP (DIP-16P-M06)

(Continued)

16-pin plastic DIP	Lead pitch	2.54 mm
	Sealing method	Plastic mold
(DIP-16P-M06)		

16-pin plastic DIP
(DIP-16P-M06)



Dimensions in mm (inches).
Note: The values in parentheses are reference values

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