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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F ² MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	5
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 2x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f274kpf-g-sne2





Clock supervisor counter

■ Built-in clock supervisor counter function

Programmable port input voltage level

■ CMOS input level / hysteresis input level

Dual operation Flash memory

■ The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

■ Protects the content of the Flash memory

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(Continued)							
Part number Parameter	MB95F262H	MB95F263H	MB95F264H	MB95F262K	MB95F263K	MB95F264K	
Watch prescaler	Eight different time	e intervals can be s	selected.				
IFIGER MAMORY	mands. It has a flag indi Number of prog Data retention ti	cating the completi ram/erase cycles: ' me: 20 years	ion of the operatior	n of Embedded Alg	se/erase-suspend/e	rase-resume com-	
Standby mode	Sleep mode, stop	mode, watch mode	e, time-base timer i	mode			
Package	DIP-24P-M07 LCC-32P-M19 FPT-20P-M09 FPT-20P-M10						



7. Pin Description (MB95260H Series, 20 pins)

Pin no.	Pin name	I/O circuit type*	Function				
1	PF0	В	General-purpose I/O port				
	X0	Б	Main clock input oscillation pin				
2 -	PF1	В	General-purpose I/O port				
2	X1	Б	Main clock I/O oscillation pin				
3	V _{SS}	_	Power supply pin (GND)				
4	PG2	С	General-purpose I/O port				
4	X1A		Subclock I/O oscillation pin				
5 -	PG1	С	General-purpose I/O port				
5	X0A		Subclock input oscillation pin				
6	V _{CC}	_	Power supply pin				
7	С	_	Capacitor connection pin				
	PF2		General-purpose I/O port				
8	RST	A	Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H.				
9	P62	D	General-purpose I/O port High-current pin				
	TO10		8/16-bit composite timer ch. 1 output pin				
10	P63	D	General-purpose I/O port High-current pin				
	TO11		8/16-bit composite timer ch. 1 output pin				
44	P64	5	General-purpose I/O port				
11 -	EC1	D	8/16-bit composite timer ch. 1 clock input pin				
10	P00	E	General-purpose I/O port				
12	AN00		A/D converter analog input pin				
13	P01	E	General-purpose I/O port				
13	AN01		A/D converter analog input pin				
	P02		General-purpose I/O port				
14	INT02		External interrupt input pin				
14	14 AN02		A/D converter analog input pin				
	SCK		LIN-UART clock I/O pin				
	P03		General-purpose I/O port				
15	INT03	E E	External interrupt input pin				
	AN03		A/D converter analog input pin				
	SOT		LIN-UART data output pin				

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9. Pin Description (MB95280H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function					
1	PF1	В	General-purpose I/O port					
'	X1		Main clock I/O oscillation pin					
2	PF0	В	General-purpose I/O port					
	X0		Main clock input oscillation pin					
3	Vss	_	Power supply pin (GND)					
4	PG2	С	General-purpose I/O port					
4	X1A		Subclock I/O oscillation pin					
5	PG1	С	General-purpose I/O port					
3	X0A		Subclock input oscillation pin					
6	Vcc	_	Power supply pin					
7	С	_	Capacitor connection pin					
	PF2		General-purpose I/O port					
8	RST	A	Reset pin This is a dedicated reset pin in MB95F282H/F283H/F284H.					
9	NC	_	It is an internally connected pin. Always leave it unconnected.					
10	NC	_	It is an internally connected pin. Always leave it unconnected.					
11	NC	_	It is an internally connected pin. Always leave it unconnected.					
12	NC	_	It is an internally connected pin. Always leave it unconnected.					
13	NC	_	It is an internally connected pin. Always leave it unconnected.					
14	NC	_	It is an internally connected pin. Always leave it unconnected.					
15	NC	_	It is an internally connected pin. Always leave it unconnected.					
16	NC	_	It is an internally connected pin. Always leave it unconnected.					
17	P01	E	General-purpose I/O port					
.,	AN01	_	A/D converter analog input pin					
	P02		General-purpose I/O port					
18	INT02	E	External interrupt input pin					
	AN02	_	A/D converter analog input pin					
	SCK		LIN-UART clock I/O pin					
	P03		General-purpose I/O port					
19	INT03	E E	External interrupt input pin					
	AN03		A/D converter analog input pin					
	SOT		LIN-UART data output pin					
	P04		General-purpose I/O port					
	INT04		External interrupt input pin					
20	AN04	F	A/D converter analog input pin					
	SIN		LIN-UART data input pin					
	EC0		8/16-bit composite timer ch. 0 clock input pin					

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Address	Register abbreviation	Register name	R/W	Initial value
0F81 _H	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000 _B
0F82 _H	WRDR0	Wild register data setting register ch. 0	R/W	00000000 _B
0F83 _H	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000 _B
0F84 _H	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000 _B
0F85 _H	WRDR1	Wild register data setting register ch. 1	R/W	00000000 _B
0F86 _H	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000 _B
0F87 _H	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000 _B
0F88 _H	WRDR2	Wild register data setting register ch. 2	R/W	00000000 _B
0F89 _H to 0F91 _H	_	(Disabled)	_	_
0F92 _H	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000 _B
0F93 _H	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000 _B
0F94 _H	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000 _B
0F95 _H	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000 _B
0F96 _H	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000 _B
0F97 _H	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000 _B
0F98 _H	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000 _B
0F99 _H	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000 _B
0F9A _H	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000 _B
0F9B _H	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000 _B
0F9C _H to 0FBB _H	_	(Disabled)	_	_
0FBC _H	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 _B
0FBD _H	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 _B
0FBE _H to 0FC2 _H	_	(Disabled)	_	_
0FC3 _H	AIDRL	A/D input disable register (Lower)	R/W	00000000 _B
0FC4 _H to 0FE3 _H	_	(Disabled)		_
0FE4 _H	CRTH	Main CR clock trimming register (Upper)	R/W	1XXXXXXX _B
0FE5 _H	CRTL	Main CR clock trimming register (Lower)	R/W	000XXXXX _B



Address	Register abbreviation	Register name	R/W	Initial value
004A _H	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000 _B
004B _H	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000 _B
004C _H to 004F _H	_	(Disabled)	_	_
0050 _H	SCR	LIN-UART serial control register	R/W	00000000 _B
0051 _H	SMR	LIN-UART serial mode register	R/W	00000000 _B
0052 _H	SSR	LIN-UART serial status register	R/W	00001000 _B
0053 _H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000 _B
0054 _H	ESCR	LIN-UART extended status control register	R/W	00000100 _B
0055 _H	ECCR	LIN-UART extended communication control register	R/W	000000XX _B
0056 _H to 006B _H	_	(Disabled)	_	_
006C _H	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 _B
006D _H	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 _B
006E _H	ADDH	8/10-bit A/D converter data register upper	R/W	00000000 _B
006F _H	ADDL	8/10-bit A/D converter data register lower	R/W	00000000 _B
0070 _H	_	(Disabled)		_
0071 _H	FSR2	Flash memory status register 2	R/W	00000000 _B
0072 _H	FSR	Flash memory status register	R/W	000X0000 _B
0073 _H	SWRE0	Flash memory sector write control register 0	R/W	00000000 _B
0074 _H	FSR3	Flash memory status register 3	R	0000XXXX _B
0075 _H	_	(Disabled)	_	_
0076 _H	WREN	Wild register address compare enable register	R/W	00000000 _B
0077 _H	WROR	Wild register data test setting register	R/W	00000000 _B
0078 _H	_	Mirror of register bank pointer (RP) and direct bank pointer (DP)	_	_
0079 _H	ILR0	Interrupt level setting register 0		11111111 _B
007A _H	ILR1	Interrupt level setting register 1		11111111 _B
007B _H	ILR2	Interrupt level setting register 2		11111111 _B
007C _H	ILR3	Interrupt level setting register 3	R/W	11111111 _B
007D _H	ILR4	Interrupt level setting register 4	R/W	11111111 _B
007E _H	ILR5	Interrupt level setting register 5	R/W	11111111 _B
007F _H	_	(Disabled)		_



22. Interrupt Source Table (MB95270H Series)

		Vector tak	ole address	D ''	Priority order of
Interrupt source	Interrupt request number	Upper	Lower	Bit name of interrupt level setting register	interrupt sources of the same level (occurring simultaneously)
External interrupt ch. 4	IRQ00	FFFA _H	FFFB _H	L00 [1:0]	High
_	IRQ01	FFF8 _H	FFF9 _H	L01 [1:0]]g
_	IRQ02	FFF6 _H	FFF7 _H	L02 [1:0]	↑
External interrupt ch. 6	111002	TTTOH	'''''H	L02 [1.0]	
_	IRQ03	FFF4 _H	FFF5 _H	L03 [1:0]	
-			оп	200 [0]	<u> </u>
_	IRQ04	FFF2 _H	FFF3 _H	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ05	FFF0 _H	FFF1 _H	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ06	FFEE _H	FFEF _H	L06 [1:0]	
_	IRQ07	FFEC _H	FFED _H	L07 [1:0]	
_	IRQ08	FFEA _H	FFEB _H	L08 [1:0]	
_	IRQ09	FFE8 _H	FFE9 _H	L09 [1:0]	
_	IRQ10	FFE6 _H	FFE7 _H	L10 [1:0]	
_	IRQ11	FFE4 _H	FFE5 _H	L11 [1:0]	
_	IRQ12	FFE2 _H	FFE3 _H	L12 [1:0]	_
_	IRQ13	FFE0 _H	FFE1 _H	L13 [1:0]	
_	IRQ14	FFDE _H	FFDF _H	L14 [1:0]	
_	IRQ15	FFDC _H	FFDD _H	L15 [1:0]	
_	IRQ16	FFDA _H	FFDB _H	L16 [1:0]	
_	IRQ17	FFD8 _H	FFD9 _H	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 _H	FFD7 _H	L18 [1:0]	
Time-base timer	IRQ19	FFD4 _H	FFD5 _H	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 _H	FFD3 _H	L20 [1:0]	
_	IRQ21	FFD0 _H	FFD1 _H	L21 [1:0]	1 ↓
_	IRQ22	FFCE _H	FFCF _H	L22 [1:0]	▼
Flash memory	IRQ23	FFCC _H	FFCD _H	L23 [1:0]	Low

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24. Electrical Characteristics

24.1 Absolute Maximum Ratings

Davamatar	Cumbal	Rating		11	Domosko	
Parameter	Symbol	Min	Max	Unit	Remarks	
Power supply voltage*1	V _{CC}	V _{SS} - 0.3	V _{SS} + 6	V		
Input voltage*1	VI	V _{SS} - 0.3	V _{SS} + 6	V	*2	
Output voltage*1	Vo	V _{SS} - 0.3	V _{SS} + 6	V	*2	
Maximum clamp current	I _{CLAMP}	- 2	+ 2	mA	Applicable to specific pins*3	
Total maximum clamp current	ΣΙΙ _{CLAMP} Ι	_	20	mA	Applicable to specific pins*3	
"L" level maximum output	I _{OL1}		15	mA	Other than P05, P06, P62 and P63*4	
current	I _{OL2}	_	15	IIIA	P05, P06, P62 and P63 ^{*4}	
"L" level average current	I _{OLAV1}		4	- mA	Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)	
L level average current	I _{OLAV2}	_	12	IIIA	P05, P06, P62 and P63 ^{*4} Average output current= operating current × operating ratio (1 pin)	
"L" level total maximum output current	Σl _{OL}	_	100	mA		
"L" level total average output current	ΣI _{OLAV}	_	50	mA	Total average output current= operating current × operating ratio (Total number of pins)	
"H" level maximum output	I _{OH1}		- 15		Other than P05, P06, P62 and P63*4	
current	I _{OH2}	-	- 15	mA	P05, P06, P62 and P63*4	
"Ll" lovel everage current	I _{OHAV1}		- 4		Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin)	
"H" level average current	I _{OHAV2}	_	- 8	- mA	P05, P06, P62 and P63 ^{*4} Average output current= operating current × operating ratio (1 pin)	
"H" level total maximum output current	Σl _{OH}	_	- 100	mA		
"H" level total average output current	ΣΙ _{ΟΗΑV}	_	- 50	mA	Total average output current= operating current ´ operating ratio (Total number of pins)	
Power consumption	Pd	_	320	mW		
Operating temperature	T _A	- 40	+ 85	°C		
Storage temperature	Tstg	- 55	+ 150	°C		

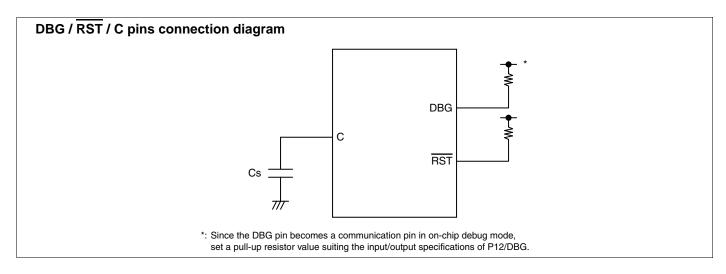


24.2 Recommended Operating Conditions

 $(V_{SS} = 0.0 V)$

Parameter	Symbol	Va	Value		Remarks			
raiametei	Syllibol	Min	Max	Unit	One Remarks			
		2.4*1*2	5.5* ¹		In normal operation	Other than on-chip debug mode		
Power supply	\ \/	2.3	5.5	V	Hold condition in stop mode	- Other than on-chip debug mode		
voltage	V _{CC}	2.9	5.5	ľ	In normal operation	On ohin dahug mada		
		2.3	5.5		Hold condition in stop mode	On-chip debug mode		
Smoothing capacitor	C _S	0.022	1	μF	*3			
Operating	т	-40	+ 85	°C	Other than on-chip debug mode			
temperature	T _A	+ 5	+ 35		On-chip debug mode			

- *1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.
- *2: The value is 2.88 V when the low-voltage detection reset is used.
- st3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V $_{
 m CC}$ pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.

Users considering application outside the listed conditions are advised to contact their representatives beforehand.



 $(V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = 0.0 \text{ V}, T_A = -40^{\circ}\text{C to } + 85^{\circ}\text{C})$

Donomotor	Cumbal	Pin name	Condition		Value		Unit	Damarka
Parameter	Symbol	riii iiaille	Condition	Min	Тур	Max	Unit	Remarks
			V _{CC} = 5.5 V F _{CH} = 32 MHz	_	13	17	mA	Except during Flash memory programming and erasing
	I _{CC}		F _{MP} = 16 MHz Main clock mode (divided by 2)	_	33.5	39.5	mA	During Flash memory programming and erasing
				_	15	21	mA	At A/D conversion
	Iccs		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	_	5.5	9	mA	
Power supply current*4	I _{CCL}	V _{CC} (External clock operation)	V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	_	65	153	μА	
	Iccls		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	_	10	84	μА	
	Ісст		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	_	5	30	μΑ	
	I _{CCMCR}	V	V_{CC} = 5.5 V F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode		8.6	_	mA	
	Iccscr	V _{CC}	V _{CC} = 5.5 V Sub-CR clock mode (divided by 2) T _A = +25°C	_	110	410	μА	



24.4.2 Source Clock / Machine Clock

 $(V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = 0.0 \text{ V}, T_A = -40^{\circ}\text{C to } + 85^{\circ}\text{C})$

Danamatan.	0	Pin	Value			Unit	Ddes
Parameter	Symbol	name	Min	Тур	Max Office		Remarks
			61.5	_	2000	ns	When the main external clock is used Min: F _{CH} = 32.5 MHz, divided by 2 Max: F _{CH} = 1 MHz, divided by 2
Source clock cycle time*1	t _{SCLK}	_	100	_	1000	ns	When the main CR clock is used Min: F _{CRH} = 10 MHz Max: F _{CRH} = 1 MHz
			_	61		μs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			_	20		μs	When the sub CR clock is used F _{CRL} = 100 kHz, divided by 2
	F _{SP}		0.5	_	16.25	MHz	When the main oscillation clock is used
Source clock	SP		1	_	10	MHz	When the main CR clock is used
frequency		_	_	16.384	_	kHz	When the sub-oscillation clock is used
	F _{SPL}		_	50	_	kHz	When the sub-CR clock is used F _{CRL} = 100 kHz, divided by 2
			61.5	_	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
Machine clock cycle time*2 (minimum			100	_	16000	ns	When the main CR clock is used Min: F _{SP} = 10 MHz Max: F _{SP} = 1 MHz, divided by 16
instruction execution time)	t _{MCLK}		61	_	976.5	μs	When the sub-oscillation clock is used Min: F _{SPL} = 16.384 kHz, no division Max: F _{SPL} = 16.384 kHz, divided by 16
			20	_	320	μs	When the sub-CR clock is used Min: F _{SPL} = 50 kHz, no division Max: F _{SPL} = 50 kHz, divided by 16
	Е		0.031	_	16.25	MHz	When the main oscillation clock is used
Machine clock	F _{MP}		0.0625	_	10	MHz	When the main CR clock is used
frequency] —	1.024	_	16.384	kHz	When the sub-oscillation clock is used
почистоу	F _{MPL}		3.125	_	50	kHz	When the sub-CR clock is used F _{CRL} = 100 kHz

^{*1:} This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC: DIV1 and DIV0). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC: DIV1 and DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

- Source clock (no division)
- · Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

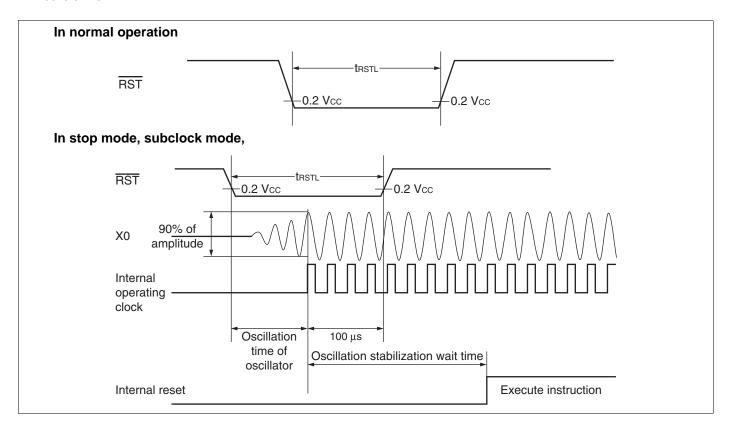
^{*2:} This is the operating clock of the microcontroller. A machine clock can be selected from the following.



24.4.3 External Reset

Parameter	Symbol	Value			Remarks	
	Syllibol	Min	Max	Unit	ivemark2	
RST "L" level pulse width		2 t _{MCLK} *1	_	ns	In normal operation	
	t _{RSTL}	Oscillation time of the oscillator* ² + 100	_		In stop mode, subclock mode, sub-sleep mode, watch mode, and power-on	
		100	_	μs	In time-base timer mode	

- *1: See "24.4.2. Source Clock / Machine Clock" for t_{MCLK}.
- *2 : The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of μs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several μs and several ms.



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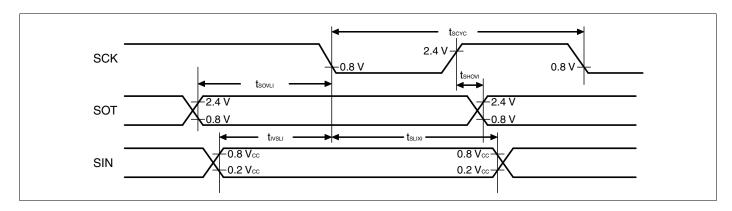
Sampling is executed at the rising edge of the sampling clock*1, and $serial\ clock\ delay\ is\ enabled*2$. (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

$(V_{CC} = 5.0 V \pm 10\%,$	$V_{CC} = 0.0 \text{ V. } T_A$	$= -40^{\circ}$ C to	+ 85°C)
(V()() = 0.0 V ± 10 /0,	VSS - 0.0 V, 1A	- - 0 0 10	. 00 0,

Parameter	Symbol	Pin name	Condition	Val	Unit		
Parameter	Symbol	rin name	Condition	Min	Max	Oiiit	
Serial clock cycle time	t _{SCYC}	SCK		5 t _{MCLK} *3	_	ns	
SCK ↑→ SOT delay time	t _{SHOVI}	SCK, SOT	Internal clock	- 95	+ 95	ns	
$Valid\;SIN\toSCK\;\!\downarrow$	t _{IVSLI}	SCK, SIN	operation output pin:	t _{MCLK} *3 + 190	_	ns	
$SCK \downarrow \to valid \; SIN \; hold \; time$	t _{SLIXI}	SCK, SIN	C _L = 80 pF + 1 TTL	0	_	ns	
$SOT \to SCK \downarrow delay\ time$	t _{SOVLI}	SCK, SOT		_	4 t _{MCLK} *3	ns	

^{*1:} There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

^{*3:} See "24.4.2. Source Clock / Machine Clock" for t_{MCLK}.



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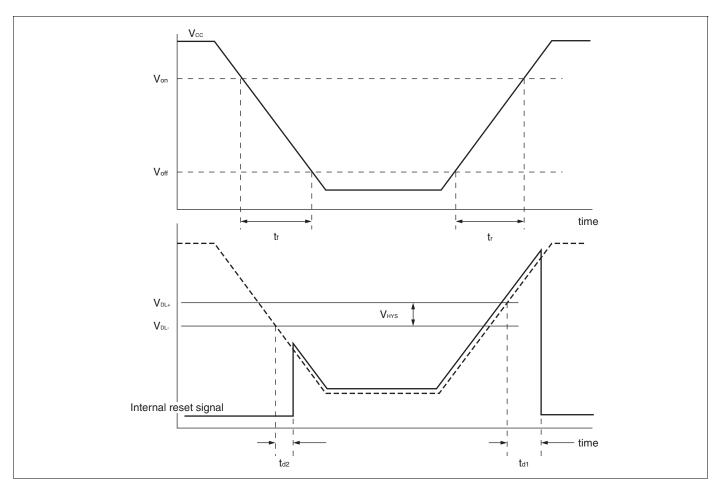
^{*2:} The serial clock delay function is a function that delays the output signal of the serial clock for half clock.



24.4.7 Low-voltage Detection

 $(V_{SS} = 0.0 \text{ V}, T_A = -40^{\circ}\text{C to } + 85^{\circ}\text{C})$

Parameter	Symbol	Value		Unit	Remarks		
Parameter	Syllibol	Min	Тур	Max	Offic	Kellidiks	
Release voltage	V _{DL+}	2.52	2.7	2.88	V	At power supply rise	
Detection voltage	V _{DL} -	2.42	2.6	2.78	V	At power supply fall	
Hysteresis width	V _{HYS}	70	100	_	mV		
Power supply start voltage	V _{off}	_	_	2.3	V		
Power supply end voltage	V _{on}	4.9	_	_	V		
Power supply voltage change time (at power supply rise)	t _r	3000	_	_	μs	Slope of power supply that the reset release signal generates within the rating (V _{DL+})	
Power supply voltage change time (at power supply fall)	t _f	300	_	_	μs	Slope of power supply that the reset detection signal generates within the rating (V _{DL} -)	
Reset release delay time	t _{d1}	_	_	300	μs		
Reset detection delay time	t _{d2}	_	_	20	μs		





24.5 A/D Converter

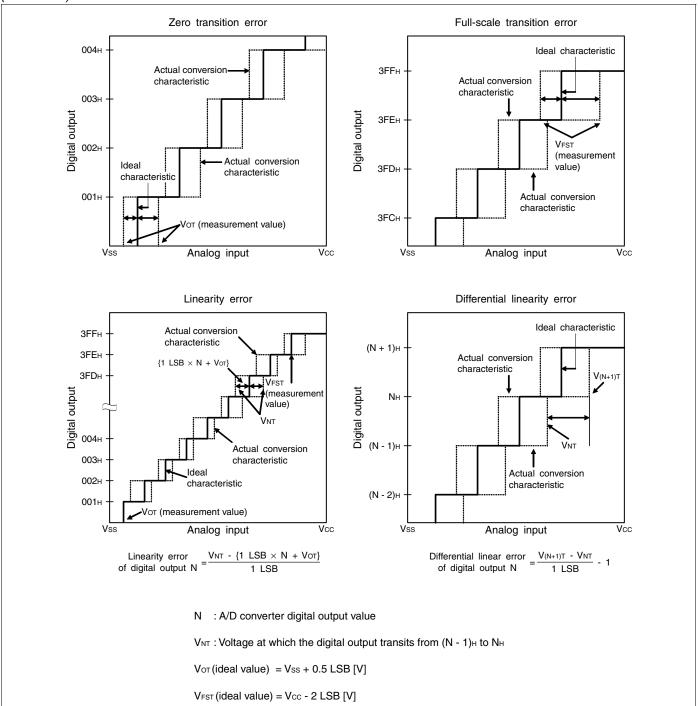
24.5.1 A/D Converter Electrical Characteristics

 $(V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40^{\circ}\text{C to } + 85^{\circ}\text{C})$

Parameter	Symbol	Value				Remarks
Parameter	Symbol	Min Typ		Max	Unit	Remarks
Resolution		_	_	10	bit	
Total error		- 3	_	+ 3	LSB	
Linearity error		- 2.5	_	+ 2.5	LSB	
Differential linear error		- 1.9	_	+ 1.9	LSB	
Zero transition voltage	V _{OT}	V _{SS} - 1.5 LSB	V _{SS} + 0.5 LSB	V _{SS} + 2.5 LSB	V	
Full-scale transition voltage	V _{FST}	V _{CC} - 4.5 LSB	V _{CC} - 2 LSB	V _{CC} + 0.5 LSB	٧	
Compare time		0.9	_	16500	μs	$4.5 \text{ V} \le \text{V}_{CC} \le 5.5 \text{ V}$
Compare time	_	1.8	_	16500	μs	4.0 V ≤ V _{CC} < 4.5 V
Sampling time		0.6	_	∞	μs	$4.5 \text{ V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{ V}$, with external impedance $< 5.4 \text{ k}\Omega$
Sampling time	_	1.2	_	∞	μs	$4.0 \text{ V} \le \text{V}_{CC} < 4.5 \text{ V}$, with external impedance < $2.4 \text{ k}\Omega$
Analog input current	I _{AIN}	- 0.3	_	+ 0.3	μΑ	
Analog input voltage	V _{AIN}	V _{SS}	_	V _{CC}	V	

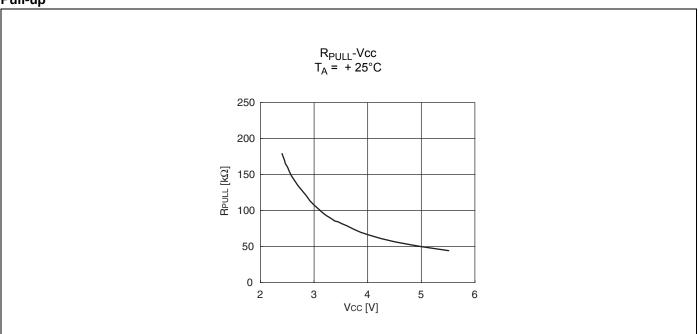
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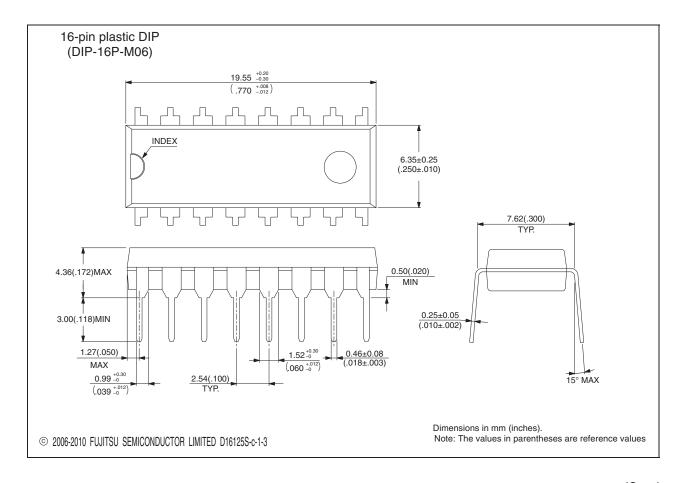


27. Ordering Information

Part Number	Package
MB95F262HWQN-G-SNE1	
MB95F262HWQN-G-SNERE1	
MB95F262KWQN-G-SNE1	
MB95F262KWQN-G-SNERE1	
MB95F263HWQN-G-SNE1	
MB95F263HWQN-G-SNERE1	32-pin plastic QFN
MB95F263KWQN-G-SNE1	(LCC-32P-M19)
MB95F263KWQN-G-SNERE1	
MB95F264HWQN-G-SNE1	
MB95F264HWQN-G-SNERE1	
MB95F264KWQN-G-SNE1	
MB95F264KWQN-G-SNERE1	
MB95F262HP-G-SH-SNE2	
MB95F262KP-G-SH-SNE2	
MB95F263HP-G-SH-SNE2	24-pin plastic SDIP
MB95F263KP-G-SH-SNE2	(DIP-24P-M07)
MB95F264HP-G-SH-SNE2	
MB95F264KP-G-SH-SNE2	
MB95F262HPF-G-SNE2	
MB95F262KPF-G-SNE2	
MB95F263HPF-G-SNE2	20-pin plastic SOP
MB95F263KPF-G-SNE2	(FPT-20P-M09)
MB95F264HPF-G-SNE2	, ,
MB95F264KPF-G-SNE2	
MB95F262HPFT-G-SNE2	
MB95F262KPFT-G-SNE2	
MB95F263HPFT-G-SNE2	20-pin plastic TSSOP
MB95F263KPFT-G-SNE2	(FPT-20P-M10)
MB95F264HPFT-G-SNE2	,
MB95F264KPFT-G-SNE2	
MB95F282HWQN-G-SNE1	
MB95F282HWQN-G-SNERE1	
MB95F282KWQN-G-SNE1	
MB95F282KWQN-G-SNERE1	
MB95F283HWQN-G-SNE1	
MB95F283HWQN-G-SNERE1	32-pin plastic QFN
MB95F283KWQN-G-SNE1	(LCC-32P-M19)
MB95F283KWQN-G-SNERE1	,
MB95F284HWQN-G-SNE1	
MB95F284HWQN-G-SNERE1	
MB95F284KWQN-G-SNE1	
MB95F284KWQN-G-SNERE1	
MB95F282HPH-G-SNE2	
MB95F282KPH-G-SNE2	
MB95F283HPH-G-SNE2	16-pin plastic DIP
MB95F283KPH-G-SNE2	(DIP-16P-M06)
MB95F284HPH-G-SNE2	
MB95F284KPH-G-SNE2	



16-pin plastic DIP	Lead pitch	2.54 mm
	Sealing method	Plastic mold
(DIP-16P-M06)		





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