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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I ² C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20224-12lkxi

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Typical Application

Figure 2 illustrates a typical application: CapSense multimedia keys for a notebook computer with a slider, four buttons, and four LEDs.

Figure 2. CapSense Multimedia Button-Board Application



Additional System Resources

System resources, some of which are previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection (LVD) and power on reset (POR). Brief statements describing the merits of each system resource follow.

- The I²C slave and SPI master-slave module provides 50, 100, or 400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- LVD interrupts signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.8-V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

Getting Started

This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC[®] Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.



Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
- Hardware and software I²C slaves and masters
- □ Full-speed USB 2.0
- □ Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.



Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

- 1. Select user modules.
- 2. Configure user modules.
- 3. Organize and connect.
- 4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules". User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, an EzI2Cs User Module configures the I²C block in PSoC. Using these parameters, you can establish the slave address and I²C speed. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module data sheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals



24-pin Part Pinout

Figure 4. CY8C20324 24-pin PSoC Device



Table 2. 24-pin Part Pinout (QFN [2])

Pin No.	Digital	Analog	Name	Description					
1	I/O	I	P2[5]						
2	I/O	I	P2[3]						
3	I/O	I	P2[1]						
4	I _{OH}	I	P1[7]	I ² C SCL, SPI SS					
5	I _{OH}	I	P1[5]	I ² C SDA, SPI MISO					
6	I _{OH}	I	P1[3]	SPI CLK					
7	I _{OH}	I	P1[1]	CLK ^[3] , I ² C SCL, SPI MOSI					
8			NC	No connection					
9	Po	ower	V _{SS}	Ground connection					
10	I _{OH}	I	P1[0]	DATA ^[3] , I ² C SDA					
11	I _{ОН}	I	P1[2]						
12	I _{ОН}	I	P1[4]	Optional external clock input (EXTCLK)					
13	I _{ОН}	Ι	P1[6]						
14	Ir	iput	XRES	Active high external reset with internal pull-down					
15	I/O	I	P2[0]						
16	I/O	I	P0[0]						
17	I/O	I	P0[2]						
18	I/O	I	P0[4]						
19	I/O	I	P0[6]						
20	Po	ower	V _{DD}	Supply voltage					
21	I/O	I	P0[7]						
22	I/O	I	P0[5]						
23	I/O	I	P0[3]	Integrating input					
24	I/O	I	P0[1]	Integrating input					
CP	Po	ower	Vss	Center pad is connected to ground					

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Notes

The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
 These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.



28-pin Part Pinout



Figure 5. CY8C20524 28-pin PSoC Device

Table 3. 28-pin Part Pinout (SSOP)

Pin No.	Digital	Analog	Name	Description			
1	I/O	I	P0[7]				
2	I/O	I	P0[5]				
3	I/O	I	P0[3]	Integrating input			
4	I/O	I	P0[1]	Integrating input			
5	I/O	I	P2[7]				
6	I/O	I	P2[5]				
7	I/O	I	P2[3]				
8	I/O	I	P2[1]				
9	Po	wer	V _{SS}	Ground connection			
10	I _{ОН}	I	P1[7]	I ² C SCL, SPI SS			
11	I _{OH}	I	P1[5]	I ² C SDA, SPI MISO			
12	I _{OH}	I	P1[3]	SPI CLK			
13	I _{OH}	I	P1[1]	CLK ^[4] , I ² C SCL, SPL MOSI			
14	Po	wer	V _{SS}	Ground connection			
15	I _{ОН}	I	P1[0]	Data ^[4] , I ² C SDA			
16	I _{ОН}	I	P1[2]				
17	I _{OH}	I	P1[4]	Optional external clock input (EXTCLK)			
18	I _{OH}	I	P1[6]				
19	In	put	XRES	Active high external reset with internal pull-down			
20	I/O	I	P2[0]				
21	I/O	I	P2[2]				
22	I/O	I	P2[4]				
23	I/O	I	P2[6]				
24	I/O	I	P0[0]				
25	I/O		P0[2]				
26	I/O	I	P0[4]				
27	I/O	I	P0[6]				
28	Po	wer	V _{DD}	Supply voltage			

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note

4. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the PSoC Programmable System-on-Chip Technical Reference Manual for details.



48-pin OCD Part Pinout

The 48-pin QFN part table and pin diagram is for the CY8C20024 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.



	• p • • • •		, , ,				
Pin No.	Digital	Analog	Name	Description			
1			NC	No connection			
2	I/O	I	P0[1]	ntegrating Input			
3	I/O	I	P2[7]				
4	I/O	I	P2[5]				
5	I/O	I	P2[3]				
6	I/O	I	P2[1]				
7	I/O	I	P3[3]				
8	I/O	I	P3[1]				
9	I _{OH}	I	P1[7]	I ² C SCL, SPI SS			
10	I _{OH}	I	P1[5]	I ² C SDA, SPI MISO			
11			NC	No connection			
12			NC	No connection			
13			NC	No connection			
14			NC	No connection			
15	I _{OH}	I	P1[3]	SPICLK			
16	I _{OH}	I	P1[1]	CLK ^[8] , I ² C SCL, SPI MOSI			
17	Po	wer	Vss	Ground connection			
18			CCLK	OCD CPU clock output			
19			HCLK	OCD high speed clock output			
20	I _{OH}	I	P1[0]	DATA ^[8] , I ² C SDA			

Table 5. 48-pin OCD Part Pinout (QFN^[7])

Notes

7. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.

8. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the PSoC Programmable System-on-Chip Technical Reference Manual for details.



Pin No.	Digital	Analog	Name	Description			
21	I _{OH}	I	P1[2]				
22			NC	No connection			
23			NC	No connection			
24			NC	No connection			
25	I _{OH}	I	P1[4]	Optional external clock input (EXTCLK)			
26	I _{OH}	I	P1[6]				
27	In	put	XRES	Active high external reset with internal pull-down			
28	I/O	I	P3[0]				
29	I/O	I	P3[2]				
30	I/O	I	P2[0]				
31	I/O	I	P2[2]				
32	I/O	I	P2[4]				
33	I/O	I	P2[6]				
34	I/O	I	P0[0]				
35	I/O	I	P0[2]				
36	I/O	I	P0[4]				
37		•	NC	No connection			
38			NC	No connection			
39			NC	No connection			
40	I/O	I	P0[6]				
41	Po	wer	V _{DD}	Supply voltage			
42			OCDO	OCD odd data output			
43			OCDE	OCD even data I/O			
44	I/O	I	P0[7]				
45	I/O	I	P0[5]				
46	I/O	I	P0[3]	Integrating input			
47	Po	wer	V _{SS}	Ground connection			
48			NC	No connection			
CP	Po	wer	V _{SS}	Center pad is connected to ground			

Table 5. 48-pin OCD Part Pinout (QFN ^[7]) (continued)

A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive.



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC devices. For the latest electrical specifications, visit the web at http://www.cypress.com/psoc.

Specifications are valid for –40 $^\circ C \le T_A \le 85$ $^\circ C$ and $T_J \le 100$ $^\circ C$ as specified, except where noted.

Refer to Table 16 on page 19 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 8. Voltage versus CPU Frequency and IMO Frequency Trim Options





Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Тур	Max	Units	Notes
T _{STG}	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
T _A	Ambient temperature with power applied	-40	-	+85	°C	
V _{DD}	Supply voltage on V_{DD} relative to V_{SS}	-0.5	-	+6.0	V	
V _{IO}	DC input voltage	$V_{SS} - 0.5$	-	V _{DD} + 0.5	V	
V _{IOZ}	DC voltage applied to tri-state	$V_{SS} - 0.5$	-	V _{DD} + 0.5	V	
I _{MIO}	Maximum current into any port pin	-25	-	+50	mA	
ESD	Electrostatic discharge voltage	2000	-	-	V	Human Body Model ESD.
LU	Latch-up current	-	-	200	mA	

Operating Temperature

Table 7. Operating Temperature

Symbol	Description	Min	Тур	Мах	Units	Notes
T _A	Ambient temperature	-40	-	+85	°C	
Тյ	Junction temperature	-40	_	+100	°C	The temperature rise from ambient to junction is package specific. See Table 31 on page 30. The user must limit the power consumption to comply with this requirement.



Table 9. 5 V and 3.3 V DC GPIO Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OL}	Low output voltage	-	_	0.75	V	I_{OL} = 20 mA, V_{DD} > 3.0V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I _{OH2}	High level source current, port 0, 2, or 3 pins	1	_	-	mA	$V_{OH} = V_{DD} - 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH} .
I _{OH4}	High level source current, port 1 pins with LDO regulator disabled	5	_	_	mA	$V_{OH} = V_{DD} - 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH} .
I _{OL}	Low level sink current	20	-	-	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL} .
V _{IL}	Input low voltage	-	-	0.8	V	$3.0~V \leq V_{DD} \leq 5.25~V$
V _{IH}	Input high voltage	2.0	-		V	$3.0~V \leq V_{DD} \leq 5.25~V$
V _H	Input hysteresis voltage	-	140	-	mV	
IIL	Input leakage (absolute value)	-	1	-	nA	Gross tested to 1 µA
C _{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C
C _{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C

Table 10. 2.7 V DC GPIO Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
R _{PU}	Pull-up resistor	4	5.6	8	kΩ	
V _{OH1}	High output voltage, port 1 pins with LDO regulator disabled	V _{DD} – 0.2	-	_	V	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os.
V _{OH2}	High output voltage, port 1 pins with LDO regulator disabled	V _{DD} – 0.5	-	_	V	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V _{OL}	Low output voltage	_	_	0.75	V	I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I _{OH2}	High level source current, port 1 pins with LDO regulator disabled	2	-	_	mA	$V_{OH} = V_{DD} - 0.5$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH} .
I _{OL}	Low level sink current	10	-	-	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL} .
V _{OLP1}	Low output voltage port 1 pins	-	_	0.4	V	IOL = 5 mA, maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V \leq V _{DD} \leq 3.0 V
V _{IL}	Input low voltage	-	-	0.75	V	$2.4 \text{ V} \leq \text{V}_{DD} \leq 3.0 \text{ V}$
V _{IH1}	Input high voltage	1.4	_	-	V	$2.4 \text{ V} \leq \text{V}_{DD} \leq 2.7 \text{ V}$
V _{IH2}	Input high voltage	1.6	_	_	V	$2.7 \text{ V} \le \text{V}_{DD} \le 3.0 \text{ V}$
V _H	Input hysteresis voltage	_	60	_	mV	
IIL	Input leakage (absolute value)	-	1		nA	Gross tested to 1 µA



Table 10. 2.7 V DC GPIO Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
C _{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C
C _{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C

DC Analog Mux Bus Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 $^{\circ}C \leq T_A \leq 85 \,^{\circ}C$, 3.0 V to 3.6 V and –40 $^{\circ}C \leq T_A \leq 85 \,^{\circ}C$, or 2.4 V to 3.0 V and –40 $^{\circ}C \leq T_A \leq 85 \,^{\circ}C$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 $^{\circ}C$. These are for design guidance only.

Table 11. DC Analog Mux Bus Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
R _{SW}	Switch resistance to common analog bus	-	-	400 800	Ω Ω	$\begin{array}{l} Vdd \geq 2.7 \ V \\ 2.4 \ V \leq Vdd \leq 2.7 \ V \end{array}$

DC Low Power Comparator Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 12. DC Low Power Comparator Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	-	V _{DD} – 1.0	V	
I _{SLPC}	LPC supply current	-	10	40	μA	
V _{OSLPC}	LPC voltage offset	-	2.5	30	mV	

DC POR and LVD Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 13. DC POR and LVD Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
VPPOR0 VPPOR1 VPPOR2	V _{DD} value for PPOR trip PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b		2.36 2.60 2.82	2.40 2.65 2.95	V V V	V _{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
VLVD0 VLVD1 VLVD2 VLVD3 VLVD4 VLVD5 VLVD6 VLVD7	V _{DD} value for LVD trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.39 2.54 2.75 2.85 2.96 - - 4.52	2.45 2.71 2.92 3.02 3.13 - 4.73	2.51 ^[9] 2.78 ^[10] 2.99 ^[11] 3.09 3.20 - - 4.83	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	

Notes

9. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.

10. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply. 11. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.



AC Electrical Characteristics

AC Chip Level Specifications

Table 16 and Table 17 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and –40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and –40 °C \leq T_A \leq 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{CPU1}	CPU frequency (3.3 V nominal)	0.75	-	12.6	MHz	12 MHz only for SLIMO Mode = 0
F _{32K1}	ILO frequency	15	32	64	kHz	
F _{32K_U}	ILO untrimmed frequency	5	_	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F _{IMO12}	IMO stability for 12 MHz (Commercial temperature) ^[15]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F _{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DCIMO	Duty cycle of IMO	40	50	60	%	
DC _{ILO}	ILO duty cycle	20	50	80	%	
t _{RAMP}	Supply ramp time	0	-	-	μs	
t _{XRST}	External reset pulse width	10	-	-	μs	
t _{POWERUP}	Time from end of POR to CPU executing code	-	16	100	ms	Power up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t _{jit_IMO} ^[16]	12 MHz IMO cycle-to-cycle jitter (RMS)	-	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	-	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	_	100	900	ps	

Notes 15.0 °C to 70 °C ambient, V_{DD} = 3.3 V. 16. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.



Table 17. 2.7 V AC Chip Level Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{CPU1A}	CPU frequency (2.7 V nominal)	0.75	-	3.25	MHz	2.4 V < V _{DD} < 3.0 V.
F _{CPU1B}	CPU frequency (2.7 V minimum)	0.75	-	6.3	MHz	2.7 V < V _{DD} < 3.0 V.
F _{32K1}	ILO frequency	8	32	96	kHz	
F _{32K_U}	ILO untrimmed frequency	5	-	-	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F _{IMO12}	IMO stability for 12 MHz (Commercial temperature) ^[17]	11.0	12	12.9	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F _{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DCIMO	Duty cycle of IMO	40	50	60	%	
DC _{ILO}	ILO duty cycle	20	50	80	%	
t _{RAMP}	Supply ramp time	0	-	-	μs	
t _{XRST}	External reset pulse width	10	-	-	μs	
t _{POWERUP}		_	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t _{jit_IMO} ^[18]	12 MHz IMO cycle-to-cycle jitter (RMS)	-	500	900	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	-	800	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	_	300	500	ps	

Notes 17.0 °C to 70 °C ambient, V_{DD} = 3.3 V. 18. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.



Table 24. 2.7 V AC External Clock Specifications (continued)

Symbol	Description	Min	Тур	Мах	Units	Notes
F _{OSCEXT2B}	Frequency with CPU clock divide by 2 or greater (2.7 V minimum)	1.5	_	12.6	MHz	$2.7 V < V_{DD} < 3.0 V$. If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
-	High period with CPU clock divide by 1	160	-	5300	ns	
-	Low period with CPU clock divide by 1	160	-	_	ns	
-	Power-up IMO to switch	150	_	-	μs	

AC Programming Specifications

Table 25 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Symbol	Description	Min	Тур	Max	Units	Notes
t _{RSCLK}	Rise time of SCLK	1	-	20	ns	
t _{FSCLK}	Fall time of SCLK	1	-	20	ns	
t _{SSCLK}	Data set up time to falling edge of SCLK	40	-	-	ns	
t _{HSCLK}	Data hold time from falling edge of SCLK	40	-	-	ns	
F _{SCLK}	Frequency of SCLK	0	-	8	MHz	
t _{ERASEB}	Flash erase time (Block)	-	10	-	ms	
t _{WRITE}	Flash block write time	-	40	-	ms	
t _{DSCLK}	Data out delay from falling edge of SCLK	-	_	45	ns	3.6 < V _{DD}
t _{DSCLK3}	Data out delay from falling edge of SCLK	-	-	50	ns	$3.0 \le V_{DD} \le 3.6$
t _{DSCLK2}	Data out delay from falling edge of SCLK	-	-	70	ns	$2.4 \le V_{DD} \le 3.0$
t _{ERASEALL}	Flash erase time (Bulk)	-	20	-	ms	Erase all blocks and protection fields at once
t _{PROGRAM_HOT}	Flash block erase + Flash block write time	-	-	100	ms	$0 \ ^{\circ}C \le Tj \le 100 \ ^{\circ}C$
t _{PROGRAM_} COLD	Flash block erase + Flash block write time	-	-	200	ms	$-40 \ ^{\circ}C \leq Tj \leq 0 \ ^{\circ}C$

Table 25. AC Programming Specifications



AC I²C Specifications

Table 26 and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and –40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and –40 °C \leq T_A \leq 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table OC	10	Chavesteristics	af 4h a	120 004	and 001	Dine fe	
Table 26.	AC	Characteristics	or the	I-C SDA	and SCL	PINS TO	⊺ V _{DD} ≥ 3.0 V

Symbol	Description	Standard Mode Fast Mode		Mode	Unite	Inite Notos	
Gymbol	Description	Min	Max	Min	Max	Units	Notes
F _{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
t _{HDSTAI2C}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	-	0.6	-	μs	
t _{LOWI2C}	LOW period of the SCL clock	4.7	-	1.3	-	μs	
t _{HIGHI2C}	HIGH period of the SCL clock	4.0	-	0.6	-	μs	
t _{SUSTAI2C}	Setup time for a repeated START condition	4.7	-	0.6	-	μs	
t _{HDDATI2C}	Data hold time	0	-	0	-	μs	
t _{SUDATI2C}	Data setup time	250	-	100 ^[19]	-	ns	
t _{SUSTOI2C}	Setup time for STOP condition	4.0	-	0.6	-	μs	
t _{BUFI2C}	Bus free time between a STOP and START condition	4.7	-	1.3	-	μs	
t _{SPI2C}	Pulse width of spikes are suppressed by the input filter	-	-	0	50	ns	

Table 27. 2.7 V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not supported)

Symbol	Description	Standard Mode		Fast	Mode	Unite	Notos
Symbol	Description	Min	Max	Min	Мах	Units	Notes
F _{SCLI2C}	SCL clock frequency	0	100	-	-	kHz	
t _{HDSTAI2C}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	-	-	_	μs	
t _{LOWI2C}	LOW period of the SCL clock	4.7	-	-	-	μs	
t _{HIGHI2C}	HIGH period of the SCL clock	4.0	-	-	-	μs	
t _{SUSTAI2C}	Setup time for a repeated START condition	4.7	-	-	-	μs	
t _{HDDATI2C}	Data hold time	0	-	-	-	μs	
t _{SUDATI2C}	Data setup time	250	-	-	-	ns	
t _{SUSTOI2C}	Setup time for STOP condition	4.0	-	-	-	μs	
t _{BUFI2C}	Bus free time between a STOP and START condition	4.7	-	_	-	μs	
t _{SPI2C}	Pulse width of spikes are suppressed by the input filter.	-	-	-	-	ns	

Note 19. A Fast Mode I^2C bus device is used in a Standard Mode I^2C bus system but the requirement $T_{SUDAT} \ge 250$ ns is met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + $T_{SUDAT} = 1000 + 250 = 1250$ ns (according to the Standard Mode I^2C bus specification) before the SCL line is released.



Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- Two CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack



Acronyms

Acronyms Used

Table 34 lists the acronyms that are used in this document.

Table 34. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PGA	programmable gain amplifier
CPU	central processing unit	POR	power on reset
EEPROM	electrically erasable programmable read-only memory	PPOR	precision power on reset
GPIO	general purpose I/O	PSoC®	Programmable System-on-Chip
ICE	in-circuit emulator	PWM	pulse width modulator
IDAC	current DAC	QFN	quad flat no leads
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SPI [™]	serial peripheral interface
IMO	internal main oscillator	SRAM	static random access memory
I/O	input/output	SROM	supervisory read only memory
ISSP	in-system serial programming	SSOP	shrink small-outline package
LCD	liquid crystal display	USB	universal serial bus
LDO		WDT	watchdog timer
LED	light-emitting diode	WLCSP	wafer level chip scale package
LVD	low voltage detect	XRES	external reset
MCU	microcontroller unit		•

Reference Documents

PSoC[®] CY8C20x34 and PSoC[®] CY8C20x24 Technical Reference Manual (TRM) – 001-13033

Design Aids – Reading and Writing $PSoC^{(8)}$ Flash – AN2015 (001-40459)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.



Glossary (continued)

External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I ² C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.
	The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the <i>slave device</i> .
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.



Glossary (continued)

modulator	A device that imposes a signal on a carrier.
noise	 A disturbance that affects a signal and that may distort the information carried by the signal. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC [®]	Cypress Semiconductor's PSoC [®] is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	 Pertaining to a process in which all events occur one after the other. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.



Glossary (continued)

SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	 A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V _{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V _{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.



Document History Page

Document Title: CY8C20224/CY8C20324/CY8C20424/CY8C20524, CapSense [®] PSoC [®] Programmable System-on-Chip™ Document Number: 001-41947				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1734104	YHW / AESA	See ECN	New parts and document (Revision **).
*A	2542938	RLRM / AESA	07/28/2008	Corrected Ordering Information format. Updated package diagram 001-13937 to Rev *B. Updated to new template.
*B	2610469	SNV / PYRS	11/20/08	Updated $V_{OH5},V_{OH7},\text{and}V_{OH9}$ specifications.
*C	2634376	DRSW	01/12/09	Changed status from Preliminary to Final. Removed the part number CY3250-20234QFN from the 'CY8C20224-12LKXI' flex-pod kit Changed title from CapSense™ Multimedia PSoC [®] Mixed-Signal Array to CapSense™ Multimedia PSoC [®] Programmable System-on-Chip™ Added -12 to the CY8C20524 parts in the Ordering Information table Updated 'Development Tools' and 'Designing with PSoC Designer' sections on pages 4 and 5 Updated 'Development Tools Selection' section on page 30 Changed 16-Pin from QFN to COL
*D	2693024	DPT / PYRS	04/16/2009	Added devices CY8C20424-12LQXI and CY8C20424-12LQXIT in the Ordering Information table Added 32-Pin Sawn QFN package diagram
*E	2717566	DRSW / AESA	06/11/2009	Updated AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 (page 19), TWRITE specifications (page 22) Added IOH & IOL (page 16), Flash endurance note (page 18), DCILO (page 19), F32K_U (page 19), TPOWERUP (page 19), TERASEALL (page 22), TPROGRAM_HOT (page 22), and TPROGRAM_COLD (page 22) specifications Added AC SPI Master and Slave Specifications
*F	2899195	CFW / ISW	03/26/2010	Updated Ordering Information. Updated Package Diagrams.
*G	3037121	CFW	09/24/2010	Updated title to read AC Comparator Specifications and also updated table caption to read "AC Comparator Specifications" in the same section. Minor edits. Updated to new template.
*H	3049675	ВТК	10/06/2010	Removed AC analog mux bus specifications. Updated Development Tools and Designing with PSoC Designer sections.
*	3072668	NJF	10/27/10	Added PSoC Device Characteristics table. Added DC I ² C Specifications table. Added F _{32K U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changed were made to I ² C Timing Diagram. Updated for clearer understanding. Updated to new template.
*J	3112469	ARVM	12/16/10	Updated Ordering Information: Updated part numbers.
*K	3182773	MATT	03/01/11	No technical updates. Completing Sunset Review.