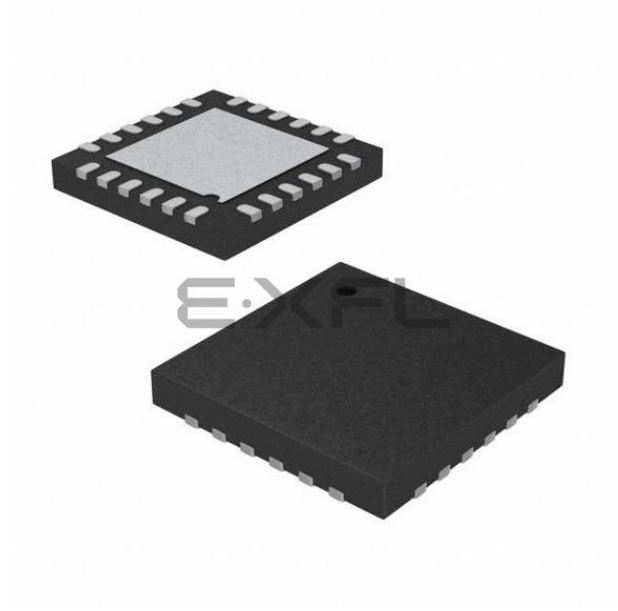

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	20
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20324-12lqxi

PSoC® Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip controller devices. These devices are designed to replace multiple traditional MCU based system components with one, low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture enables the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family is comprised of three main areas: core, system resources, and CapSense analog system. A common, versatile bus enables connection between I/O and the analog system. Each CY8C20x24 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a 2-MIPS, 8-bit Harvard-architecture microprocessor.

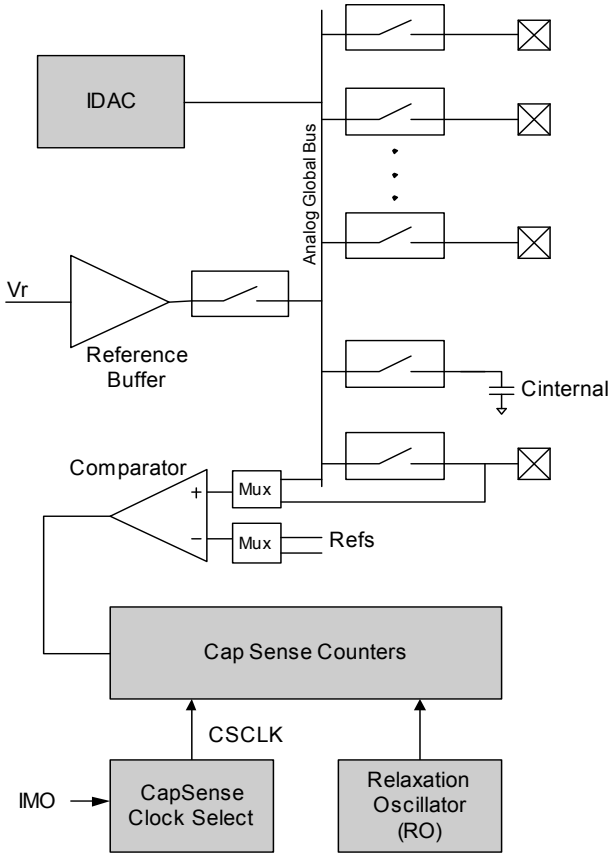
System resources provide additional capability, such as a configurable I^2C slave or SPI master-slave communication interface and various system resets supported by the M8C.

The analog system is composed of the CapSense PSoC block and an internal 1.8-V analog reference. Together, they support capacitive sensing of up to 28 inputs.

CapSense Analog System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The analog mux bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. The analog multiplexer system in the CY8C20x24 device family is optimized for basic CapSense functionality. It supports sensing of CapSense buttons, proximity sensors, and a single slider. Other multiplexer applications include:

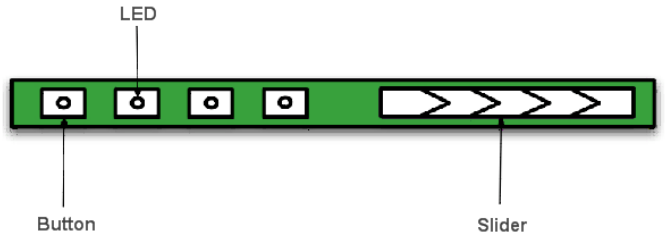
- Capacitive slider interface.
- Chip-wide mux that enables analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

When designing capacitive sensing applications, refer to the latest signal to noise signal level requirements application notes, which are found in http://www.cypress.com > Design Resources > Application Notes. In general, and unless otherwise noted in the relevant application notes, the minimum signal-to-noise ratio (SNR) requirement for CapSense applications is 5:1.

Typical Application

Figure 2 illustrates a typical application: CapSense multimedia keys for a notebook computer with a slider, four buttons, and four LEDs.

Figure 2. CapSense Multimedia Button-Board Application



Additional System Resources

System resources, some of which are previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection (LVD) and power on reset (POR). Brief statements describing the merits of each system resource follow.

- The I^2C slave and SPI master-slave module provides 50, 100, or 400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- LVD interrupts signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.8-V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

Getting Started

This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

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Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

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Pinouts

This section describes, lists, and illustrates the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC device pins and pinout configurations.

The CY8C20x24 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

16-pin Part Pinout

Figure 3. CY8C20224 16-pin PSoC Device

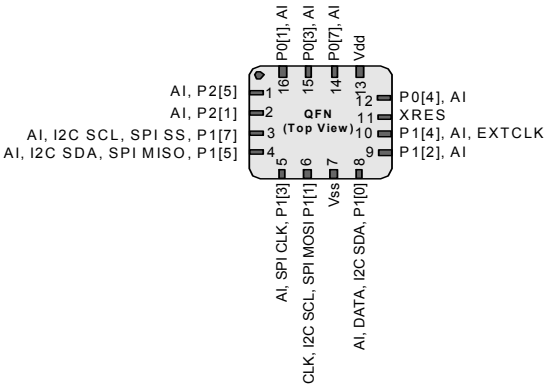


Table 1. 16-pin Part Pinout (COL)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
5	I_{OH}	I	P1[3]	SPI CLK
6	I_{OH}	I	P1[1]	CLK[1], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	I_{OH}	I	P1[0]	DATA[1], I^2C SDA
9	I_{OH}	I	P1[2]	
10	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating input
16	I/O	I	P0[1]	Integrating input

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
1. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

24-pin Part Pinout

Figure 4. CY8C20324 24-pin PSoC Device

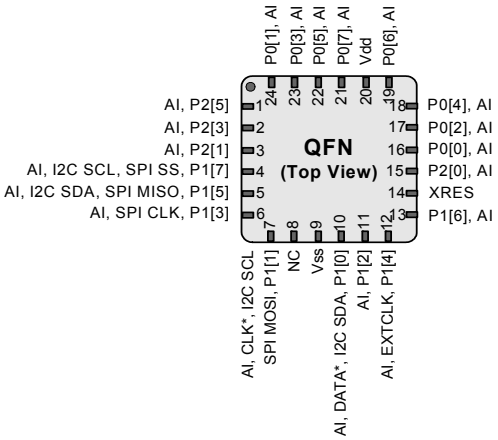


Table 2. 24-pin Part Pinout (QFN [2])

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
5	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
6	I_{OH}	I	P1[3]	SPI CLK
7	I_{OH}	I	P1[1]	CLK[3], I^2C SCL, SPI MOSI
8			NC	No connection
9	Power		V_{SS}	Ground connection
10	I_{OH}	I	P1[0]	DATA[3], I^2C SDA
11	I_{OH}	I	P1[2]	
12	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
13	I_{OH}	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down
15	I/O	I	P2[0]	
16	I/O	I	P0[0]	
17	I/O	I	P0[2]	
18	I/O	I	P0[4]	
19	I/O	I	P0[6]	
20	Power		V_{DD}	Supply voltage
21	I/O	I	P0[7]	
22	I/O	I	P0[5]	
23	I/O	I	P0[3]	Integrating input
24	I/O	I	P0[1]	Integrating input
CP	Power		Vss	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Notes
2. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
3. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

32-pin Part Pinout

Figure 6. CY8C20424 32-pin PSoC Device

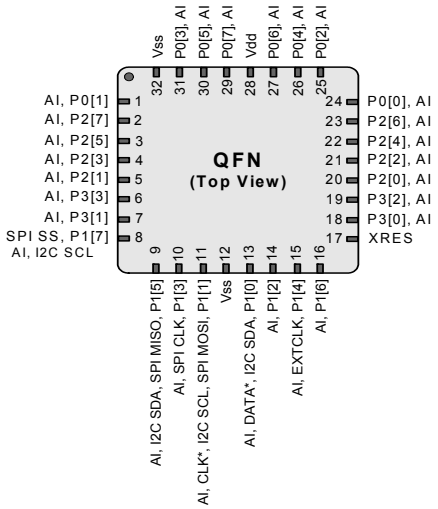


Table 4. 32-pin Part Pinout (QFN [5])

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[1]	Integrating Input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
9	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
10	I_{OH}	I	P1[3]	SPI CLK
11	I_{OH}	I	P1[1]	CLK[6], I^2C SCL, SPI MOSI
12	Power		V_{SS}	Ground connection
13	I_{OH}	I	P1[0]	DATA[6], I^2C SDA
14	I_{OH}	I	P1[2]	
15	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
16	I_{OH}	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down

Notes
5. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
6. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

DC Electrical Characteristics

DC Chip Level Specifications

Table 8 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 8. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz.
I_{SB27}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C.

DC GPIO Specifications

Unless otherwise noted, Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 9. 5 V and 3.3 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.
V_{OH7}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.1	2.4	2.7	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.0	–	–	V	I_{OH} < 200 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.6	1.8	2.0	V	I_{OH} < 10 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤ 85 °C, maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.5	–	–	V	I_{OH} < 100 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ TA ≤ 85 °C, maximum of 20 mA source current in all I/Os.

Table 9. 5 V and 3.3 V DC GPIO Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA, V_{DD} > 3.0V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current, port 0, 2, or 3 pins	1	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OH4}	High level source current, port 1 pins with LDO regulator disabled	5	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	20	–	–	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low voltage	–	–	0.8	V	3.0 V ≤ V_{DD} ≤ 5.25 V
V_{IH}	Input high voltage	2.0	–		V	3.0 V ≤ V_{DD} ≤ 5.25 V
V_H	Input hysteresis voltage	–	140	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C

Table 10. 2.7 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage, port 1 pins with LDO regulator disabled	$V_{DD} – 0.2$	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage, port 1 pins with LDO regulator disabled	$V_{DD} – 0.5$	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current, port 1 pins with LDO regulator disabled	2	–	–	mA	$V_{OH} = V_{DD} – 0.5$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	10	–	–	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	IOL = 5 mA, maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V ≤ V_{DD} ≤ 3.0 V
V_{IL}	Input low voltage	–	–	0.75	V	2.4 V ≤ V_{DD} ≤ 3.0 V
V_{IH1}	Input high voltage	1.4	–	–	V	2.4 V ≤ V_{DD} ≤ 2.7 V
V_{IH2}	Input high voltage	1.6	–	–	V	2.7 V ≤ V_{DD} ≤ 3.0 V
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA

DC Programming Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 14. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[12]	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[13]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 15. DC I^2C Specifications[14]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

Notes
12. The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.
13. A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
14. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

AC Electrical Characteristics

AC Chip Level Specifications

Table 16 and Table 17 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency (3.3 V nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (Commercial temperature)[15]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F_{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{RAMP}	Supply ramp time	0	–	–	µs	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[16]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Notes
15. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
16. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.

Table 17. 2.7 V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1A}	CPU frequency (2.7 V nominal)	0.75	–	3.25	MHz	2.4 V < V_{DD} < 3.0 V.
F_{CPU1B}	CPU frequency (2.7 V minimum)	0.75	–	6.3	MHz	2.7 V < V_{DD} < 3.0 V.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	–	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (Commercial temperature)[17]	11.0	12	12.9	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F_{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{RAMP}	Supply ramp time	0	–	–	µs	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$		–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[18]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	500	900	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	800	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	300	500	ps	

Notes
17. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
18. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.

AC GPIO Specifications

Table 18 an d Table 19 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

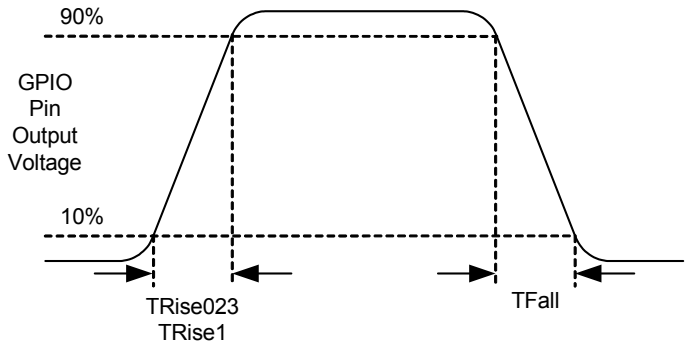
Table 18. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	6	MHz	Normal strong mode, Port 1.
$t_{Rise023}$	Rise time, strong mode, Cload = 50 pF, ports 0, 2, 3	15	–	80	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, port 1	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF, all ports	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%

Table 19. 2.7 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	1.5	MHz	Normal Strong Mode, Port 1.
$t_{Rise023}$	Rise time, strong mode, Cload = 50 pF, ports 0, 2, 3	15	–	100	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, port 1	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF, all ports	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%

Figure 9. GPIO Timing Diagram



AC Comparator Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 20. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator response time, 50 mV overdrive	–	–	100 200	ns ns	V_{DD} ≥ 3.0 V 2.4 V < V_{CC} < 3.0 V

Table 24. 2.7 V AC External Clock Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{OSCEXT2B}$	Frequency with CPU clock divide by 2 or greater (2.7 V minimum)	1.5	–	12.6	MHz	2.7 V < V_{DD} < 3.0 V. If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 25 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 25. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (Block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	40	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	3.6 < V_{DD}
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0
$t_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200	ms	–40 °C ≤ Tj ≤ 0 °C

Ordering Information

Table 30 lists the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC devices key package features and ordering codes.

Table 30. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Maximum Number of Buttons	Maximum Number of Sliders	Maximum Number of LEDs	Configurable LED Behavior (Fade, Strobe)	Proximity Sensing
16-pin (3 × 3 mm 0.60 Max) COL	CY8C20224-12LKXI	8 K	512	10	1	13	Yes	Yes
16-pin (3 × 3 mm 0.60 Max) COL (Tape and Reel)	CY8C20224-12LKXIT	8 K	512	10	1	13	Yes	Yes
24-pin (4 × 4 mm 0.60 Max) QFN	CY8C20324-12LQXI	8 K	512	17	1	20	Yes	Yes
24-pin (4 × 4 mm 0.60 Max) QFN (Tape and Reel)	CY8C20324-12LQXIT	8 K	512	17	1	20	Yes	Yes
28-pin (210-Mil) SSOP	CY8C20524-12PVXI	8 K	512	21	1	24	Yes	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C20524-12PVXIT	8 K	512	21	1	24	Yes	Yes
32-pin (5 × 5 mm 0.60 Max) QFN (Sawn)	CY8C20424-12LQXI	8 K	512	25	1	28	Yes	Yes
32-pin (5 × 5 mm 0.60 Max) QFN (Sawn)	CY8C20424-12LQXIT	8 K	512	25	1	28	Yes	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

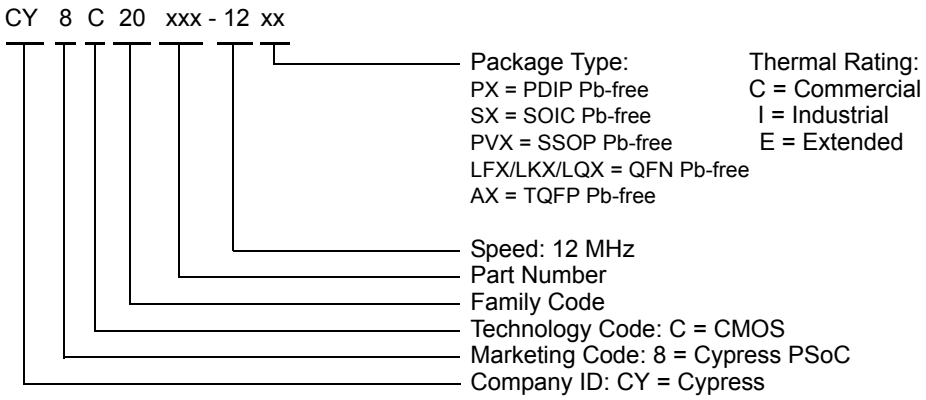
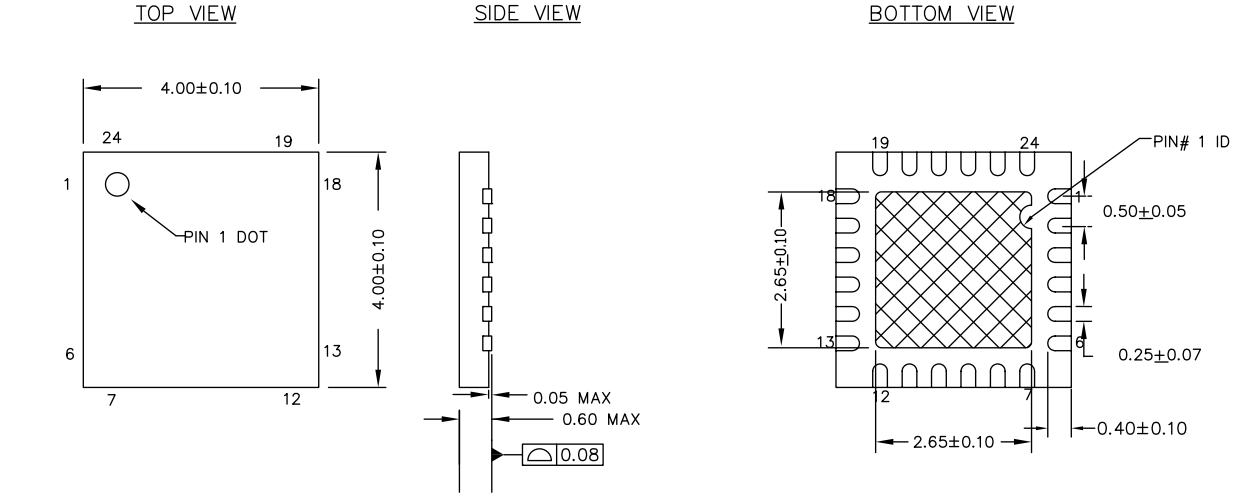


Figure 12. 24-pin QFN (4 × 4 × 0.55 mm) 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937

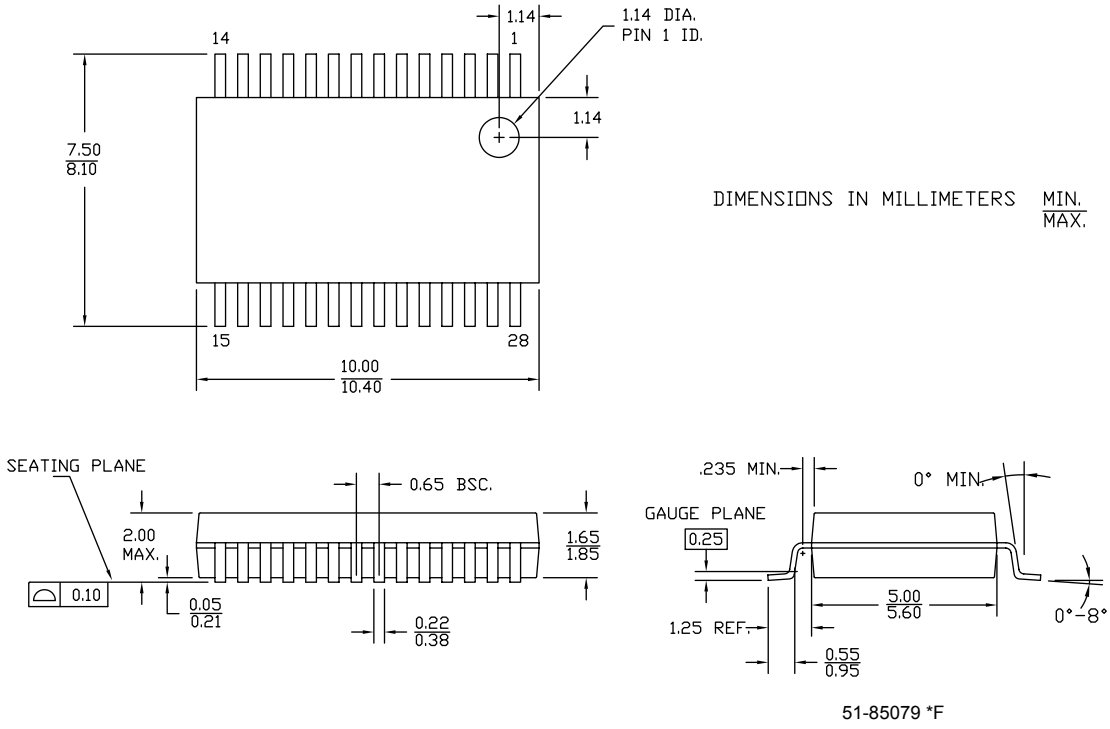


NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

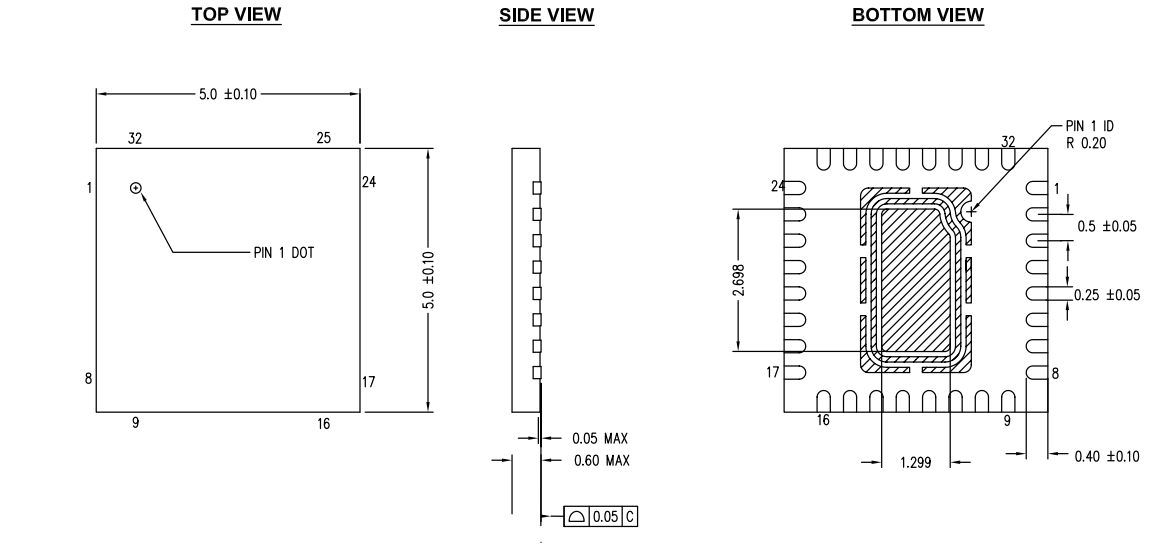
001-13937 *F

Figure 13. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *F

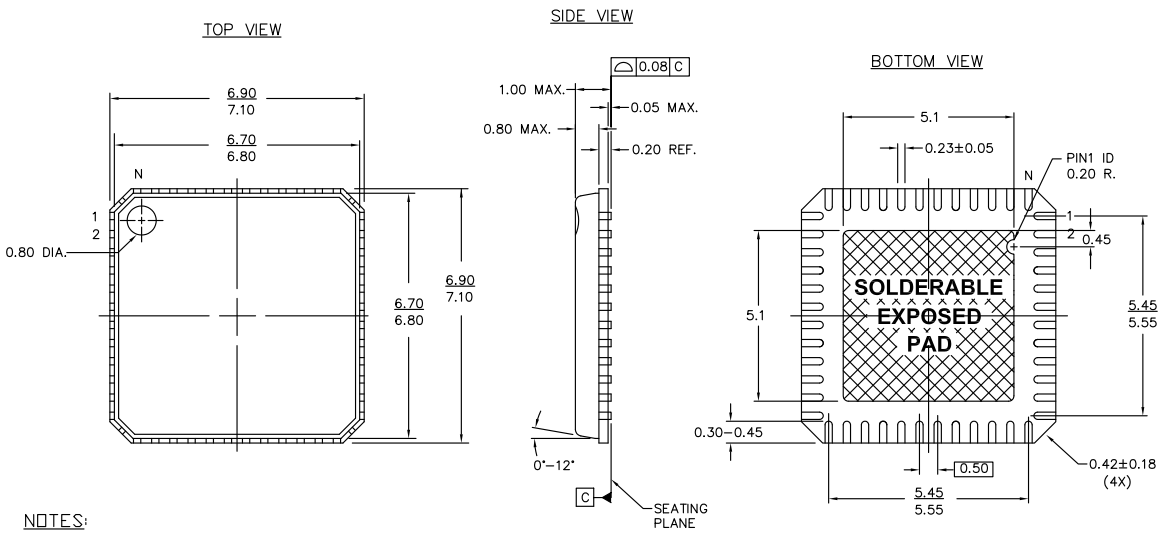
Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Figure 15. 48-pin QFN (7 × 7 × 1.0 mm) 5.1 × 5.1 E-Pad (Subcon Punch Type Package) Package Outline, 001-12919



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *D

Important For information on the preferred dimensions for mounting the QFN packages, see the following application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Document Conventions

Units of Measure

Table 35 lists the units of measures.

Table 35. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	ms	millisecond
pF	picofarad	ns	nanosecond
kHz	kilohertz	ps	picosecond
MHz	megahertz	µV	microvolts
kΩ	kilohm	mV	millivolts
Ω	ohm	V	volts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	%	percent
µs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary *(continued)*

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

Glossary *(continued)*

SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page *(continued)*

Document Title: CY8C20224/CY8C20324/CY8C20424/CY8C20524, CapSense® PSoC® Programmable System-on-Chip™ Document Number: 001-41947				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	3638597	BVI	06/06/2012	Updated Getting Started: Updated description. Updated Application Notes: Updated description. Updated Development Kits: Updated description. Updated Training: Updated description. Updated CYPros Consultants: Updated description. Updated Solutions Library: Updated description. Updated Technical Support: Updated description. Updated AC SPI Specifications: Updated Table 28: Renamed “t_{OUT_HIGH}” as “t_{OUT_H}” in “Symbol” column. Updated Table 29: Removed t_{SCLK} parameter and its details. Added F_{SCLK} parameter and its details. Updated Packaging Dimensions: spec 001-09116 – Changed revision from *E to *F. spec 001-13937 – Changed revision from *C to *D. spec 51-85079 – Changed revision from *D to *E. spec 001-12919 – Changed revision from *B to *C. Updated Solder Reflow Specifications: Updated Table 32: Replaced “Time at Maximum Temperature” with “Time at Maximum Peak Temperature” in column heading and updated details in that column. Updated Development Tool Selection: Updated Software: Updated PSoC Designer: Updated description. Updated PSoC Designer: Updated description. Updated Reference Documents: Removed spec 001-17397 and spec 001-14503 from the list as these specs are obsolete.
*M	4311264	VAIR	03/19/2014	Updated Designing with PSoC Designer: Updated Configure User Modules: Updated description (Replaced references of PWM User Module with EzI2Cs User Module). Updated Packaging Dimensions: spec 001-09116 – Changed revision from *F to *J. spec 001-13937 – Changed revision from *D to *E. spec 001-48913 – Changed revision from *B to *D. spec 001-12919 – Changed revision from *C to *D.
*N	5625819	DCHE	02/09/2017	Updated Packaging Dimensions: spec 001-13937 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

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