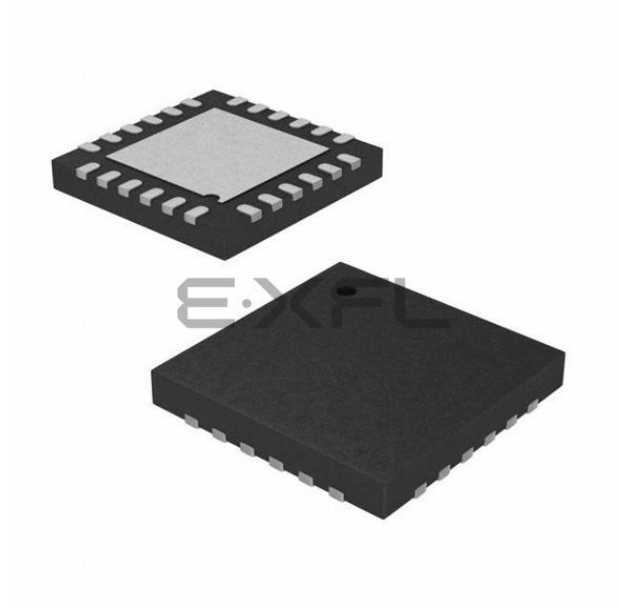

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	20
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20324-12lqxit

Contents

PSoC® Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip controller devices. These devices are designed to replace multiple traditional MCU based system components with one, low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture enables the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family is comprised of three main areas: core, system resources, and CapSense analog system. A common, versatile bus enables connection between I/O and the analog system. Each CY8C20x24 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a 2-MIPS, 8-bit Harvard-architecture microprocessor.

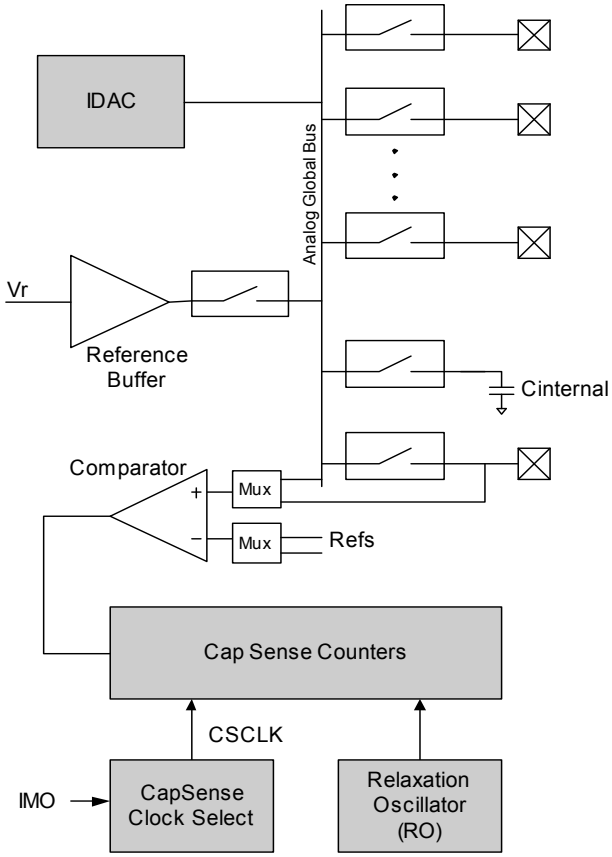
System resources provide additional capability, such as a configurable I^2C slave or SPI master-slave communication interface and various system resets supported by the M8C.

The analog system is composed of the CapSense PSoC block and an internal 1.8-V analog reference. Together, they support capacitive sensing of up to 28 inputs.

CapSense Analog System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The analog mux bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. The analog multiplexer system in the CY8C20x24 device family is optimized for basic CapSense functionality. It supports sensing of CapSense buttons, proximity sensors, and a single slider. Other multiplexer applications include:

- Capacitive slider interface.
- Chip-wide mux that enables analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

When designing capacitive sensing applications, refer to the latest signal to noise signal level requirements application notes, which are found in http://www.cypress.com > Design Resources > Application Notes. In general, and unless otherwise noted in the relevant application notes, the minimum signal-to-noise ratio (SNR) requirement for CapSense applications is 5:1.

28-pin Part Pinout

Figure 5. CY8C20524 28-pin PSoC Device

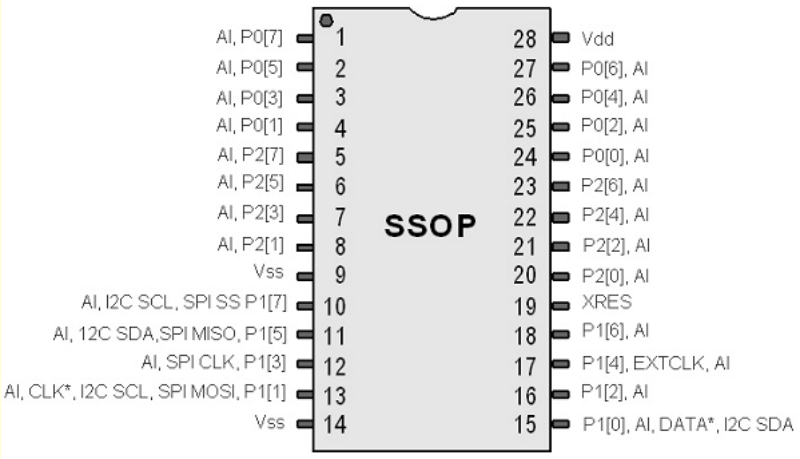


Table 3. 28-pin Part Pinout (SSOP)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	
2	I/O	I	P0[5]	
3	I/O	I	P0[3]	Integrating input
4	I/O	I	P0[1]	Integrating input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	
7	I/O	I	P2[3]	
8	I/O	I	P2[1]	
9	Power		V_{SS}	Ground connection
10	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
11	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
12	I_{OH}	I	P1[3]	SPI CLK
13	I_{OH}	I	P1[1]	CLK[4], I^2C SCL, SPL MOSI
14	Power		V_{SS}	Ground connection
15	I_{OH}	I	P1[0]	Data[4], I^2C SDA
16	I_{OH}	I	P1[2]	
17	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
18	I_{OH}	I	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	
28	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
4. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

32-pin Part Pinout

Figure 6. CY8C20424 32-pin PSoC Device

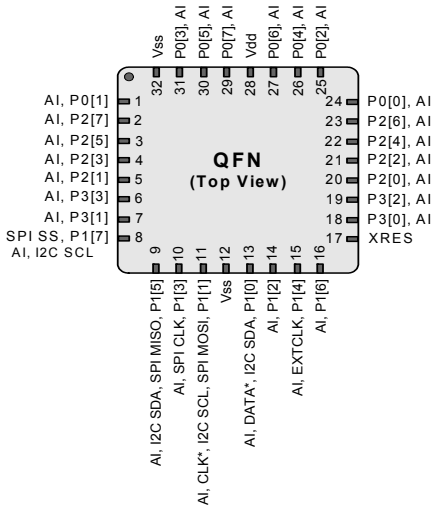


Table 4. 32-pin Part Pinout (QFN [5])

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[1]	Integrating Input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
9	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
10	I_{OH}	I	P1[3]	SPI CLK
11	I_{OH}	I	P1[1]	CLK[6], I^2C SCL, SPI MOSI
12	Power		V_{SS}	Ground connection
13	I_{OH}	I	P1[0]	DATA[6], I^2C SDA
14	I_{OH}	I	P1[2]	
15	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
16	I_{OH}	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down

Notes
5. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
6. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

DC Electrical Characteristics

DC Chip Level Specifications

Table 8 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 8. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz.
I_{SB27}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C.

DC GPIO Specifications

Unless otherwise noted, Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 9. 5 V and 3.3 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.
V_{OH7}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.1	2.4	2.7	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.0	–	–	V	I_{OH} < 200 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.6	1.8	2.0	V	I_{OH} < 10 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤ 85 °C, maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.5	–	–	V	I_{OH} < 100 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ TA ≤ 85 °C, maximum of 20 mA source current in all I/Os.

Table 9. 5 V and 3.3 V DC GPIO Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA, V_{DD} > 3.0V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current, port 0, 2, or 3 pins	1	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OH4}	High level source current, port 1 pins with LDO regulator disabled	5	–	–	mA	$V_{OH} = V_{DD} – 0.9$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	20	–	–	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low voltage	–	–	0.8	V	3.0 V ≤ V_{DD} ≤ 5.25 V
V_{IH}	Input high voltage	2.0	–		V	3.0 V ≤ V_{DD} ≤ 5.25 V
V_H	Input hysteresis voltage	–	140	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C

Table 10. 2.7 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage, port 1 pins with LDO regulator disabled	$V_{DD} – 0.2$	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage, port 1 pins with LDO regulator disabled	$V_{DD} – 0.5$	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current, port 1 pins with LDO regulator disabled	2	–	–	mA	$V_{OH} = V_{DD} – 0.5$, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	10	–	–	mA	V_{OH} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	IOL = 5 mA, maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V ≤ V_{DD} ≤ 3.0 V
V_{IL}	Input low voltage	–	–	0.75	V	2.4 V ≤ V_{DD} ≤ 3.0 V
V_{IH1}	Input high voltage	1.4	–	–	V	2.4 V ≤ V_{DD} ≤ 2.7 V
V_{IH2}	Input high voltage	1.6	–	–	V	2.7 V ≤ V_{DD} ≤ 3.0 V
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA

Table 10. 2.7 V DC GPIO Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent temperature = 25 °C

DC Analog Mux Bus Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 11. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	Vdd ≥ 2.7 V 2.4 V ≤ Vdd ≤ 2.7 V

DC Low Power Comparator Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 12. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1.0	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC POR and LVD Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 13. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
VPPOR0	PORLEV[1:0] = 00b	–	2.36	2.40	V	
VPPOR1	PORLEV[1:0] = 01b	–	2.60	2.65	V	
VPPOR2	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
VLVD0	VM[2:0] = 000b	2.39	2.45	2.51[9]	V	
VLVD1	VM[2:0] = 001b	2.54	2.71	2.78[10]	V	
VLVD2	VM[2:0] = 010b	2.75	2.92	2.99[11]	V	
VLVD3	VM[2:0] = 011b	2.85	3.02	3.09	V	
VLVD4	VM[2:0] = 100b	2.96	3.13	3.20	V	
VLVD5	VM[2:0] = 101b	–	–	–	V	
VLVD6	VM[2:0] = 110b	–	–	–	V	
VLVD7	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
9. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
10. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
11. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 14. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[12]	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[13]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 15. DC I^2C Specifications[14]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

Notes
12. The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.
13. A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
14. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

AC Electrical Characteristics

AC Chip Level Specifications

Table 16 and Table 17 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency (3.3 V nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (Commercial temperature)[15]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F_{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{RAMP}	Supply ramp time	0	–	–	µs	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[16]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Notes
15. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
16. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.

Table 24. 2.7 V AC External Clock Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{OSCEXT2B}$	Frequency with CPU clock divide by 2 or greater (2.7 V minimum)	1.5	–	12.6	MHz	2.7 V < V_{DD} < 3.0 V. If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

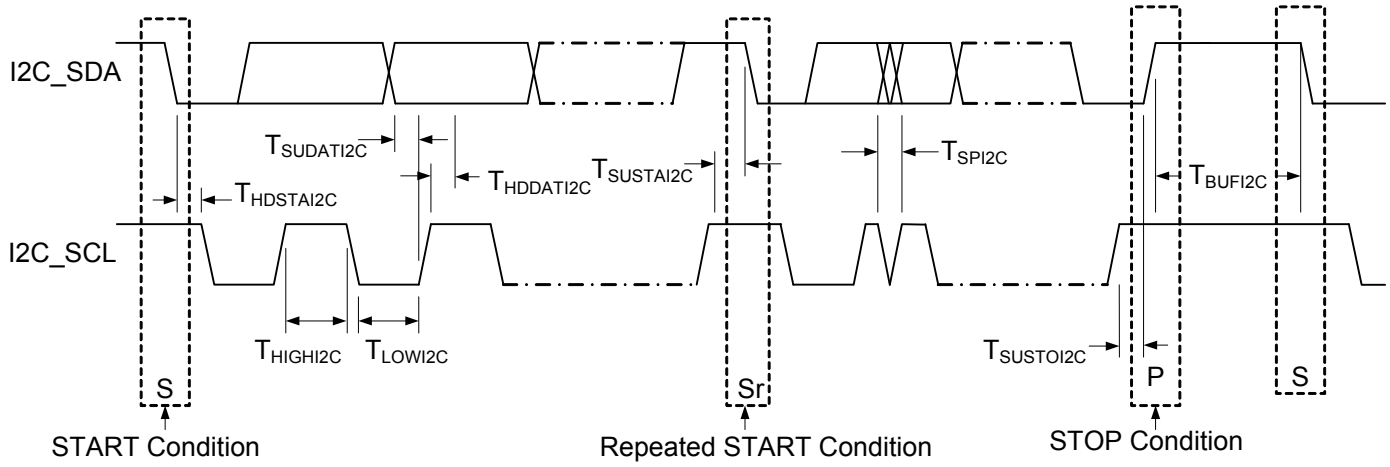
AC Programming Specifications

Table 25 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 25. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (Block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	40	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	3.6 < V_{DD}
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0
$t_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200	ms	–40 °C ≤ Tj ≤ 0 °C

Figure 10. Definition for Timing for Fast or Standard Mode on the I²C Bus



AC SPI Specifications

Table 28. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	12	MHz
DC	SCLK duty cycle		–	50	–	%
t_{SETUP}	MISO to SCLK setup time		40	–	–	ns
t_{HOLD}	SCLK to MISO hold time		40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
t_{OUT_H}	MOSI high time		40	–	–	ns

Table 29. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	4	MHz
t_{LOW}	SCLK low time		41.67	–	–	ns
t_{HIGH}	SCLK high time		41.67	–	–	ns
t_{SETUP}	MOSI to SCLK setup time		30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time		50	–	–	ns
t_{SS_MISO}	SS high to MISO valid		–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid		–	–	125	ns
t_{SS_HIGH}	SS high time		–	–	50	ns
t_{SS_CLK}	Time from SS low to first SCLK		2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high		2/SCLK	–	–	ns

Ordering Information

Table 30 lists the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC devices key package features and ordering codes.

Table 30. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Maximum Number of Buttons	Maximum Number of Sliders	Maximum Number of LEDs	Configurable LED Behavior (Fade, Strobe)	Proximity Sensing
16-pin (3 × 3 mm 0.60 Max) COL	CY8C20224-12LKXI	8 K	512	10	1	13	Yes	Yes
16-pin (3 × 3 mm 0.60 Max) COL (Tape and Reel)	CY8C20224-12LKXIT	8 K	512	10	1	13	Yes	Yes
24-pin (4 × 4 mm 0.60 Max) QFN	CY8C20324-12LQXI	8 K	512	17	1	20	Yes	Yes
24-pin (4 × 4 mm 0.60 Max) QFN (Tape and Reel)	CY8C20324-12LQXIT	8 K	512	17	1	20	Yes	Yes
28-pin (210-Mil) SSOP	CY8C20524-12PVXI	8 K	512	21	1	24	Yes	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C20524-12PVXIT	8 K	512	21	1	24	Yes	Yes
32-pin (5 × 5 mm 0.60 Max) QFN (Sawn)	CY8C20424-12LQXI	8 K	512	25	1	28	Yes	Yes
32-pin (5 × 5 mm 0.60 Max) QFN (Sawn)	CY8C20424-12LQXIT	8 K	512	25	1	28	Yes	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

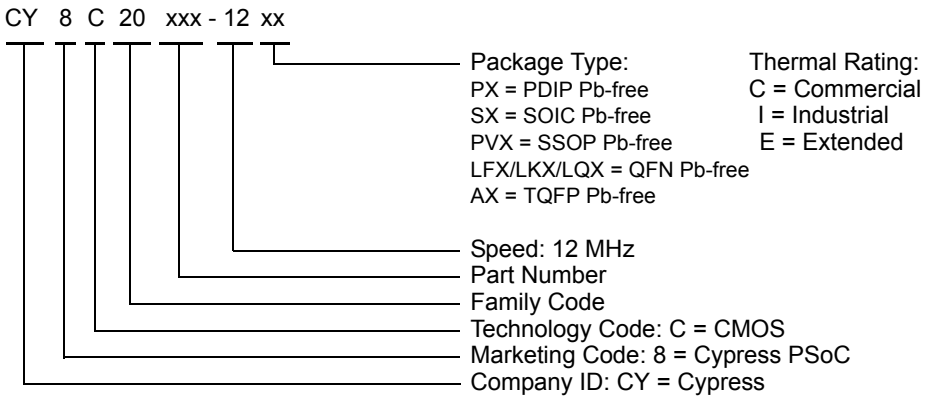
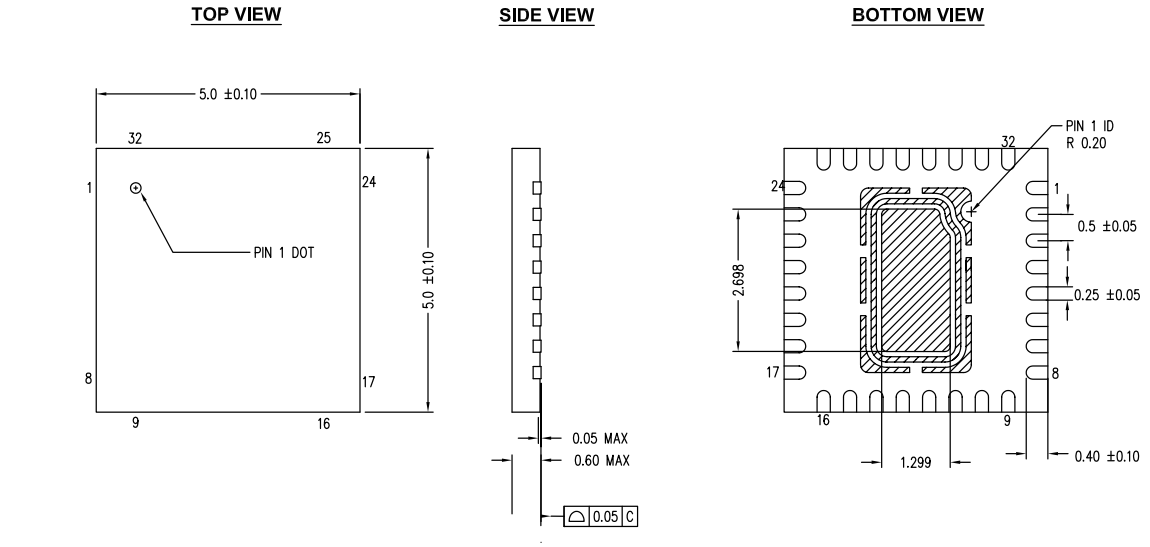


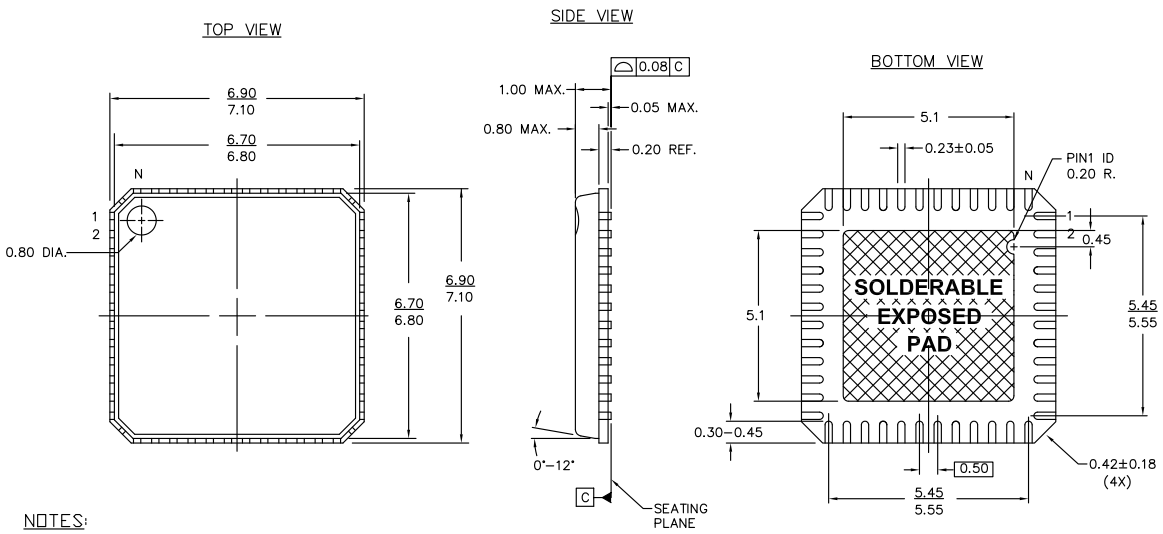
Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Figure 15. 48-pin QFN (7 × 7 × 1.0 mm) 5.1 × 5.1 E-Pad (Subcon Punch Type Package) Package Outline, 001-12919



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *D

Important For information on the preferred dimensions for mounting the QFN packages, see the following application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Thermal Impedances

Table 31. Thermal Impedances Per Package

Package	Typical θ_{JA} [20]
16-pin COL	46 °C/W
24-pin QFN[21]	25 °C/W
28-pin SSOP	96 °C/W
32-pin QFN[21]	27 °C/W
48-pin QFN[21]	28 °C/W

Solder Reflow Specifications

Table 32 lists the minimum solder reflow peak temperature to achieve good solderability.

Table 32. Solder Reflow Specifications

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
16-pin COL	260 °C	30 s
24-pin QFN	260 °C	30 s
28-pin SSOP	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

Notes
20. $T_J = T_A$ + Power x θ_{JA}.
21. To achieve the thermal impedance specified for the QFN package, the center thermal pad is soldered to the PCB ground plane.

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 33. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit [22]	Foot Kit [23]	Prototyping Module	Adapter [24]
CY8C20224-12LKXI	16-pin COL	Not available	Not available	CY3210-20X34	–
CY8C20324-12LQXI	24-pin QFN	CY3250-20334QFN	CY3250-24QFN-FK	CY3210-20X34	AS-24-28-01ML-6
CY8C20524-12PVXI	28-pin SSOP	CY3250-20534	CY3250-28SSOP-FK	CY3210-20X34	–

Third Party Tools

Several tools are specially designed by the following third party vendors to accompany PSoC devices during development and production. Specific details of each of these tools are found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on emulating the circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer application note AN2323 “Build a PSoC Emulator into Your Board”.

Notes
22. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
23. Foot kit includes surface mount feet that is soldered to the target PCB.
24. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is found at http://www.emulation.com.

Glossary *(continued)*

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.

Glossary *(continued)*

External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

Glossary *(continued)*

SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C20224/CY8C20324/CY8C20424/CY8C20524, CapSense® PSoC® Programmable System-on-Chip™ Document Number: 001-41947				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1734104	YHW / AESA	See ECN	New parts and document (Revision **).
*A	2542938	RLRM / AESA	07/28/2008	Corrected Ordering Information format. Updated package diagram 001-13937 to Rev *B. Updated to new template.
*B	2610469	SNV / PYRS	11/20/08	Updated V_{OH5}, V_{OH7}, and V_{OH9} specifications.
*C	2634376	DRSW	01/12/09	Changed status from Preliminary to Final. Removed the part number CY3250-20234QFN from the 'CY8C20224-12LKXI' flex-pod kit Changed title from CapSense™ Multimedia PSoC® Mixed-Signal Array to CapSense™ Multimedia PSoC® Programmable System-on-Chip™ Added -12 to the CY8C20524 parts in the Ordering Information table Updated 'Development Tools' and 'Designing with PSoC Designer' sections on pages 4 and 5 Updated 'Development Tools Selection' section on page 30 Changed 16-Pin from QFN to COL
*D	2693024	DPT / PYRS	04/16/2009	Added devices CY8C20424-12LQXI and CY8C20424-12LQXIT in the Ordering Information table Added 32-Pin Sawn QFN package diagram
*E	2717566	DRSW / AESA	06/11/2009	Updated AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 (page 19), TWRITE specifications (page 22) Added IOH & IOL (page 16), Flash endurance note (page 18), DCILO (page 19), F32K_U (page 19), TPOWERUP (page 19), TERASEALL (page 22), TPROGRAM_HOT (page 22), and TPROGRAM_COLD (page 22) specifications Added AC SPI Master and Slave Specifications
*F	2899195	CFW / ISW	03/26/2010	Updated Ordering Information. Updated Package Diagrams.
*G	3037121	CFW	09/24/2010	Updated title to read AC Comparator Specifications and also updated table caption to read "AC Comparator Specifications" in the same section. Minor edits. Updated to new template.
*H	3049675	BTK	10/06/2010	Removed AC analog mux bus specifications. Updated Development Tools and Designing with PSoC Designer sections.
*I	3072668	NJF	10/27/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changed were made to I^2C Timing Diagram. Updated for clearer understanding. Updated to new template.
*J	3112469	ARVM	12/16/10	Updated Ordering Information: Updated part numbers.
*K	3182773	MATT	03/01/11	No technical updates. Completing Sunset Review.

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