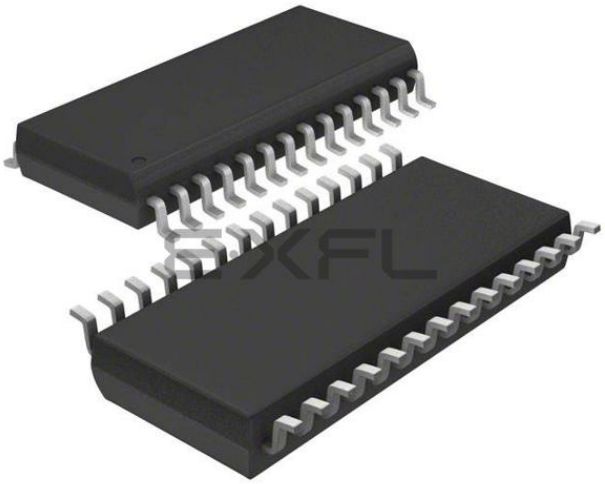

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20524-12pvxit

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, an EzI2Cs User Module configures the I^2C block in PSoC. Using these parameters, you can establish the slave address and I^2C speed. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module data sheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals

Pinouts

This section describes, lists, and illustrates the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC device pins and pinout configurations.

The CY8C20x24 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

16-pin Part Pinout

Figure 3. CY8C20224 16-pin PSoC Device

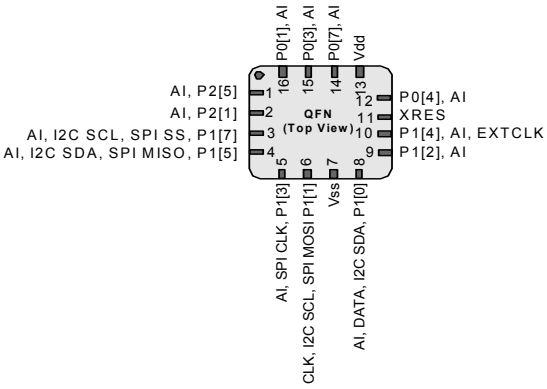


Table 1. 16-pin Part Pinout (COL)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
5	I_{OH}	I	P1[3]	SPI CLK
6	I_{OH}	I	P1[1]	CLK[1], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	I_{OH}	I	P1[0]	DATA[1], I^2C SDA
9	I_{OH}	I	P1[2]	
10	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating input
16	I/O	I	P0[1]	Integrating input

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
1. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

32-pin Part Pinout

Figure 6. CY8C20424 32-pin PSoC Device

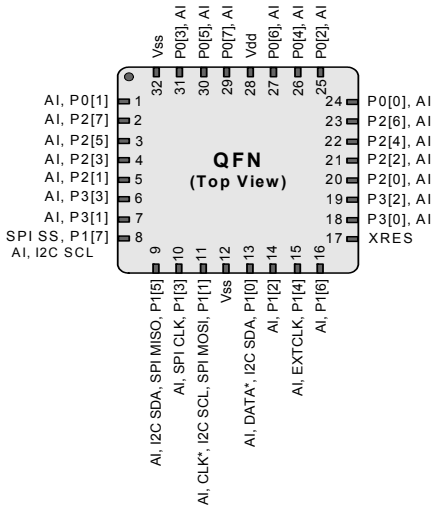


Table 4. 32-pin Part Pinout (QFN [5])

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[1]	Integrating Input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
9	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
10	I_{OH}	I	P1[3]	SPI CLK
11	I_{OH}	I	P1[1]	CLK[6], I^2C SCL, SPI MOSI
12	Power		V_{SS}	Ground connection
13	I_{OH}	I	P1[0]	DATA[6], I^2C SDA
14	I_{OH}	I	P1[2]	
15	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
16	I_{OH}	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down

Notes
5. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
6. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

48-pin OCD Part Pinout

The 48-pin QFN part table and pin diagram is for the CY8C20024 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. **It is NOT available for production**.

Figure 7. CY8C20024 OCD PSoC Device

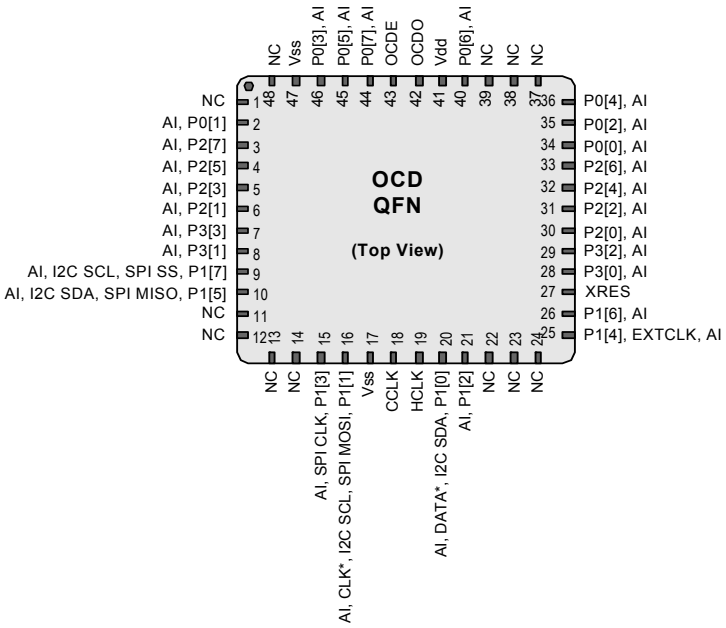


Table 5. 48-pin OCD Part Pinout (QFN [7])

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P0[1]	Integrating Input
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
10	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
11			NC	No connection
12			NC	No connection
13			NC	No connection
14			NC	No connection
15	I_{OH}	I	P1[3]	SPI CLK
16	I_{OH}	I	P1[1]	CLK[8], I^2C SCL, SPI MOSI
17	Power		Vss	Ground connection
18			CCLK	OCD CPU clock output
19			HCLK	OCD high speed clock output
20	I_{OH}	I	P1[0]	DATA[8], I^2C SDA

Notes

7. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
8. These are the ISSP pins, that are not high Z at POR (Power on reset). Refer the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

DC Electrical Characteristics

DC Chip Level Specifications

Table 8 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 8. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz.
I_{SB27}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C.

DC GPIO Specifications

Unless otherwise noted, Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 9. 5 V and 3.3 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage, port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage, port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage, port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.
V_{OH7}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.1	2.4	2.7	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage, port 1 pins with 2.4 V LDO regulator enabled	2.0	–	–	V	I_{OH} < 200 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.6	1.8	2.0	V	I_{OH} < 10 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤ 85 °C, maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage, port 1 pins with 1.8 V LDO regulator enabled	1.5	–	–	V	I_{OH} < 100 µA, 3.0 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ TA ≤ 85 °C, maximum of 20 mA source current in all I/Os.

AC Electrical Characteristics

AC Chip Level Specifications

Table 16 and Table 17 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency (3.3 V nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (Commercial temperature)[15]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F_{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{RAMP}	Supply ramp time	0	–	–	µs	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[16]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Notes
15. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
16. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.

Table 17. 2.7 V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1A}	CPU frequency (2.7 V nominal)	0.75	–	3.25	MHz	2.4 V < V_{DD} < 3.0 V.
F_{CPU1B}	CPU frequency (2.7 V minimum)	0.75	–	6.3	MHz	2.7 V < V_{DD} < 3.0 V.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	–	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (Commercial temperature)[17]	11.0	12	12.9	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 0.
F_{IMO6}	IMO stability for 6 MHz (Commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 14, SLIMO Mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{RAMP}	Supply ramp time	0	–	–	µs	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$		–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[18]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	500	900	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	800	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	300	500	ps	

Notes
17. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
18. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products - AN5054 for more information.

AC GPIO Specifications

Table 18 an d Table 19 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

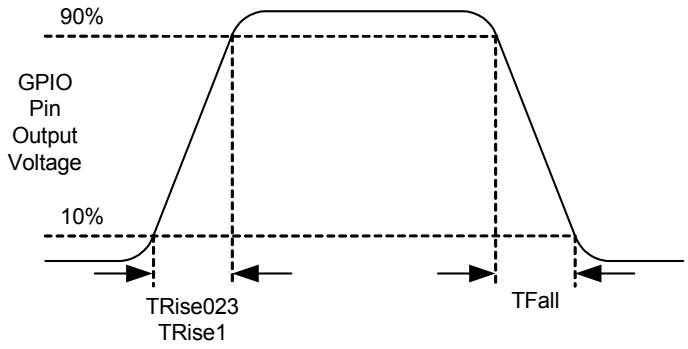
Table 18. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	6	MHz	Normal strong mode, Port 1.
$t_{Rise023}$	Rise time, strong mode, Cload = 50 pF, ports 0, 2, 3	15	–	80	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, port 1	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF, all ports	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%

Table 19. 2.7 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	1.5	MHz	Normal Strong Mode, Port 1.
$t_{Rise023}$	Rise time, strong mode, Cload = 50 pF, ports 0, 2, 3	15	–	100	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, port 1	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF, all ports	10	–	70	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%

Figure 9. GPIO Timing Diagram



AC Comparator Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 20. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator response time, 50 mV overdrive	–	–	100 200	ns ns	V_{DD} ≥ 3.0 V 2.4 V < V_{CC} < 3.0 V

Table 24. 2.7 V AC External Clock Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{OSCEXT2B}$	Frequency with CPU clock divide by 2 or greater (2.7 V minimum)	1.5	–	12.6	MHz	2.7 V < V_{DD} < 3.0 V. If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 25 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 25. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (Block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	40	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	3.6 < V_{DD}
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0
$t_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200	ms	–40 °C ≤ Tj ≤ 0 °C

AC I²C Specifications

Table 26 and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 26. AC Characteristics of the I²C SDA and SCL Pins for V_{DD} ≥ 3.0 V

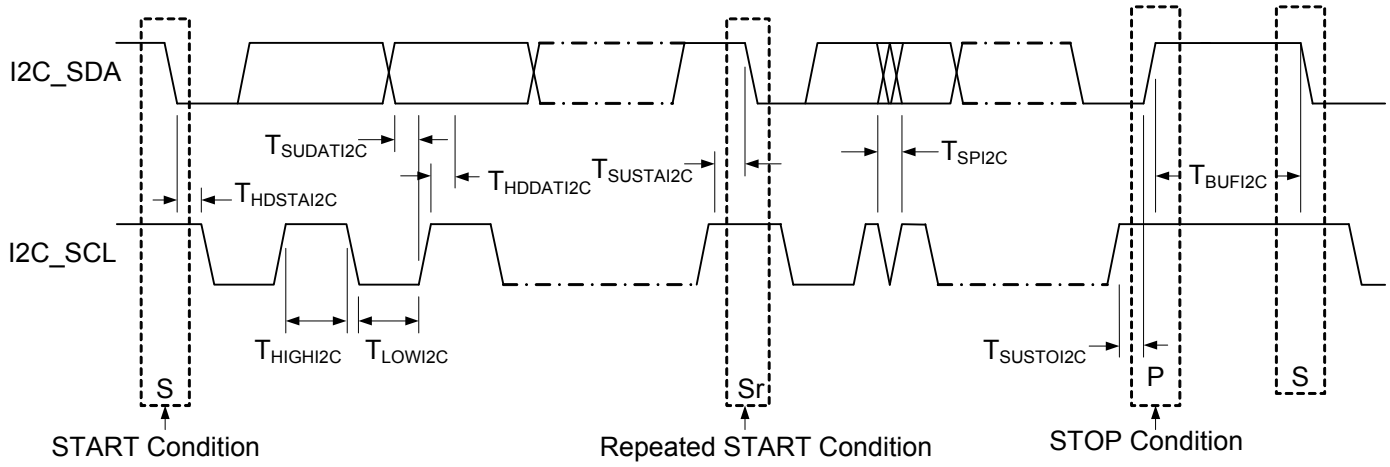
Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	100[19]	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns	

Table 27. 2.7 V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not supported)

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	–	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	–	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	–	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	–	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	–	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	–	–	µs	
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns	

Note
19. A Fast Mode I²C bus device is used in a Standard Mode I²C bus system but the requirement T_{SUDAT} ≥ 250 ns is met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + T_{SUDAT} = 1000 + 250 = 1250 ns (according to the Standard Mode I²C bus specification) before the SCL line is released.

Figure 10. Definition for Timing for Fast or Standard Mode on the I²C Bus



AC SPI Specifications

Table 28. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	12	MHz
DC	SCLK duty cycle		–	50	–	%
t_{SETUP}	MISO to SCLK setup time		40	–	–	ns
t_{HOLD}	SCLK to MISO hold time		40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time		–	–	40	ns
t_{OUT_H}	MOSI high time		40	–	–	ns

Table 29. SPI Slave AC Specifications

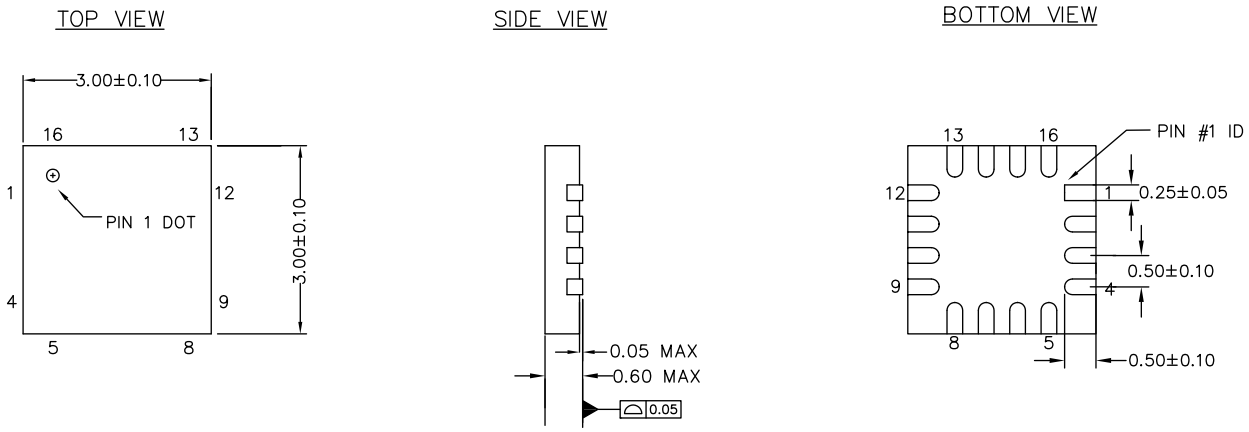
Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency		–	–	4	MHz
t_{LOW}	SCLK low time		41.67	–	–	ns
t_{HIGH}	SCLK high time		41.67	–	–	ns
t_{SETUP}	MOSI to SCLK setup time		30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time		50	–	–	ns
t_{SS_MISO}	SS high to MISO valid		–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid		–	–	125	ns
t_{SS_HIGH}	SS high time		–	–	50	ns
t_{SS_CLK}	Time from SS low to first SCLK		2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high		2/SCLK	–	–	ns

Packaging Dimensions

This section illustrates the packaging specifications for the CY8C20224, CY8C20324, CY8C20424, and CY8C20524 PSoC devices, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

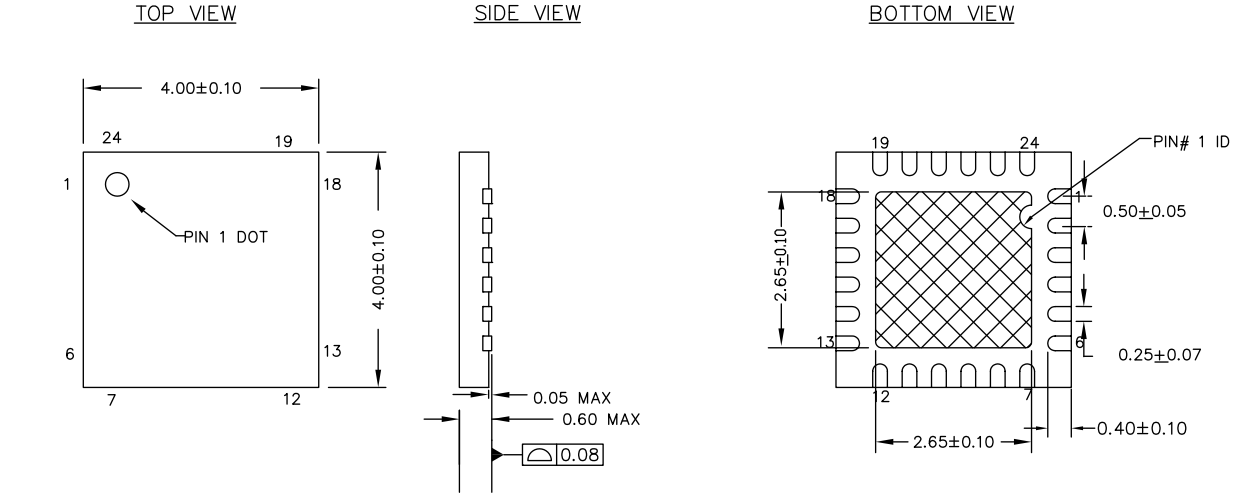
Figure 11. 16-pin Chip On-Lead (3 × 3 × 0.6 mm) (Sawn) Package Outline, 001-09116



NOTES
1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Figure 12. 24-pin QFN (4 × 4 × 0.55 mm) 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937

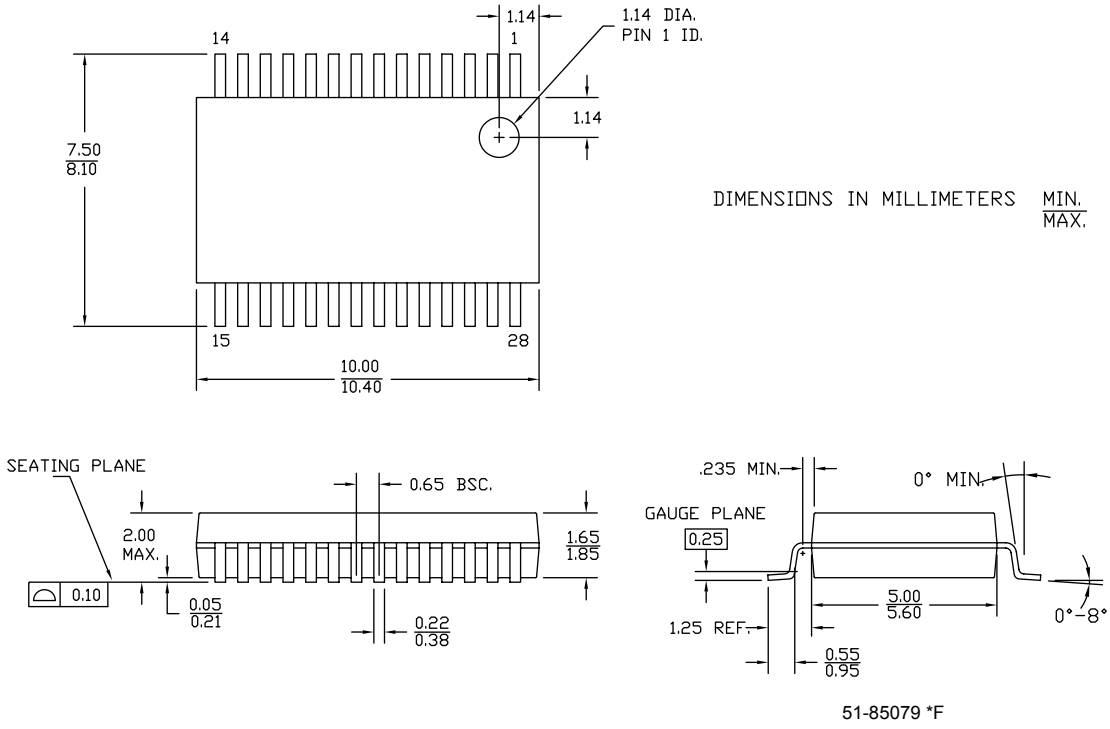


NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

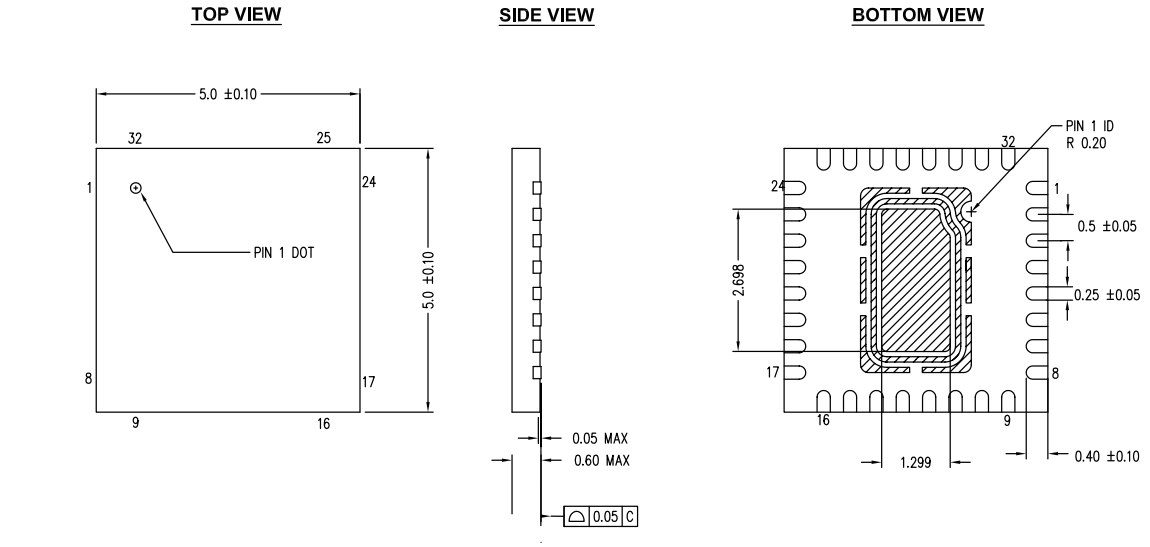
001-13937 *F

Figure 13. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *F

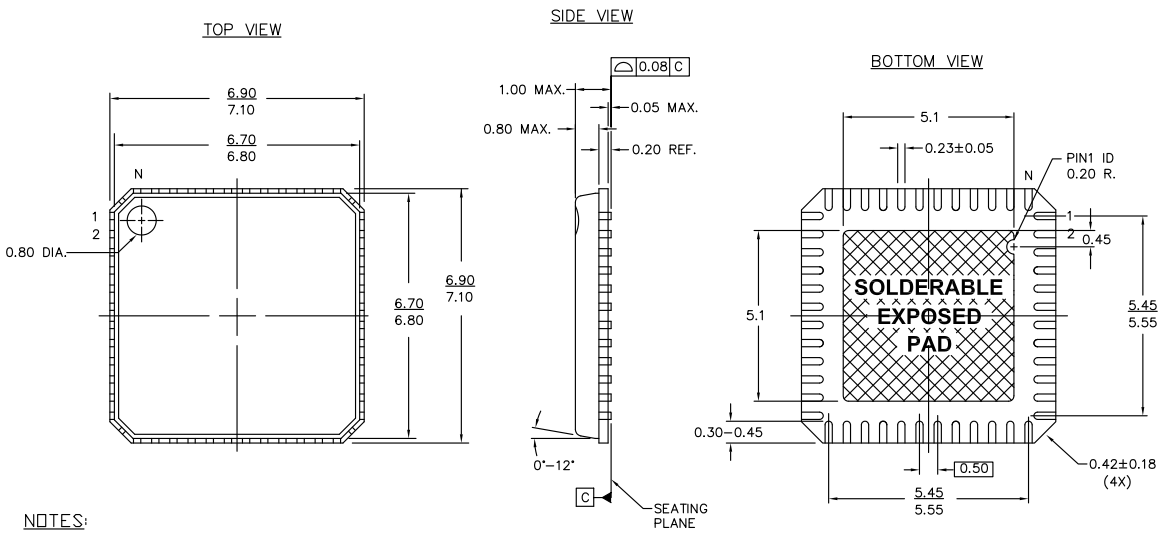
Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Figure 15. 48-pin QFN (7 × 7 × 1.0 mm) 5.1 × 5.1 E-Pad (Subcon Punch Type Package) Package Outline, 001-12919



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *D

Important For information on the preferred dimensions for mounting the QFN packages, see the following application note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Thermal Impedances

Table 31. Thermal Impedances Per Package

Package	Typical θ_{JA} [20]
16-pin COL	46 °C/W
24-pin QFN[21]	25 °C/W
28-pin SSOP	96 °C/W
32-pin QFN[21]	27 °C/W
48-pin QFN[21]	28 °C/W

Solder Reflow Specifications

Table 32 lists the minimum solder reflow peak temperature to achieve good solderability.

Table 32. Solder Reflow Specifications

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
16-pin COL	260 °C	30 s
24-pin QFN	260 °C	30 s
28-pin SSOP	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

Notes
20. $T_J = T_A$ + Power x θ_{JA}.
21. To achieve the thermal impedance specified for the QFN package, the center thermal pad is soldered to the PCB ground plane.

Acronyms

Acronyms Used

Table 34 lists the acronyms that are used in this document.

Table 34. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PGA	programmable gain amplifier
CPU	central processing unit	POR	power on reset
EEPROM	electrically erasable programmable read-only memory	PPOR	precision power on reset
GPIO	general purpose I/O	PSoC®	Programmable System-on-Chip
ICE	in-circuit emulator	PWM	pulse width modulator
IDAC	current DAC	QFN	quad flat no leads
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SPI™	serial peripheral interface
IMO	internal main oscillator	SRAM	static random access memory
I/O	input/output	SROM	supervisory read only memory
ISSP	in-system serial programming	SSOP	shrink small-outline package
LCD	liquid crystal display	USB	universal serial bus
LDO		WDT	watchdog timer
LED	light-emitting diode	WLCSP	wafer level chip scale package
LVD	low voltage detect	XRES	external reset
MCU	microcontroller unit		

Reference Documents

PSoC® CY8C20x34 and PSoC® CY8C20x24 Technical Reference Manual (TRM) – 001-13033

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Glossary *(continued)*

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.

Glossary *(continued)*

SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page *(continued)*

Document Title: CY8C20224/CY8C20324/CY8C20424/CY8C20524, CapSense® PSoC® Programmable System-on-Chip™ Document Number: 001-41947				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	3638597	BVI	06/06/2012	Updated Getting Started: Updated description. Updated Application Notes: Updated description. Updated Development Kits: Updated description. Updated Training: Updated description. Updated CYPros Consultants: Updated description. Updated Solutions Library: Updated description. Updated Technical Support: Updated description. Updated AC SPI Specifications: Updated Table 28: Renamed “t_{OUT_HIGH}” as “t_{OUT_H}” in “Symbol” column. Updated Table 29: Removed t_{SCLK} parameter and its details. Added F_{SCLK} parameter and its details. Updated Packaging Dimensions: spec 001-09116 – Changed revision from *E to *F. spec 001-13937 – Changed revision from *C to *D. spec 51-85079 – Changed revision from *D to *E. spec 001-12919 – Changed revision from *B to *C. Updated Solder Reflow Specifications: Updated Table 32: Replaced “Time at Maximum Temperature” with “Time at Maximum Peak Temperature” in column heading and updated details in that column. Updated Development Tool Selection: Updated Software: Updated PSoC Designer: Updated description. Updated PSoC Designer: Updated description. Updated Reference Documents: Removed spec 001-17397 and spec 001-14503 from the list as these specs are obsolete.
*M	4311264	VAIR	03/19/2014	Updated Designing with PSoC Designer: Updated Configure User Modules: Updated description (Replaced references of PWM User Module with EzI2Cs User Module). Updated Packaging Dimensions: spec 001-09116 – Changed revision from *F to *J. spec 001-13937 – Changed revision from *D to *E. spec 001-48913 – Changed revision from *B to *D. spec 001-12919 – Changed revision from *C to *D.
*N	5625819	DCHE	02/09/2017	Updated Packaging Dimensions: spec 001-13937 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

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