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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

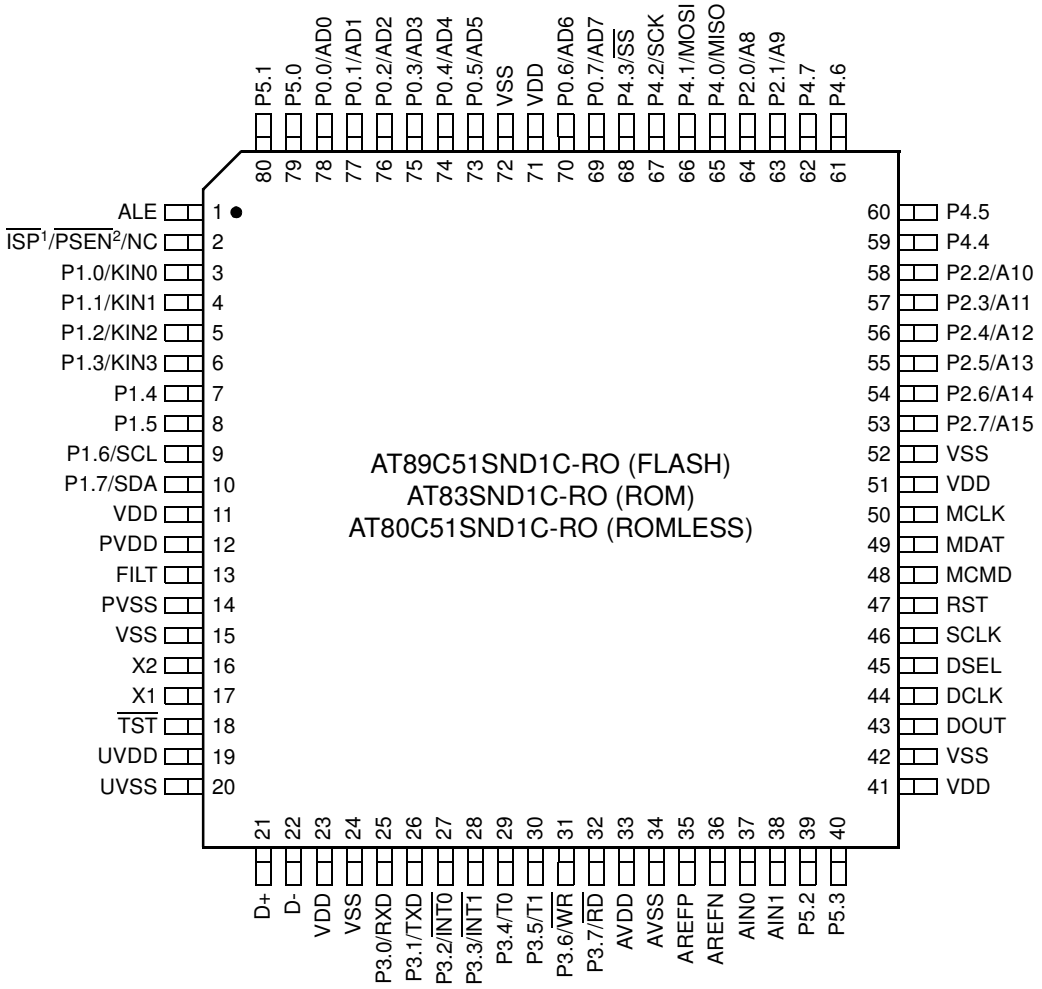
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IDE/ATAPI, Memory Card, SPI, UART/USART, USB
Peripherals	Audio, I²S, MP3, PCM, POR, WDT
Number of I/O	44
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at80c51snd1c-rotil

4. Pin Description

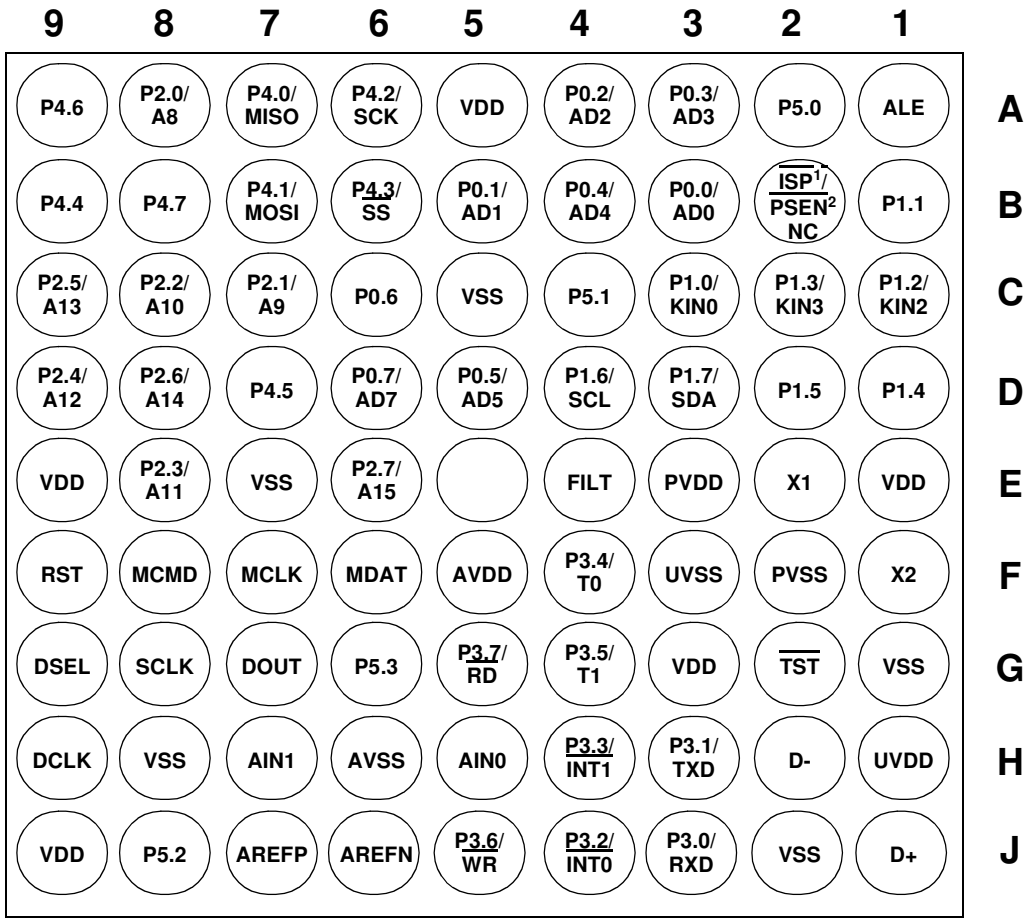
4.1 Pinouts

Figure 4-1. AT8xC51SND1C 80-pin QFP Package



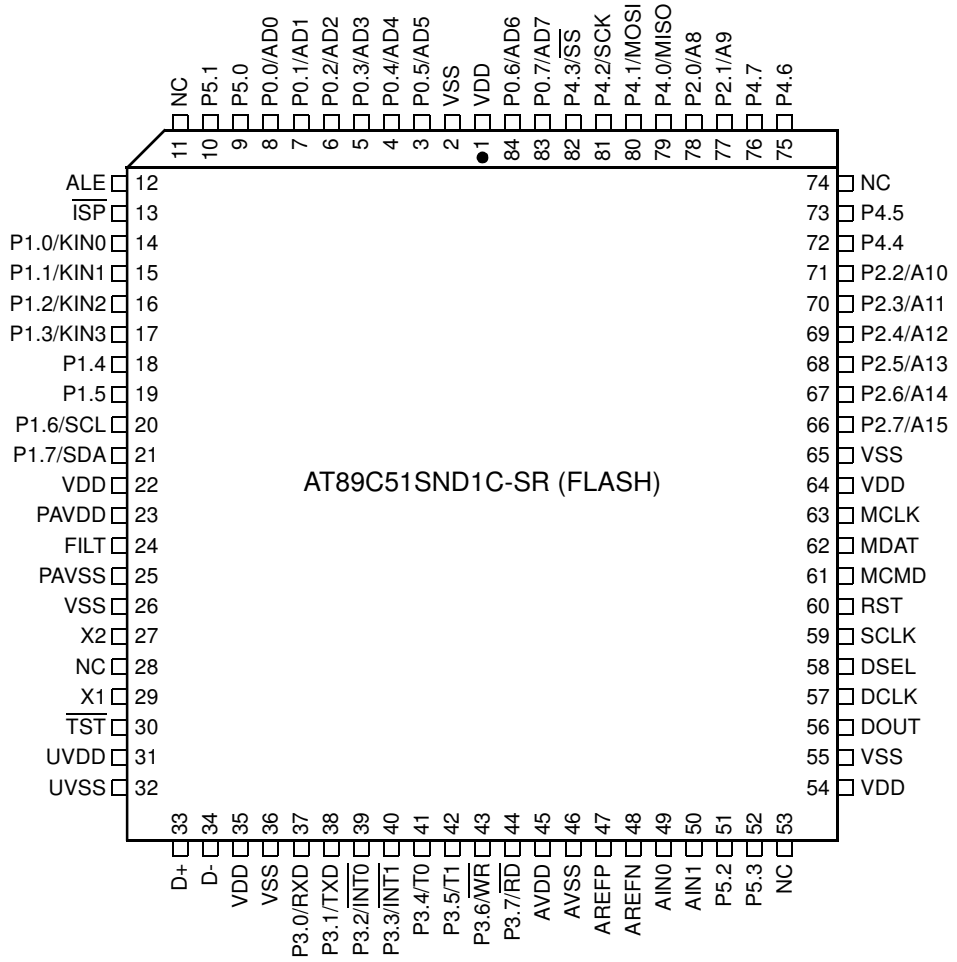
Notes: 1. ISP pin is only available in AT89C51SND1C product.
Do not connect this pin on AT83SND1C product.
2. PSEN pin is only available in AT80C51SND1C product.

Figure 4-2. AT8xC51SND1C 81-pin BGA Package



Notes: 1. $\overline{\text{ISP}}$ pin is only available in AT89C51SND1C product.
Do not connect this pin on AT83SND1C and AT80C51SND1C product.
2. $\overline{\text{PSEN}}$ pin is only available in AT80C51SND1C product.

Figure 4-3. AT8xC51SND1C 84-pin PLCC Package



4.2 Signals

All the AT8xC51SND1C signals are detailed by functionality in Table 1 to Table 14.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN3:0 SCL SDA
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8

Table 11. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 12. External Access Signal Description

Signal Name	Type	Description	Alternate Function
A15:8	I/O	**Address Lines** Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	**Address/Data Lines** Multiplexed lower address and data lines for the external memory or the IDE interface.	P0.7:0
ALE	O	**Address Latch Enable Output** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus.	-
$\overline{PSEN}$	I/O	**Program Store Enable Output (AT80C51SND1C Only)** This signal is active low during external code fetch or external code read (MOVC instruction).	-
$\overline{ISP}$	I/O	**ISP Enable Input (AT89C51SND1C Only)** This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.	-
$\overline{RD}$	O	**Read Signal** Read signal asserted during external data memory read operation.	P3.7
$\overline{WR}$	O	**Write Signal** Write signal asserted during external data memory write operation.	P3.6
$\overline{EA}^{(1)(2)}$	I	**External Access Enable (Dice Only)** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000h to FFFFh.	-

Notes: 1. For ROM/Flash Dice product versions: pad $\overline{EA}$ must be connected to VCC.
2. For ROMless Dice product versions: pad $\overline{EA}$ must be connected to VSS.

Table 13. System Signal Description

Signal Name	Type	Description	Alternate Function
RST	I	**Reset Input** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and V_{DD}. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	-
$\overline{TST}$	I	**Test Input** Test mode entry signal. This pin must be set to V_{DD}.	-

Table 14. Power Signal Description

Signal Name	Type	Description	Alternate Function
VDD	PWR	**Digital Supply Voltage** Connect these pins to +3V supply voltage.	-
VSS	GND	**Circuit Ground** Connect these pins to ground.	-
AVDD	PWR	**Analog Supply Voltage** Connect this pin to +3V supply voltage.	-
AVSS	GND	**Analog Ground** Connect this pin to ground.	-
PVDD	PWR	**PLL Supply voltage** Connect this pin to +3V supply voltage.	-
PVSS	GND	**PLL Circuit Ground** Connect this pin to ground.	-
UVDD	PWR	**USB Supply Voltage** Connect this pin to +3V supply voltage.	-
UVSS	GND	**USB Ground** Connect this pin to ground.	-

5. Application Information

Figure 5-1. AT8xC51SND1C Typical Application with On-Board Atmel DataFlash and 2-wire LCD

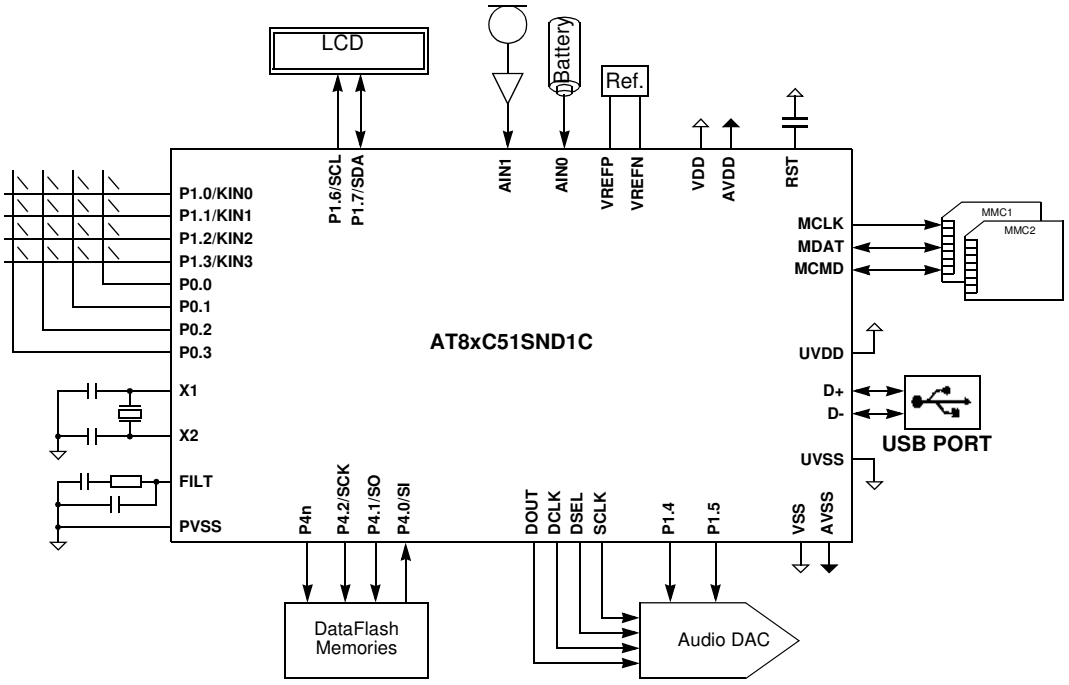


Figure 5-2. AT8xC51SND1C Typical Application with On-Board Atmel DataFlash and // LCD

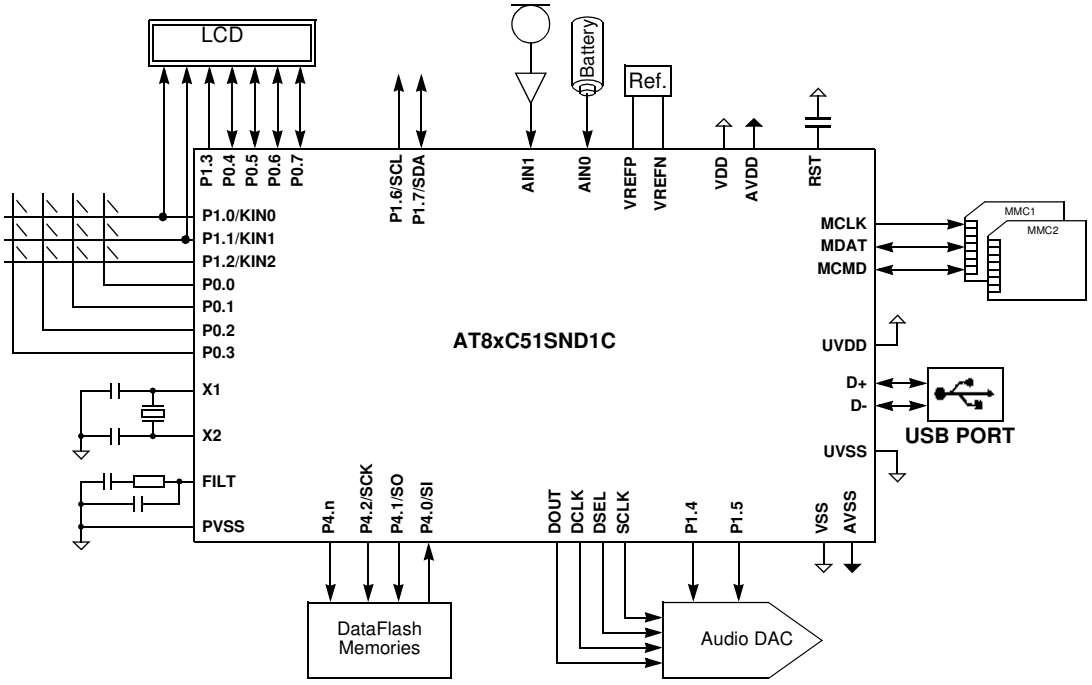


Figure 5-3. AT8xC51SND1C Typical Application with On-Board SSFDC Flash

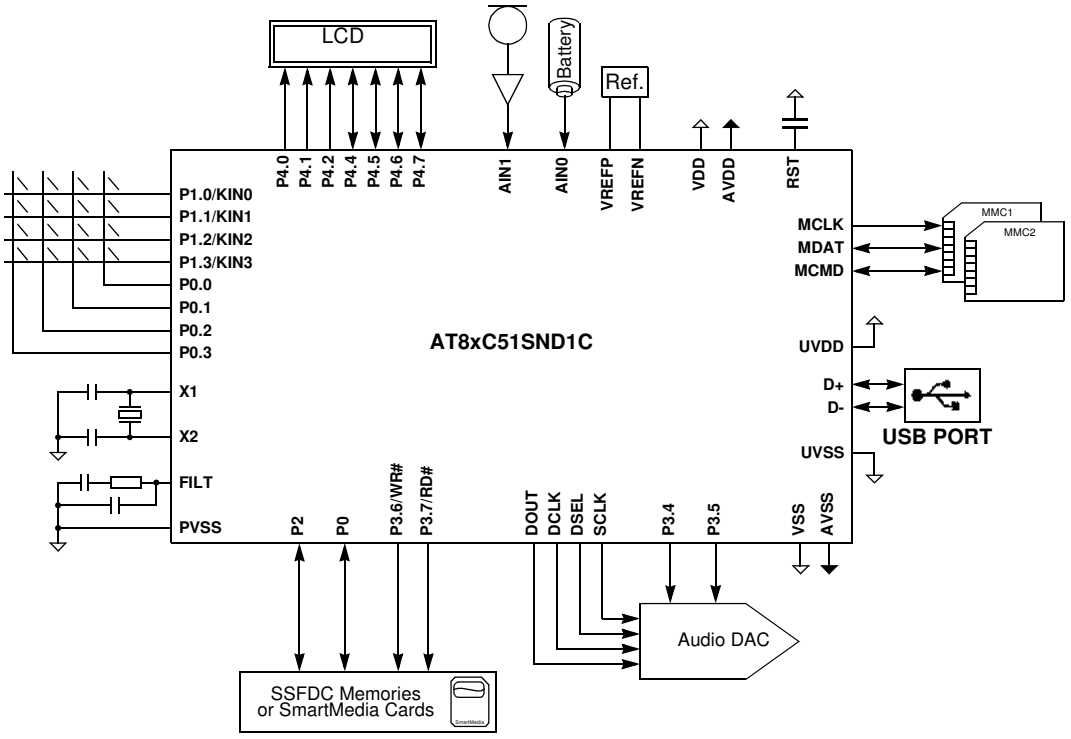
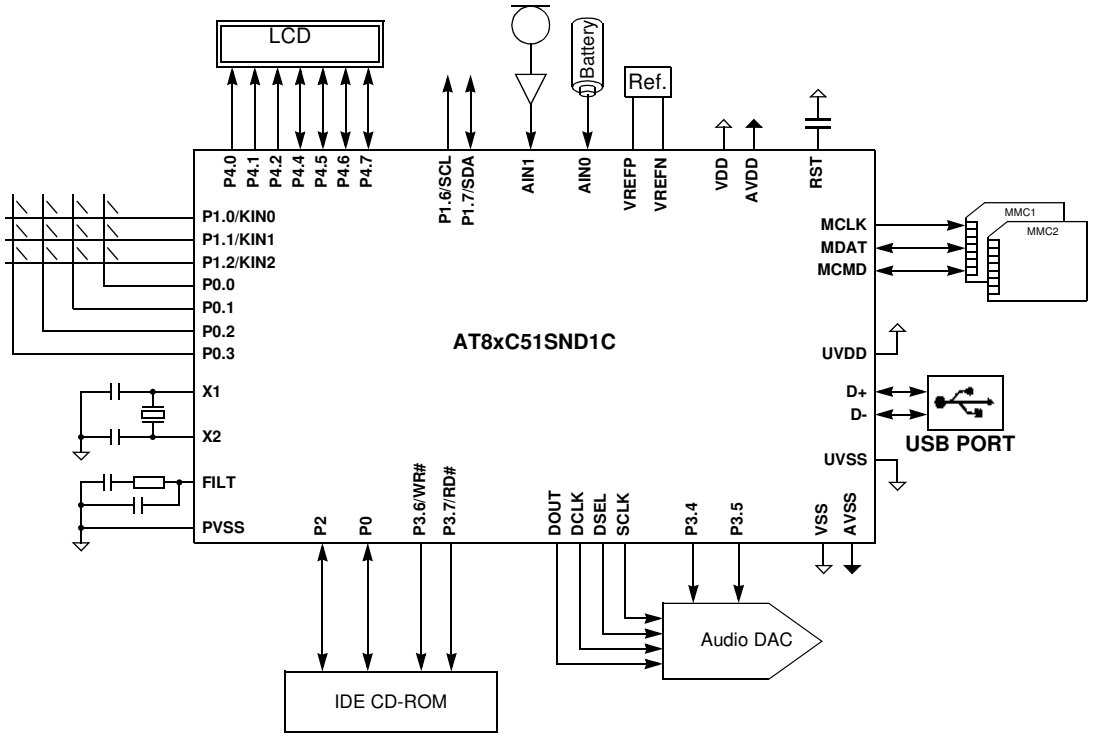


Figure 5-4. AT8xC51SND1C Typical Application with IDE CD-ROM Drive



6. Peripherals

The AT8xC51SND1C peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the AT8xC51SND1C design guide.

6.1 Clock Generator System

The AT8xC51SND1C internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the MP3 decoder, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The MP3 decoder clock is generated by dividing the PLL output clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

6.2 Ports

The AT8xC51SND1C implements five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/O, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/O and alternate functions.

6.3 Timers/Counters

The AT8xC51SND1C implements the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

6.4 Watchdog Timer

The AT8xC51SND1C implements a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

6.5 MP3 Decoder

The AT8xC51SND1C implements a MPEG I/II audio layer 3 decoder (known as MP3 decoder).
In MPEG I (ISO 11172-3) three layers of compression have been standardized supporting three sampling frequencies: 48, 44.1, and 32 KHz. Among these layers, layer 3 allows highest compression rate of about 12:1 while still maintaining CD audio quality. For example, 3 minutes of CD audio (16-bit PCM, 44.1 KHz) data, which needs about 32 MBytes of storage, can be encoded into only 2.7 MBytes of MPEG I audio layer 3 data.
In MPEG II (ISO 13818-3), three additional sampling frequencies: 24, 22.05, and 16 KHz are supported for low bit rates applications.
The AT8xC51SND1C can decode in real-time the MPEG I audio layer 3 encoded data into a PCM audio data, and also supports MPEG II audio layer 3 additional frequencies.

Additional features are supported by the AT8xC51SND1C MP3 decoder such as volume, bass, medium, and treble controls, bass boost effect and ancillary data extraction.

Table 16. Digital DC Characteristics
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
I_{DD}	AT89C51SND1C Operating Current		(3)	X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT83SND1C Operating Current			X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT80C51SND1C Idle Mode Current			X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{DL}	AT89C51SND1C Idle Mode Current		(3)	X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT83SND1C Idle Mode Current			X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT80C51SND1C Idle Mode Current			X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{PD}	AT89C51SND1C Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V
	AT83SND1C Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V
	AT80C51SND1C Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V
I_{FP}	AT89C51SND1C Flash Programming Current			15	mA	V_{DD} < 3.3 V

Notes:
1. Typical values are obtained using V_{DD}= 3 V and T_A= 25°C. They are not tested and there is no guarantee on these values.
2. Flash retention is guaranteed with the same formula for V_{DD} min down to 0V.
3. See Table 17 for typical consumption in player mode.

Table 17. Typical Reference Design AT89C51SND1C Power Consumption

Player Mode	I_{DD}	Test Conditions
Stop	10 mA	AT89C51SND1C at 16 MHz, X2 mode, V_{DD}= 3 V No song playing
Playing	30 mA	AT89C51SND1C at 16 MHz, X2 mode, V_{DD}= 3 V MP3 Song with Fs= 44.1 KHz, at any bit rates (Variable Bit Rate)

7.2.2 A to D Converter

Table 18. A to D Converter DC Characteristics

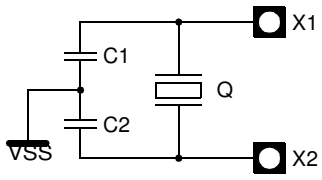
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
AV_{DD}	Analog Supply Voltage	2.7		3.3	V	
AI_{DD}	Analog Operating Supply Current			600	µA	AV_{DD}= 3.3V AIN1:0= 0 to AV_{DD} ADEN= 1
AI_{PD}	Analog Standby Current			2	µA	AV_{DD}= 3.3V ADEN= 0 or PD= 1
AV_{IN}	Analog Input Voltage	AV_{SS}		AV_{DD}	V	
AV_{REF}	Reference Voltage A_{REFN} A_{REFP}	 AV_{SS} 2.4		 AV_{DD}	V	
R_{REF}	AREF Input Resistance	10		30	KΩ	T_A= 25°C
C_{IA}	Analog Input capacitance			10	pF	T_A= 25°C

7.2.3 Oscillator & Crystal

7.2.3.1 Schematic

Figure 7-4. Crystal Connection



Note: For operation with most standard crystals, no external components are needed on X1 and X2. It may be necessary to add external capacitors on X1 and X2 to ground in special cases (max 10 pF). X1 and X2 may not be used to drive other circuits.

7.2.3.2 Parameters

Table 19. Oscillator & Crystal Characteristics

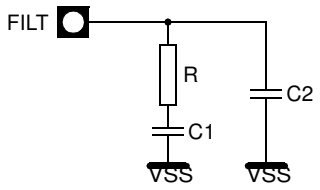
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
C_{X1}	Internal Capacitance (X1 - VSS)		10		pF
C_{X2}	Internal Capacitance (X2 - VSS)		10		pF
C_L	Equivalent Load Capacitance (X1 - X2)		5		pF
DL	Drive Level			50	µW
F	Crystal Frequency			20	MHz
RS	Crystal Series Resistance			40	Ω
CS	Crystal Shunt Capacitance			6	pF

7.2.4 Phase Lock Loop

7.2.4.1 Schematic

Figure 7-5. PLL Filter Connection



7.2.4.2 Parameters

Table 20. PLL Filter Characteristics

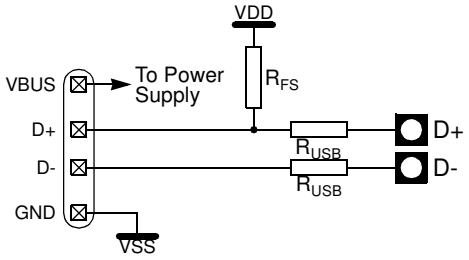
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R	Filter Resistor		100		Ω
C1	Filter Capacitance 1		10		nF
C2	Filter Capacitance 2		2.2		nF

7.2.5 USB Connection

7.2.5.1 Schematic

Figure 7-6. USB Connection



7.2.5.2 Parameters

Table 21. USB Characteristics

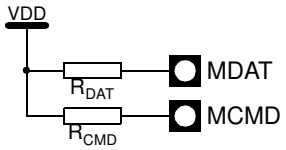
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{USB}	USB Termination Resistor		27		Ω
R_{FS}	USB Full Speed Resistor		1.5		KΩ

7.2.6 MMC Controller

7.2.6.1 Schematic

Figure 7-7. MMC Connection



7.2.6.2 Parameters

Table 22. MMC Components Characteristics

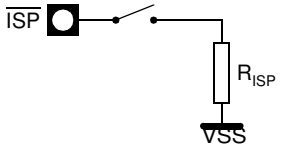
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{CMD}	MMC/SD Command Line Pull-Up Resistor		1OO		KΩ
R_{DAT}	MMC/SD Data Line Pull-Up Resistor		10		KΩ

7.2.7 In System Programming

7.2.7.1 Schematic

Figure 7-8. ISP Pull-Down Connection



7.2.7.2 Parameters

Table 23. ISP Pull-Down Characteristics

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{ISP}	ISP Pull-Down Resistor		2.2		KΩ

7.3 AC Characteristics

7.3.1 External Program Bus Cycles

7.3.1.1 Definition of Symbols

Table 24. External Program Bus Cycles Timing Symbol Definitions

Signals	
A	Address
I	Instruction In
L	ALE
P	$\overline{\text{PSEN}}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

7.3.1.2 Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 25. External Program Bus Cycle - Read AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLIV}	ALE Low to Valid Instruction	$4 \cdot T_{CLCL}-35$		$2 \cdot T_{CLCL}-35$		ns
T_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	$3 \cdot T_{CLCL}-25$		$1.5 \cdot T_{CLCL}-25$		ns
T_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction		$3 \cdot T_{CLCL}-35$		$1.5 \cdot T_{CLCL}-35$	ns
T_{PXIX}	Instruction Hold After $\overline{\text{PSEN}}$ High	0		0		ns
T_{PXIZ}	Instruction Float After $\overline{\text{PSEN}}$ High		$T_{CLCL}-10$		$0.5 \cdot T_{CLCL}-10$	ns
T_{AVIV}	Address Valid to Valid Instruction		$5 \cdot T_{CLCL}-35$		$2.5 \cdot T_{CLCL}-35$	ns
T_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{RHLH}	$\overline{RD}$ high to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}-65$		$4.5 \cdot T_{CLCL}-65$	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}-30$		$2.5 \cdot T_{CLCL}-30$	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Data Float After $\overline{RD}$ High		$2 \cdot T_{CLCL}-25$		$T_{CLCL}-25$	ns

Table 28. External Data 8-bit Bus Cycle - Write AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}-30$		$1.5 \cdot T_{CLCL}-30$		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}-20$		$3.5 \cdot T_{CLCL}-20$		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	$T_{CLCL}-15$		$0.5 \cdot T_{CLCL}-15$		ns

7.3.2.3 Waveforms

Figure 7-10. External Data 8-bit Bus Cycle - Read Waveforms

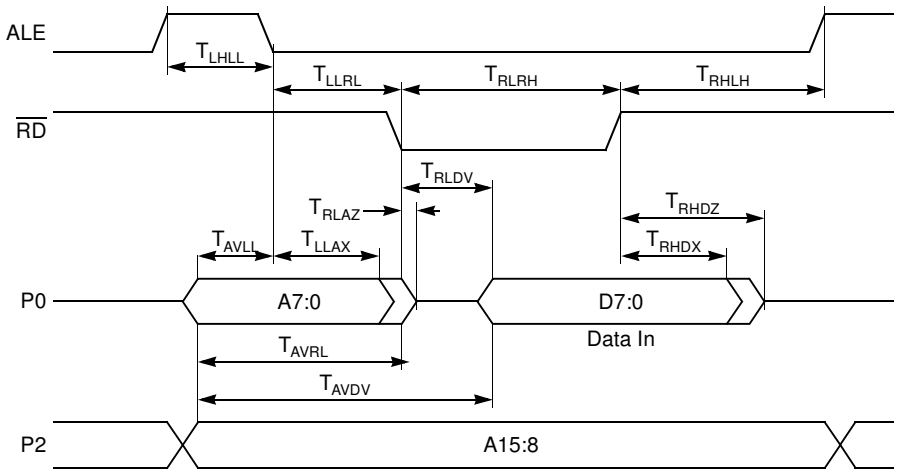
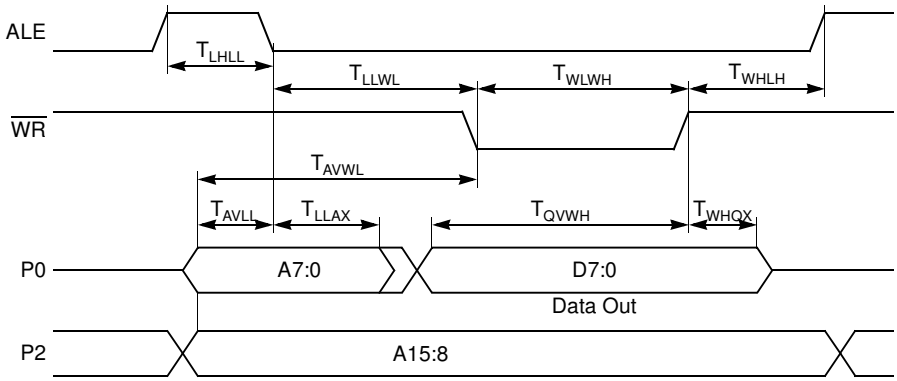


Figure 7-11. External Data 8-bit Bus Cycle - Write Waveforms



7.3.3 External IDE 16-bit Bus Cycles

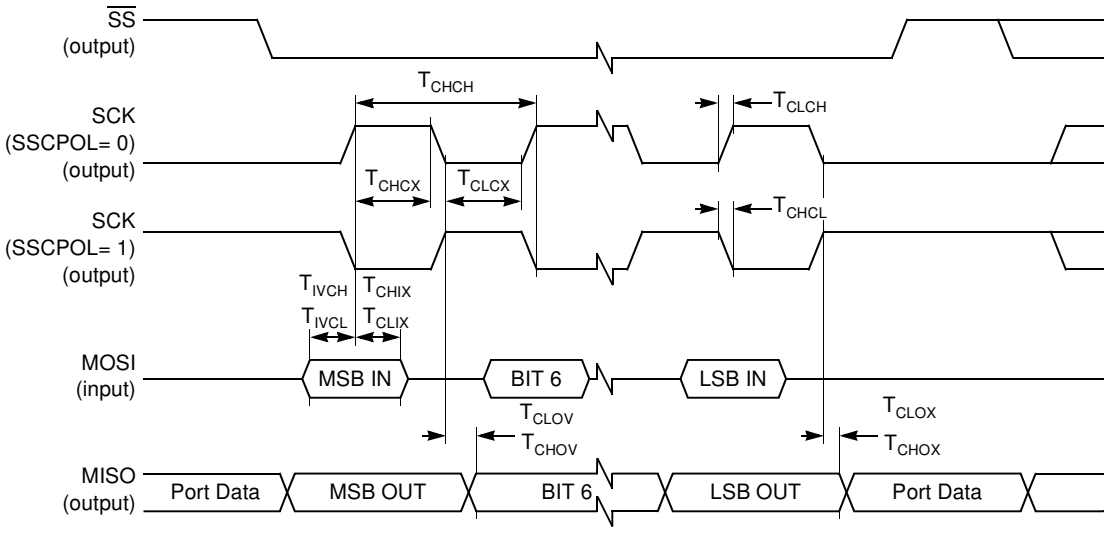
7.3.3.1 Definition of Symbols

Table 29. External IDE 16-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

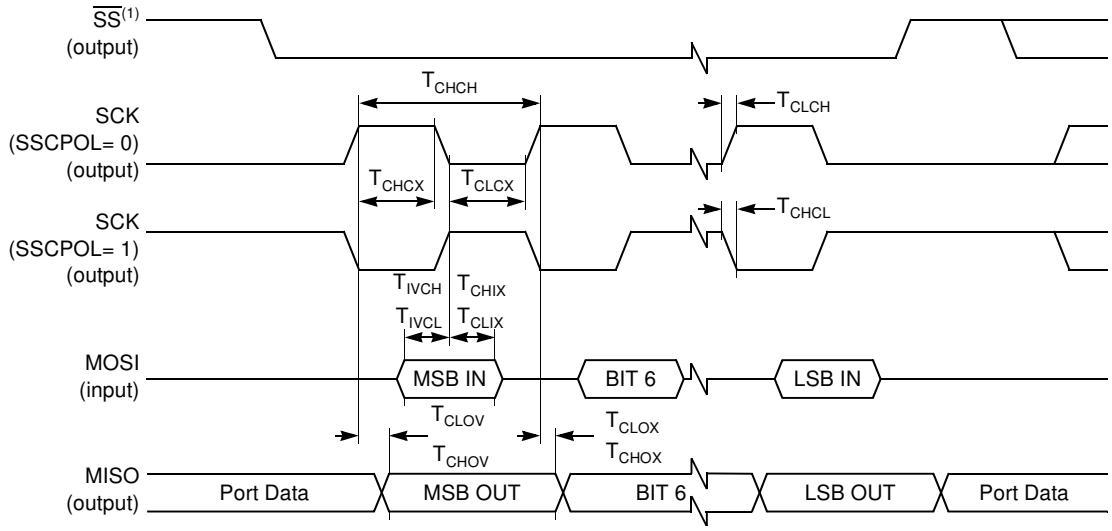
Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Figure 7-16. SPI Master Waveforms (SSCPHA= 0)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Figure 7-17. SPI Master Waveforms (SSCPHA= 1)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

7.4.1 Two-wire Interface

7.4.1.1 Timings

Table 34. TWI Interface AC Timing

7.4.3 Audio Interface

7.4.3.1 Definition of symbols

Table 37. Audio Interface Timing Symbol Definitions

Signals	
C	Clock
O	Data Out
S	Data Select

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

7.4.3.2 Timings

Table 38. Audio Interface AC timings

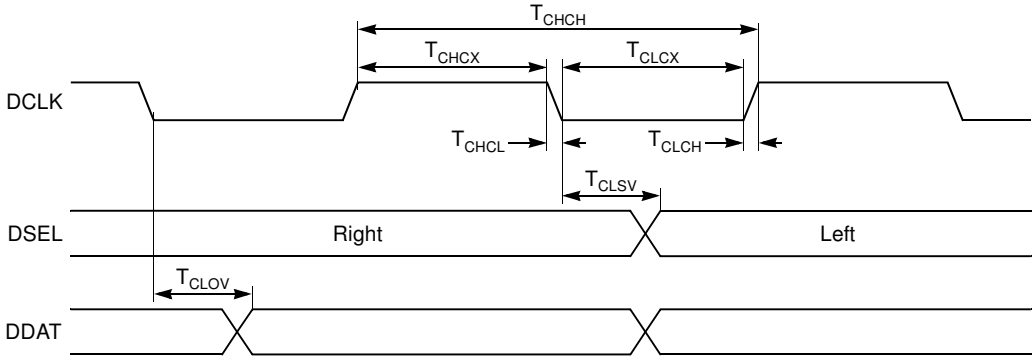
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C, CL≤ 30pF

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period		325.5(1)	ns
T_{CHCX}	Clock High Time	30		ns
T_{CLCX}	Clock Low Time	30		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{CLSV}	Clock Low to Select Valid		10	ns
T_{CLOV}	Clock Low to Data Valid		10	ns

Note: 1. 32-bit format with Fs= 48 KHz.

7.4.3.3 Waveforms

Figure 7-20. Audio Interface Waveforms



7.4.4.3 Waveforms

Figure 7-21. Analog to Digital Converter Internal Waveforms

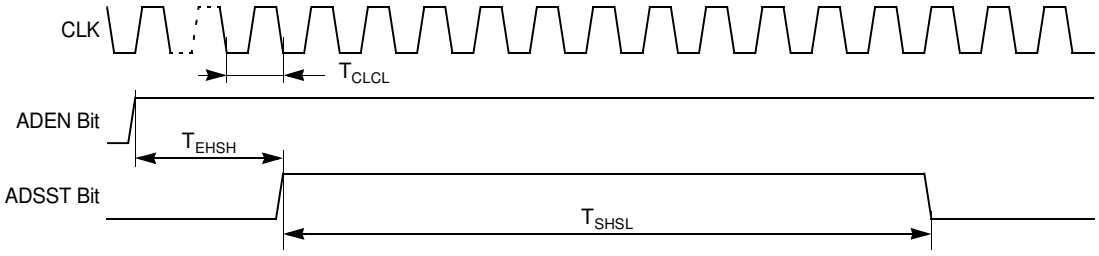
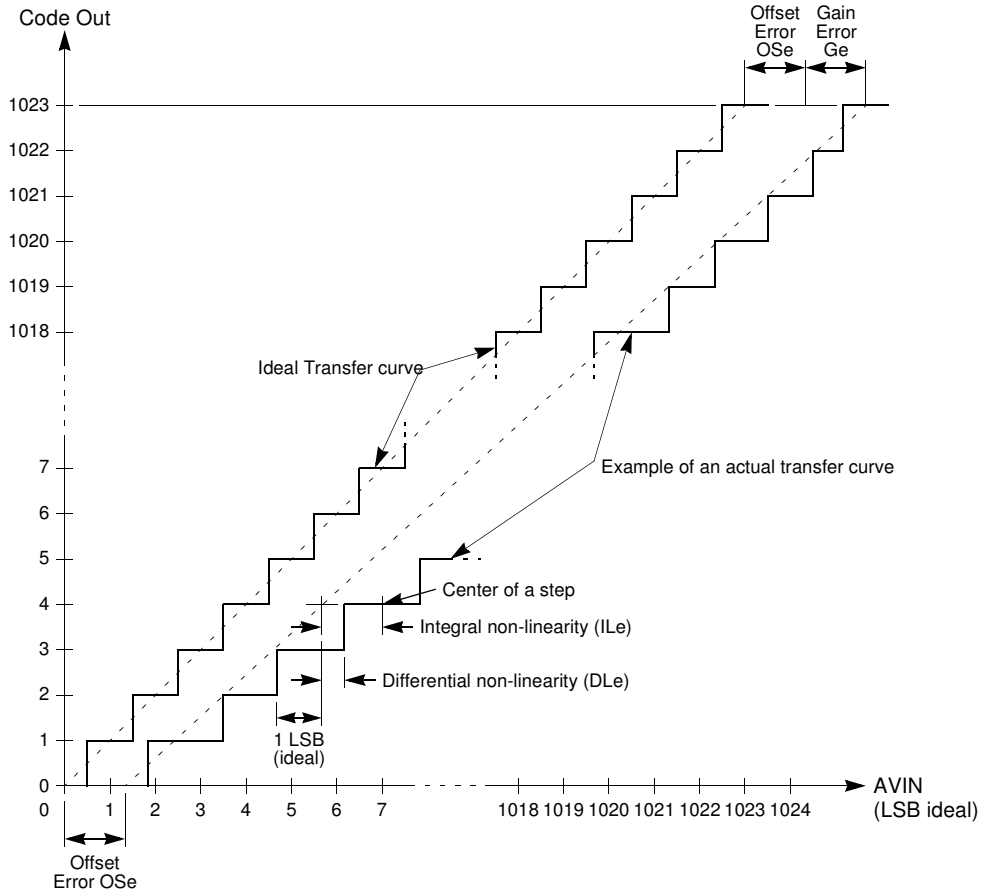


Figure 7-22. Analog to Digital Converter Characteristics



8. Ordering Information

Part Number	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package[2]	Packing	Product Marking
AT89C51SND1C-ROTIL	OBSOLETE						
AT89C51SND1C-7HTIL							
AT89C51SND1C-DDV							
AT83SND1Cxxx[1]-ROTIL							
AT83SND1Cxxx[1]-7HTIL							
AT83SND1Cxxx-DDV							
AT80C51SND1C-ROTIL							
AT80C51SND1C-7HTIL							
AT80C51SND1C-DDV							
AT89C51SND1C-ROTUL	64K Flash	3V	Industrial & Green	40 MHz	TQFP80	Tray	89C51SND1C-IL
AT89C51SND1C-7HTJL	64K Flash	3V	Industrial	40 MHz	BGA81	Tray	89C51SND1C-IL
AT83SND1Cxxx[1]-ROTUL	64K ROM	3V	Industrial & Green	40 MHz	TQFP80	Tray	89C51SND1C-IL
AT83SND1Cxxx[1]-7HTJL	64K ROM	3V	Industrial & Green	40 MHz	BGA81	Tray	89C51SND1C-IL
AT80C51SND1C-ROTUL	ROMless	3V	Industrial & Green	40 MHz	TQFP80	Tray	89C51SND1C-IL
AT80C51SND1C-7HTJL	ROMless	3V	Industrial & Green	40 MHz	BGA81	Tray	89C51SND1C-IL

Notes: 1. Refers to ROM code.
2. PLCC84 package only available for development board.