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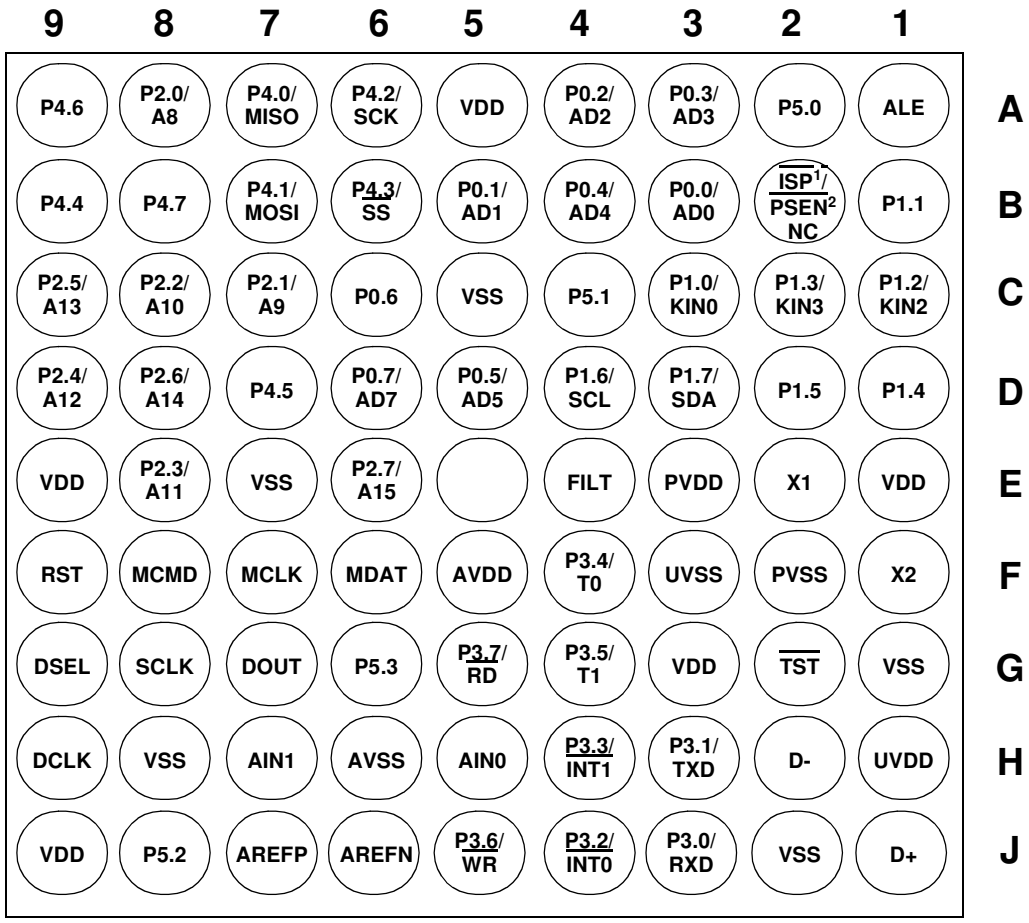
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IDE/ATAPI, Memory Card, SPI, UART/USART, USB
Peripherals	Audio, I²S, MP3, PCM, POR, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LFBGA
Supplier Device Package	81-BGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51snd1c-7htul

Figure 4-2. AT8xC51SND1C 81-pin BGA Package



Notes: 1. $\overline{\text{ISP}}$ pin is only available in AT89C51SND1C product.
Do not connect this pin on AT83SND1C and AT80C51SND1C product.
2. $\overline{\text{PSEN}}$ pin is only available in AT80C51SND1C product.

Signal Name	Type	Description	Alternate Function
T0	I	**Timer 0 External Clock Input** When timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer 1 External Clock Input** When timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5

Table 4. Audio Interface Signal Description

Signal Name	Type	Description	Alternate Function
DCLK	O	**DAC Data Bit Clock**	-
DOUT	O	**DAC Audio Data**	-
DSEL	O	**DAC Channel Select Signal** DSEL is the sample rate clock output.	-
SCLK	O	**DAC System Clock** SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL).	-

Table 5. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 KΩ pull-up to V_{DD} for full speed operation.	-
D-	I/O	**USB Negative Data Upstream Port**	-

Table 6. MutiMediaCard Interface Signal Description

Signal Name	Type	Description	Alternate Function
MCLK	O	**MMC Clock output** Data or command clock transfer.	-
MCMD	I/O	**MMC Command line** Bidirectional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to V_{DD} or V_{SS}.	-
MDAT	I/O	**MMC Data line** Bidirectional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to V_{DD} or V_{SS}.	-

Table 7. UART Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1

Table 8. SPI Controller Signal Description

Signal Name	Type	Description	Alternate Function
MISO	I/O	**SPI Master Input Slave Output Data Line** When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller.	P4.0
MOSI	I/O	**SPI Master Output Slave Input Data Line** When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller.	P4.1
SCK	I/O	**SPI Clock Line** When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.	P4.2
$\overline{SS}$	I	**SPI Slave Select Line** When in controlled slave mode, $\overline{SS}$ enables the slave mode.	P4.3

Table 9. TWI Controller Signal Description

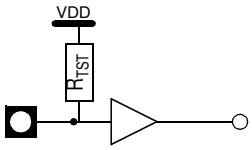
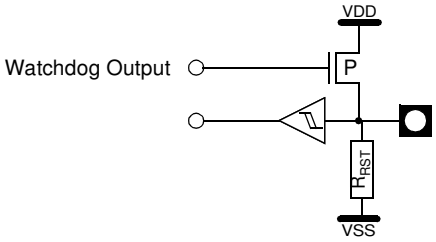
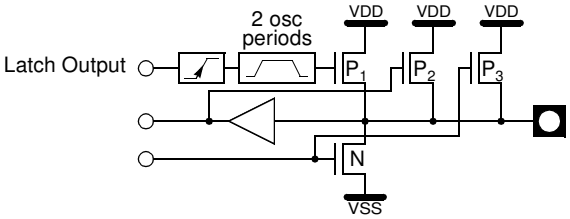
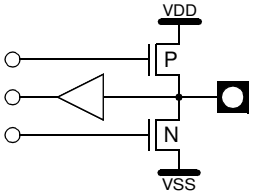
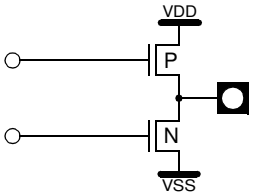
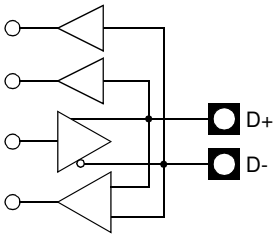
Signal Name	Type	Description	Alternate Function
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to the slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bidirectional Two Wire data line.	P1.7

Table 10. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AVSS.	-

4.3 Internal Pin Structure

Table 15. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input	$\overline{TST}$
	Input/Output	RST
	Input/Output	P1[2] P2[3] P3 P4 P53:0
	Input/Output	P0 MCMD MDAT $\overline{ISP}$ $\overline{PSEN}$
	Output	ALE SCLK DCLK DOUT DSEL MCLK
	Input/Output	D+ D-

Notes:
1. For information on resistors value, input/output levels, and drive capability, refer to the Section “DC Characteristics”, page 18.
2. When the Two Wire controller is enabled, P_1, P_2, and P_3 transistors are disabled allowing pseudo open-drain structure.
3. In Port 2, P_1 transistor is continuously driven when outputting a high level bit address (A15:8).

5. Application Information

Figure 5-1. AT8xC51SND1C Typical Application with On-Board Atmel DataFlash and 2-wire LCD

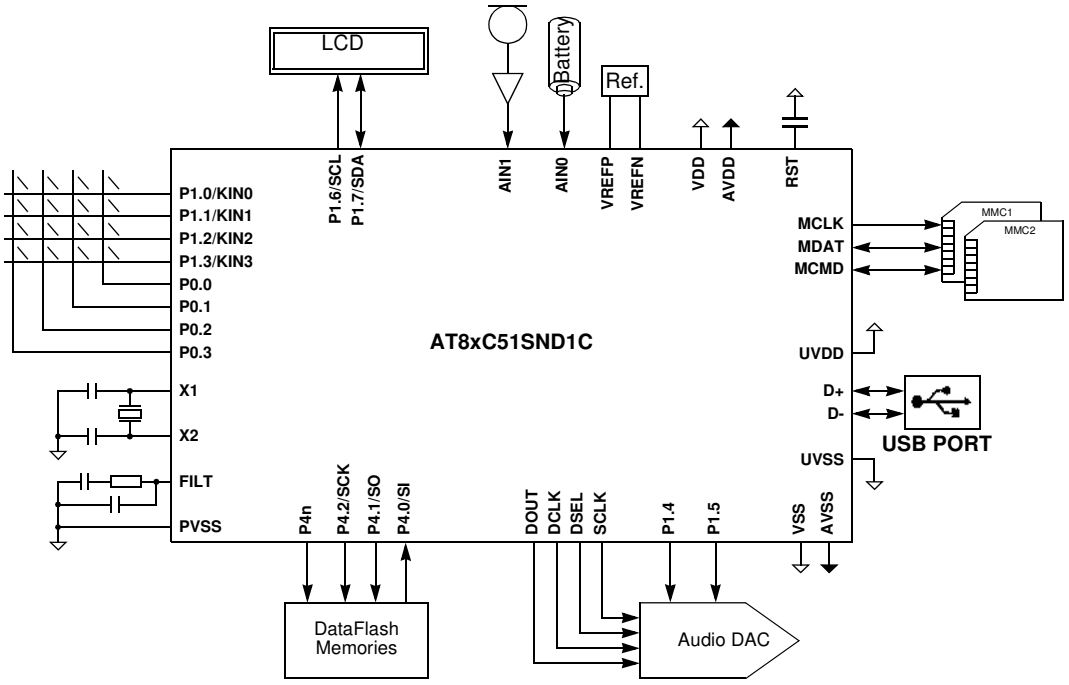


Figure 5-2. AT8xC51SND1C Typical Application with On-Board Atmel DataFlash and // LCD

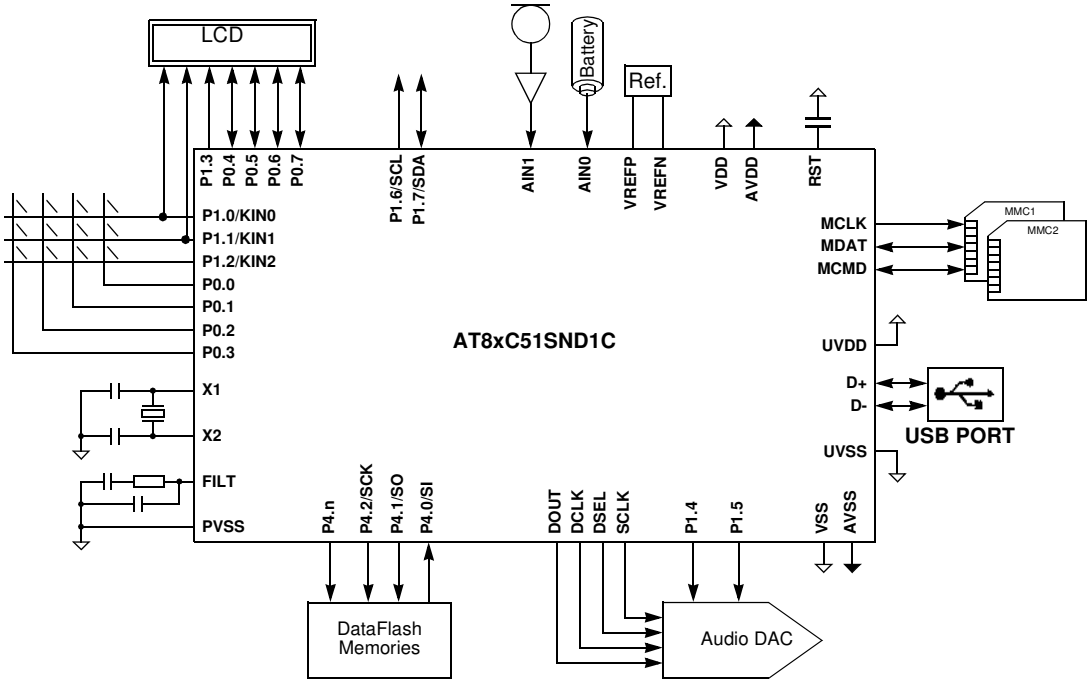
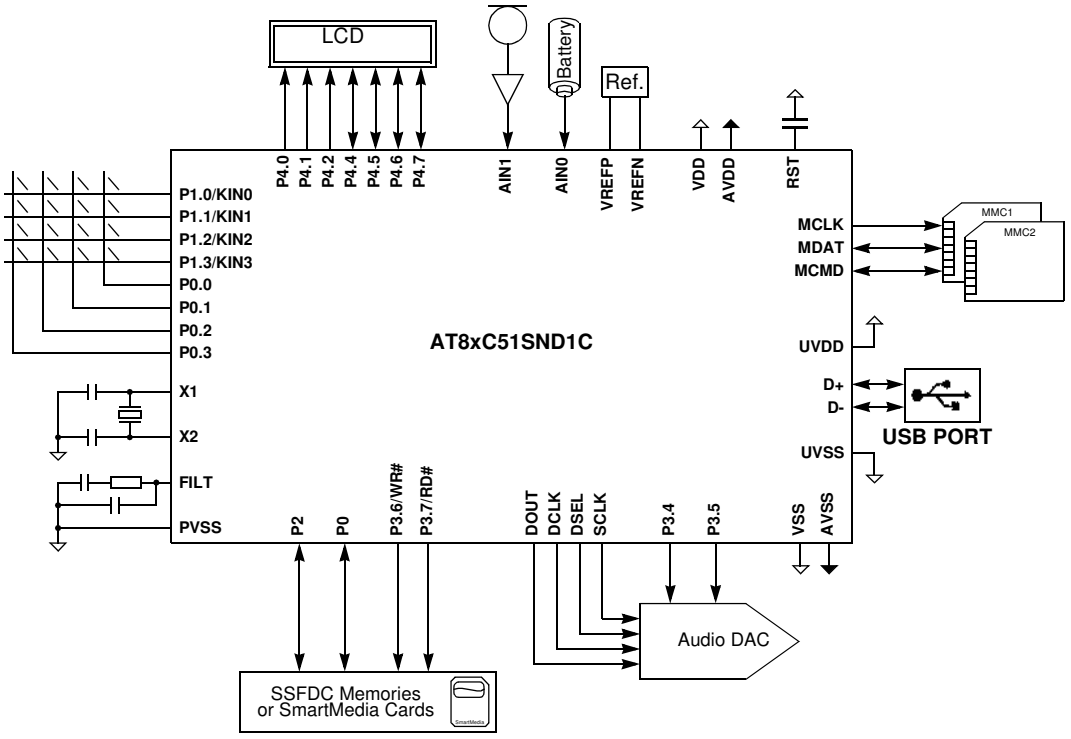


Figure 5-3. AT8xC51SND1C Typical Application with On-Board SSFDC Flash



6.6 Audio Output Interface

The AT8xC51SND1C implements an audio output interface allowing the decoded audio bit-stream to be output in various formats. It is compatible with right and left justification PCM and I^2S formats and thanks to the on-chip PLL (see Section 6.1) allows connection of almost all of the commercial audio DAC families available on the market.

6.7 Universal Serial Bus Interface

The AT8xC51SND1C implements a full speed Universal Serial Bus Interface. It can be used for the following purposes:

- Download of MP3 encoded audio files by supporting the USB mass storage class.
- In System Programming by supporting the USB firmware upgrade class.

6.8 MultiMediaCard Interface

The AT8xC51SND1C implements a MultiMediaCard (MMC) interface compliant to the V2.2 specification in MultiMediaCard Mode. The MMC allows storage of MP3 encoded audio files in removable flash memory cards that can be easily plugged or removed from the application. It can also be used for In System Programming.

6.9 IDE/ATAPI interface

The AT8xC51SND1C provides an IDE/ATAPI interface allowing connexion of devices such as CD-ROM reader, CompactFlash cards, Hard Disk Drive… It consists in a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In System Programming using CD-ROM.

6.10 Serial I/O Interface

The AT8xC51SND1C implements a serial port with its own baud rate generator providing one single synchronous communication mode and three full-duplex Universal Asynchronous Receiver Transmitter (UART) communication modes. It is provided for the following purposes:

- In System Programming.
- Remote control of the AT8xC51SND1C by a host.

6.11 Serial Peripheral Interface

The AT8xC51SND1C implements a Serial Peripheral Interface (SPI) supporting master and slave modes. It is provided for the following purposes:

- Interfacing DataFlash memory for MP3 encoded audio files storage.
- Remote control of the AT8xC51SND1C by a host.
- In System Programming.

6.12 2-wire Controller

The AT8xC51SND1C implements a 2-wire controller supporting the four standard master and slave modes with multimaster capability. It is provided for the following purposes:

- Connection of slave devices like LCD controller, audio DAC…
- Remote control of the AT8xC51SND1C by a host.
- In System Programming.

7.2.2 A to D Converter

Table 18. A to D Converter DC Characteristics

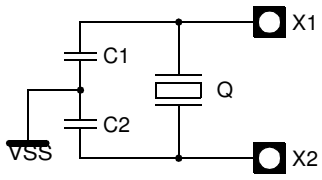
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
AV_{DD}	Analog Supply Voltage	2.7		3.3	V	
AI_{DD}	Analog Operating Supply Current			600	µA	AV_{DD}= 3.3V AIN1:0= 0 to AV_{DD} ADEN= 1
AI_{PD}	Analog Standby Current			2	µA	AV_{DD}= 3.3V ADEN= 0 or PD= 1
AV_{IN}	Analog Input Voltage	AV_{SS}		AV_{DD}	V	
AV_{REF}	Reference Voltage A_{REFN} A_{REFP}	 AV_{SS} 2.4		 AV_{DD}	V	
R_{REF}	AREF Input Resistance	10		30	KΩ	T_A= 25°C
C_{IA}	Analog Input capacitance			10	pF	T_A= 25°C

7.2.3 Oscillator & Crystal

7.2.3.1 Schematic

Figure 7-4. Crystal Connection



Note: For operation with most standard crystals, no external components are needed on X1 and X2. It may be necessary to add external capacitors on X1 and X2 to ground in special cases (max 10 pF). X1 and X2 may not be used to drive other circuits.

7.2.3.2 Parameters

Table 19. Oscillator & Crystal Characteristics

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
C_{X1}	Internal Capacitance (X1 - VSS)		10		pF
C_{X2}	Internal Capacitance (X2 - VSS)		10		pF
C_L	Equivalent Load Capacitance (X1 - X2)		5		pF
DL	Drive Level			50	µW
F	Crystal Frequency			20	MHz
RS	Crystal Series Resistance			40	Ω
CS	Crystal Shunt Capacitance			6	pF

7.3 AC Characteristics

7.3.1 External Program Bus Cycles

7.3.1.1 Definition of Symbols

Table 24. External Program Bus Cycles Timing Symbol Definitions

Signals	
A	Address
I	Instruction In
L	ALE
P	$\overline{\text{PSEN}}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

7.3.1.2 Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 25. External Program Bus Cycle - Read AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLIV}	ALE Low to Valid Instruction	$4 \cdot T_{CLCL}-35$		$2 \cdot T_{CLCL}-35$		ns
T_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	$3 \cdot T_{CLCL}-25$		$1.5 \cdot T_{CLCL}-25$		ns
T_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction		$3 \cdot T_{CLCL}-35$		$1.5 \cdot T_{CLCL}-35$	ns
T_{PXIX}	Instruction Hold After $\overline{\text{PSEN}}$ High	0		0		ns
T_{PXIZ}	Instruction Float After $\overline{\text{PSEN}}$ High		$T_{CLCL}-10$		$0.5 \cdot T_{CLCL}-10$	ns
T_{AVIV}	Address Valid to Valid Instruction		$5 \cdot T_{CLCL}-35$		$2.5 \cdot T_{CLCL}-35$	ns
T_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{RHLH}	$\overline{RD}$ high to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}-65$		$4.5 \cdot T_{CLCL}-65$	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}-30$		$2.5 \cdot T_{CLCL}-30$	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Data Float After $\overline{RD}$ High		$2 \cdot T_{CLCL}-25$		$T_{CLCL}-25$	ns

Table 28. External Data 8-bit Bus Cycle - Write AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}-30$		$1.5 \cdot T_{CLCL}-30$		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}-20$		$3.5 \cdot T_{CLCL}-20$		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	$T_{CLCL}-15$		$0.5 \cdot T_{CLCL}-15$		ns

7.3.2.3 Waveforms

Figure 7-10. External Data 8-bit Bus Cycle - Read Waveforms

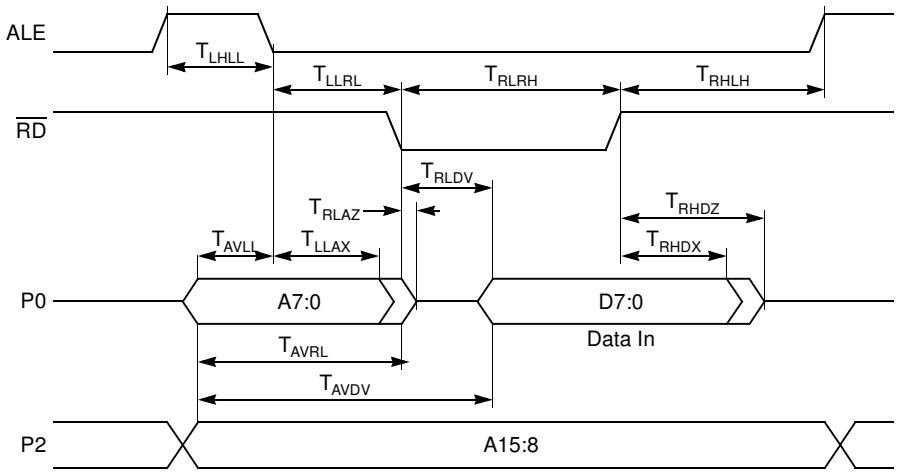
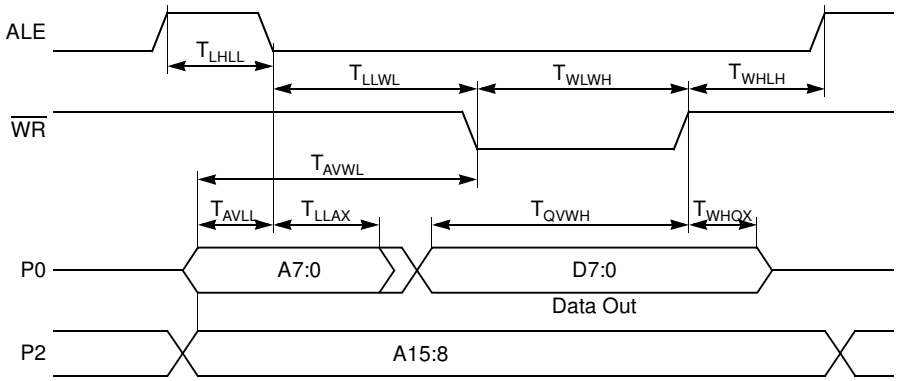


Figure 7-11. External Data 8-bit Bus Cycle - Write Waveforms



7.3.3 External IDE 16-bit Bus Cycles

7.3.3.1 Definition of Symbols

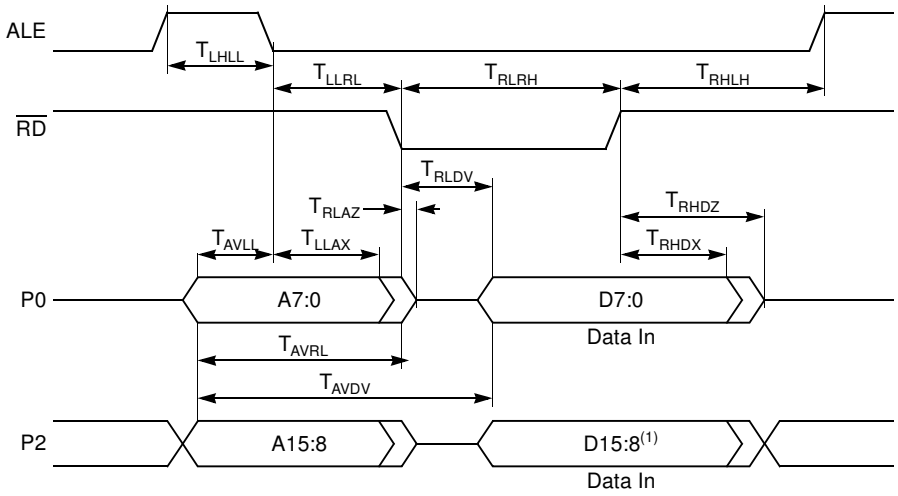
Table 29. External IDE 16-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

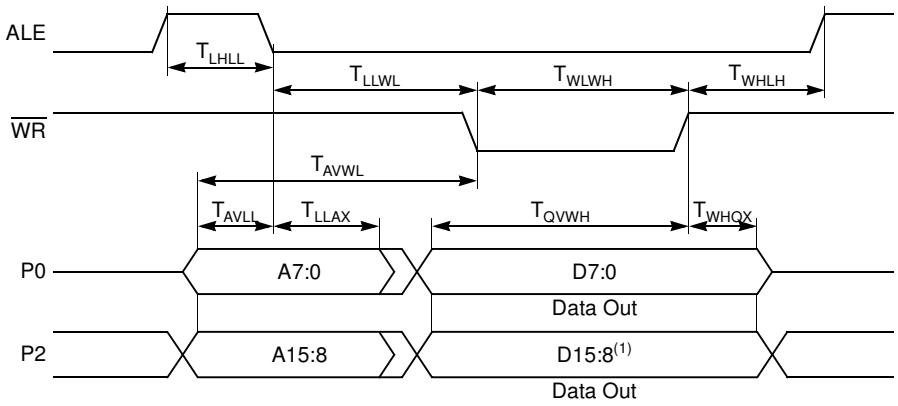
7.3.3.3 Waveforms

Figure 7-12. External IDE 16-bit Bus Cycle - Data Read Waveforms



Note: 1. D15:8 is written in DAT16H SFR.

Figure 7-13. External IDE 16-bit Bus Cycle - Data Write Waveforms



Note: 1. D15:8 is the content of DAT16H SFR.

7.4 SPI Interface

7.4.0.4 Definition of Symbols

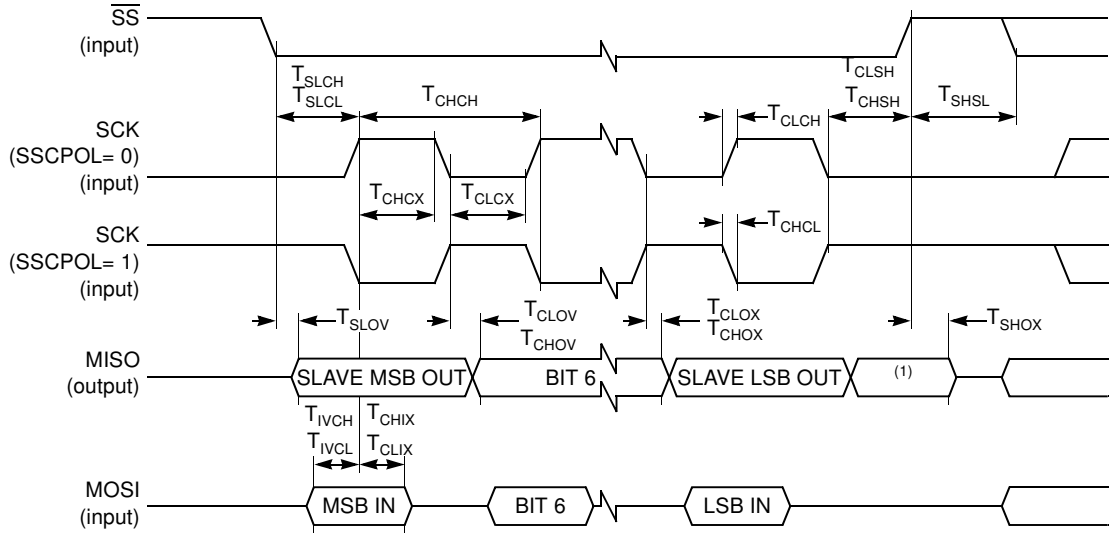
Table 32. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

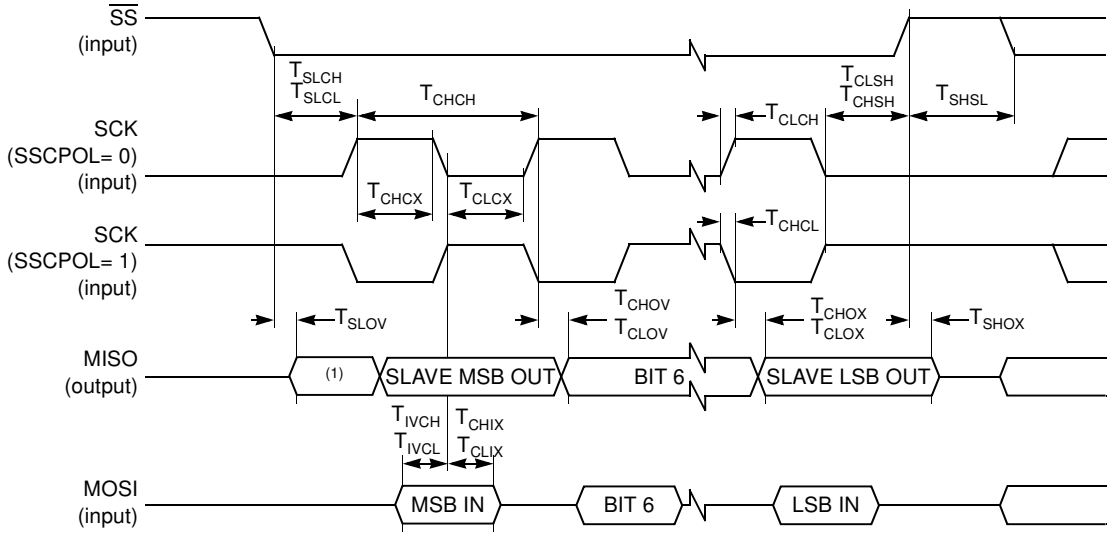
7.4.0.6 Waveforms

Figure 7-14. SPI Slave Waveforms (SSCPHA= 0)



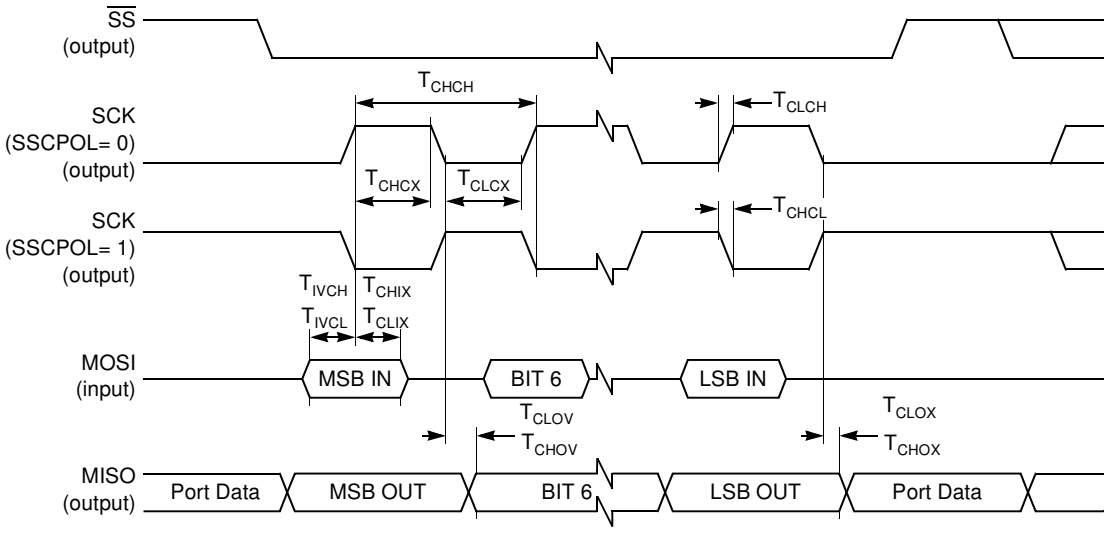
Note: 1. Not Defined but generally the MSB of the character which has just been received.

Figure 7-15. SPI Slave Waveforms (SSCPHA= 1)



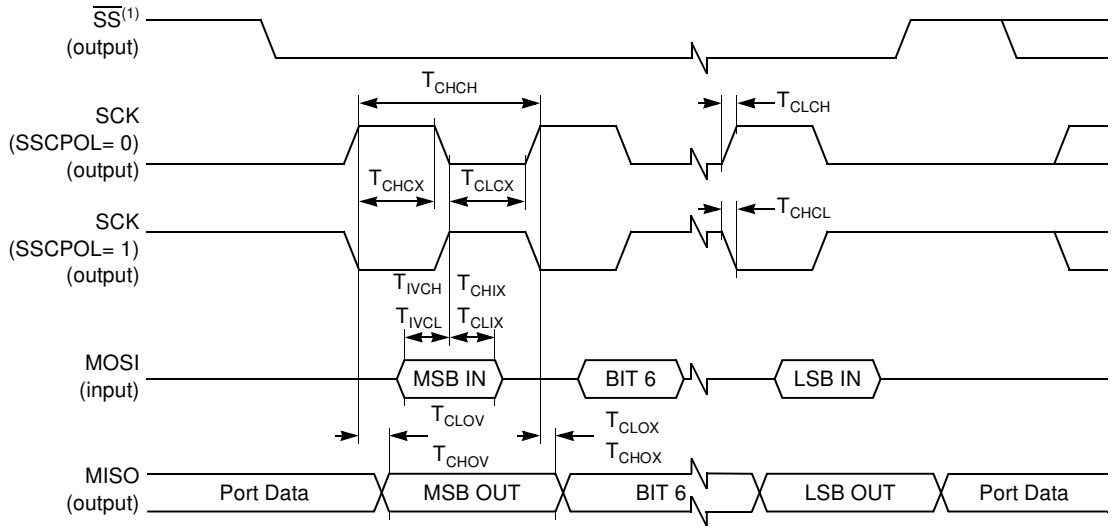
Note: 1. Not Defined but generally the LSB of the character which has just been received.

Figure 7-16. SPI Master Waveforms (SSCPHA= 0)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Figure 7-17. SPI Master Waveforms (SSCPHA= 1)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

7.4.1 Two-wire Interface

7.4.1.1 Timings

Table 34. TWI Interface AC Timing

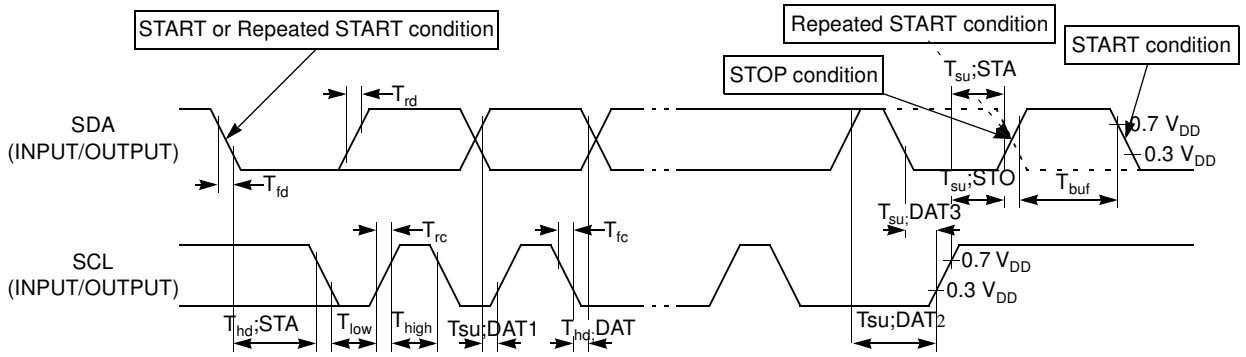
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	INPUT Min Max	OUTPUT Min Max
T_{HD}; STA	Start condition hold time	14·T_{CLCL}(4)	4.0 µs(1)
T_{LOW}	SCL low time	16·T_{CLCL}(4)	4.7 µs(1)
T_{HIGH}	SCL high time	14·T_{CLCL}(4)	4.0 µs(1)
T_{RC}	SCL rise time	1 µs	-(2)
T_{FC}	SCL fall time	0.3 µs	0.3 µs(3)
T_{SU}; DAT1	Data set-up time	250 ns	20·T_{CLCL}(4)- T_{RD}
T_{SU}; DAT2	SDA set-up time (before repeated START condition)	250 ns	1 µs(1)
T_{SU}; DAT3	SDA set-up time (before STOP condition)	250 ns	8·T_{CLCL}(4)
T_{HD}; DAT	Data hold time	0 ns	8·T_{CLCL}(4) - T_{FC}
T_{SU}; STA	Repeated START set-up time	14·T_{CLCL}(4)	4.7 µs(1)
T_{SU}; STO	STOP condition set-up time	14·T_{CLCL}(4)	4.0 µs(1)
T_{BUF}	Bus free time	14·T_{CLCL}(4)	4.7 µs(1)
T_{RD}	SDA rise time	1 µs	-(2)
T_{FD}	SDA fall time	0.3 µs	0.3 µs(3)

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3·T_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL= 400 pF.
4. T_{CLCL}= T_{OSC}= one oscillator clock period.

7.4.1.2 Waveforms

Figure 7-18. Two Wire Waveforms



7.4.2 MMC Interface

7.4.2.1 *Definition of symbols*

Table 35. MMC Interface Timing Symbol Definitions

Signals	
C	Clock
D	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

7.4.2.2 *Timings*

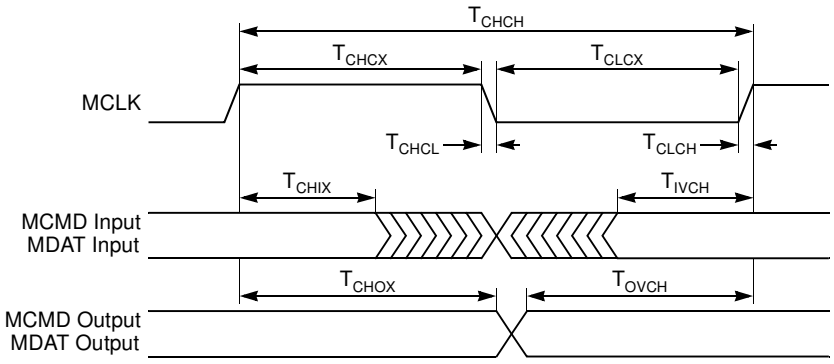
Table 36. MMC Interface AC timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C, CL ≤ 100pF (10 cards)

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period	50		ns
T_{CHCX}	Clock High Time	10		ns
T_{CLCX}	Clock Low Time	10		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{DVCH}	Input Data Valid to Clock High	3		ns
T_{CHDX}	Input Data Hold after Clock High	3		ns
T_{CHOX}	Output Data Hold after Clock High	5		ns
T_{OVCH}	Output Data Valid to Clock High	5		ns

7.4.2.3 *Waveforms*

Figure 7-19. MMC Input-Output Waveforms



7.4.3 Audio Interface

7.4.3.1 Definition of symbols

Table 37. Audio Interface Timing Symbol Definitions

Signals	
C	Clock
O	Data Out
S	Data Select

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

7.4.3.2 Timings

Table 38. Audio Interface AC timings

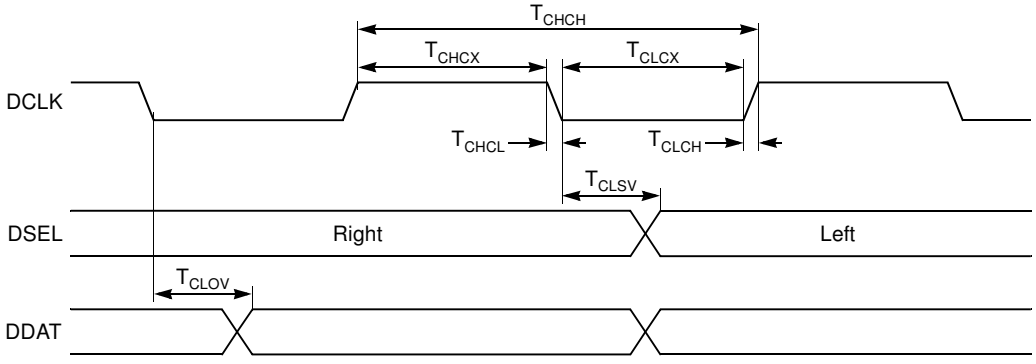
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C, CL≤ 30pF

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period		325.5(1)	ns
T_{CHCX}	Clock High Time	30		ns
T_{CLCX}	Clock Low Time	30		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{CLSV}	Clock Low to Select Valid		10	ns
T_{CLOV}	Clock Low to Data Valid		10	ns

Note: 1. 32-bit format with Fs= 48 KHz.

7.4.3.3 Waveforms

Figure 7-20. Audio Interface Waveforms



7.4.4 Analog to Digital Converter

7.4.4.1 Definition of symbols

Table 39. Analog to Digital Converter Timing Symbol Definitions

Signals	
C	Clock
E	Enable (ADEN bit)
S	Start Conversion (ADSST bit)

Conditions	
H	High
L	Low

7.4.4.2 Characteristics

Table 40. Analog to Digital Converter AC Characteristics

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	4		µs
T_{EHSH}	Start-up Time		4	µs
T_{SHSL}	Conversion Time		$11 \cdot T_{CLCL}$	µs
DLe	Differential non-linearity error(1)(2)		1	LSB
ILe	Integral non-linearity errorss(1)(3)		2	LSB
OSe	Offset error(1)(4)		4	LSB
Ge	Gain error(1)(5)		4	LSB

Notes:
1. AV_{DD}= AV_{REFP}= 3.0 V, AV_{SS}= AV_{REFN}= 0 V. ADC is monotonic with no missing code.
2. The differential non-linearity is the difference between the actual step width and the ideal step width (see Figure 7-22).
3. The integral non-linearity is the peak difference between the center of the actual step and the ideal transfer curve after appropriate adjustment of gain and offset errors (see Figure 7-22).
4. The offset error is the absolute difference between the straight line which fits the actual transfer curve (after removing of gain error), and the straight line which fits the ideal transfer curve (see Figure 7-22).
5. The gain error is the relative difference in percent between the straight line which fits the actual transfer curve (after removing of offset error), and the straight line which fits the ideal transfer curve (see Figure 7-22).

7.4.6 External Clock Drive and Logic Level References

7.4.6.1 Definition of symbols

Table 43. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

7.4.6.2 Timings

External Clock AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	50		ns
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns
T_{CR}	Cyclic Ratio in X2 mode	40	60	%

7.4.6.3 Waveforms

Figure 7-25. External Clock Waveform

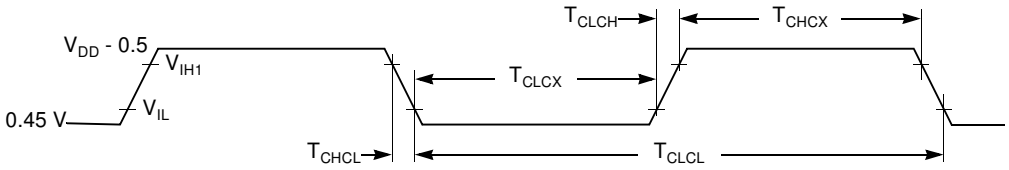
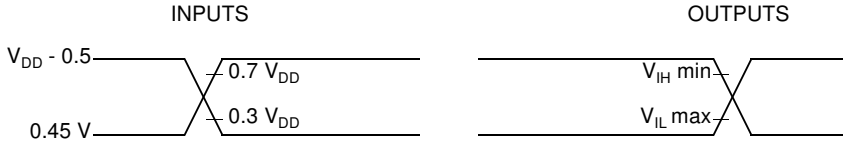
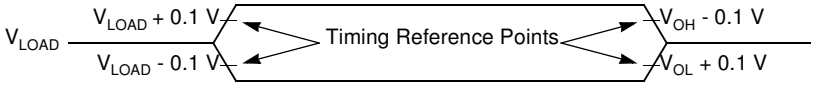


Figure 7-26. AC Testing Input/Output Waveforms



Note: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 7-27. Float Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH}= \pm 20$ mA.