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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IDE/ATAPI, Memory Card, SPI, UART/USART, USB
Peripherals	Audio, I²S, MP3, PCM, POR, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 2x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51snd1c-rotul

1. Description

The AT8xC51SND1C are fully integrated stand-alone hardwired MPEG I/II-Layer 3 decoder with a C51 microcontroller core handling data flow and MP3-player control.

The AT89C51SND1C includes 64K Bytes of Flash memory and allows In-System Programming through an embedded 4K Bytes of Boot Flash memory.

The AT83SND1C includes 64K Bytes of ROM memory.

The AT80C51SND1C does not include any code memory.

The AT8xC51SND1C include 2304 Bytes of RAM memory.

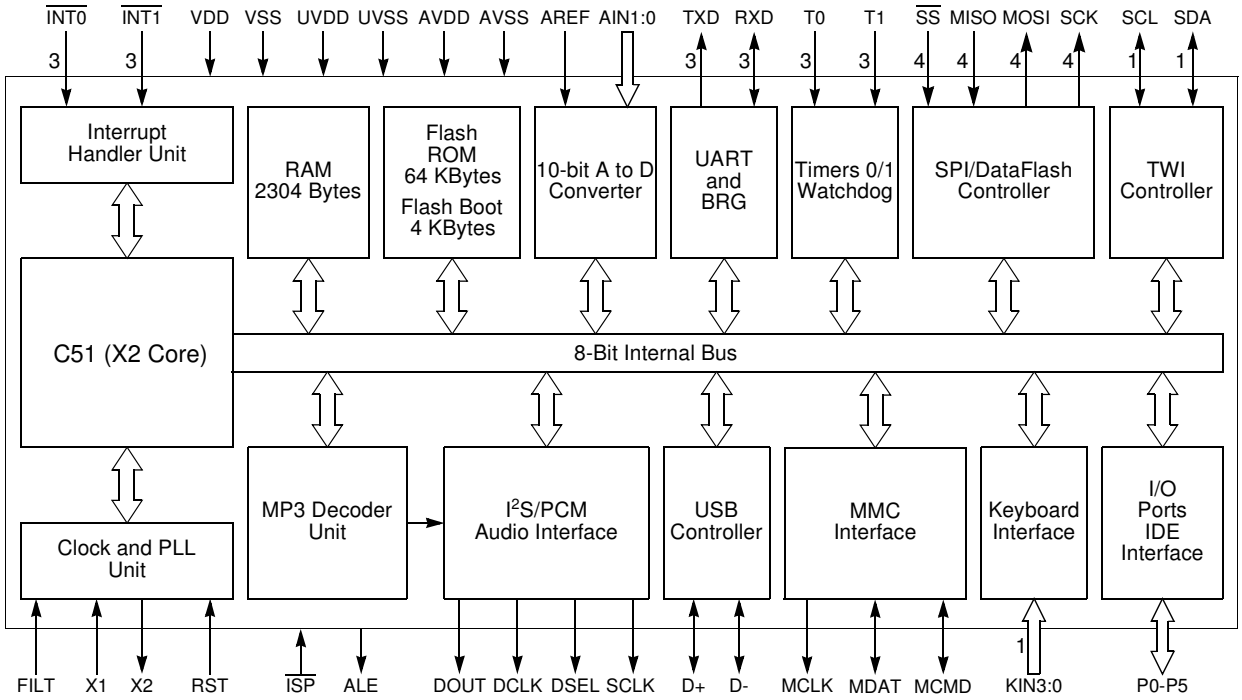
The AT8xC51SND1C provides the necessary features for human interface like timers, keyboard port, serial or parallel interface (USB, TWI, SPI, IDE), ADC input, I^2S output, and all external memory interface (NAND or NOR Flash, SmartMedia, MultiMedia, DataFlash cards).

2. Typical Applications

- MP3-Player
- PDA, Camera, Mobile Phone MP3
- Car Audio/Multimedia MP3
- Home Audio/Multimedia MP3

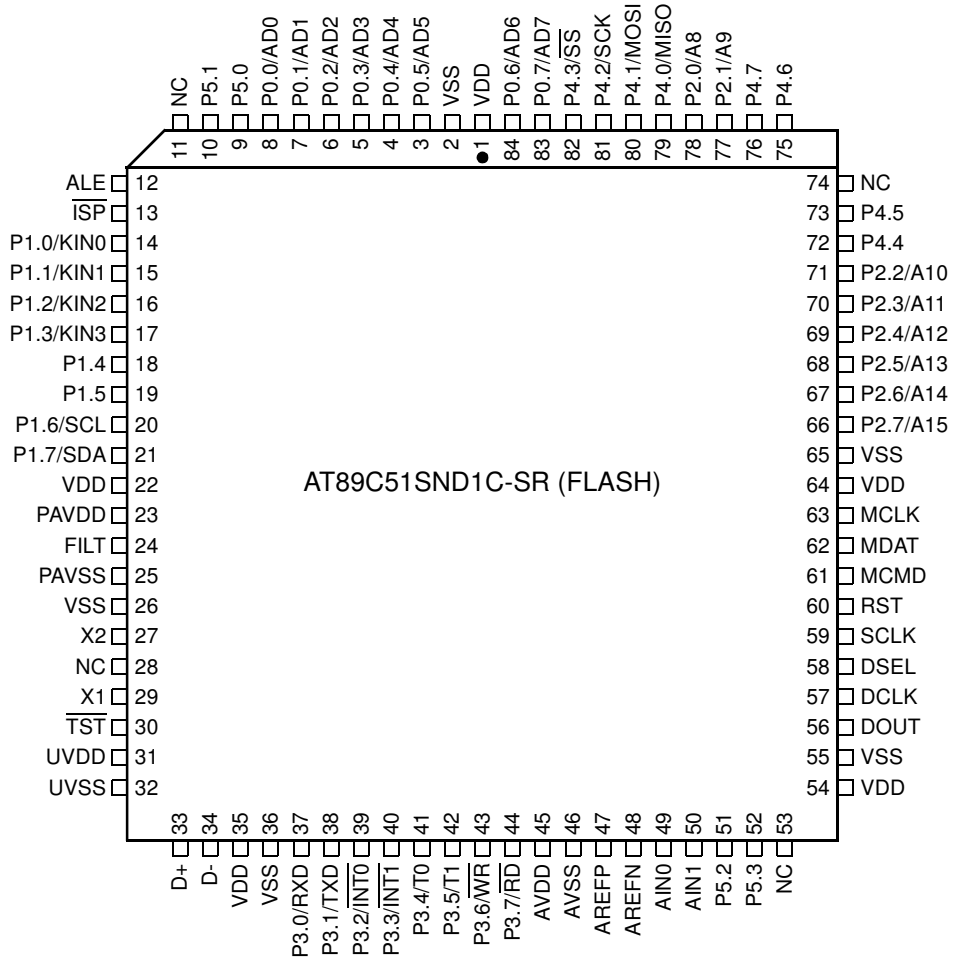
3. Block Diagram

Figure 3-1. AT8xC51SND1C Block Diagram



1 Alternate function of Port 1
3 Alternate function of Port 3
4 Alternate function of Port 4

Figure 4-3. AT8xC51SND1C 84-pin PLCC Package



4.2 Signals

All the AT8xC51SND1C signals are detailed by functionality in Table 1 to Table 14.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN3:0 SCL SDA
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8

Signal Name	Type	Description	Alternate Function
P3.7:0	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	RXD TXD $\overline{INT0}$ INT1 T0 T1 $\overline{WR}$ $\overline{RD}$
P4.7:0	I/O	**Port 4** P4 is an 8-bit bidirectional I/O port with internal pull-ups.	MISO MOSI SCK $\overline{SS}$
P5.3:0	I/O	**Port 5** P5 is a 4-bit bidirectional I/O port with internal pull-ups.	-

Table 2. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
FILT	I	**PLL Low Pass Filter input** FILT receives the RC network of the PLL low pass filter.	-

Table 3. Timer 0 and Timer 1 Signal Description

Signal Name	Type	Description	Alternate Function
$\overline{INT0}$	I	**Timer 0 Gate Input** $\overline{INT0}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{INT0}$ input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bit IE0 is set by a low level on $\overline{INT0}$.	P3.2
$\overline{INT1}$	I	**Timer 1 Gate Input** $\overline{INT1}$ serves as external run control for timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{INT1}$ input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bit IE1 is set by a low level on $\overline{INT1}$.	P3.3

Signal Name	Type	Description	Alternate Function
T0	I	**Timer 0 External Clock Input** When timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer 1 External Clock Input** When timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5

Table 4. Audio Interface Signal Description

Signal Name	Type	Description	Alternate Function
DCLK	O	**DAC Data Bit Clock**	-
DOUT	O	**DAC Audio Data**	-
DSEL	O	**DAC Channel Select Signal** DSEL is the sample rate clock output.	-
SCLK	O	**DAC System Clock** SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL).	-

Table 5. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 KΩ pull-up to V_{DD} for full speed operation.	-
D-	I/O	**USB Negative Data Upstream Port**	-

Table 6. MutiMediaCard Interface Signal Description

Signal Name	Type	Description	Alternate Function
MCLK	O	**MMC Clock output** Data or command clock transfer.	-
MCMD	I/O	**MMC Command line** Bidirectional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to V_{DD} or V_{SS}.	-
MDAT	I/O	**MMC Data line** Bidirectional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to V_{DD} or V_{SS}.	-

Table 7. UART Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1

Table 8. SPI Controller Signal Description

Signal Name	Type	Description	Alternate Function
MISO	I/O	**SPI Master Input Slave Output Data Line** When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller.	P4.0
MOSI	I/O	**SPI Master Output Slave Input Data Line** When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller.	P4.1
SCK	I/O	**SPI Clock Line** When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.	P4.2
$\overline{SS}$	I	**SPI Slave Select Line** When in controlled slave mode, $\overline{SS}$ enables the slave mode.	P4.3

Table 9. TWI Controller Signal Description

Signal Name	Type	Description	Alternate Function
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to the slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bidirectional Two Wire data line.	P1.7

Table 10. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AVSS.	-

Figure 5-2. AT8xC51SND1C Typical Application with On-Board Atmel DataFlash and // LCD

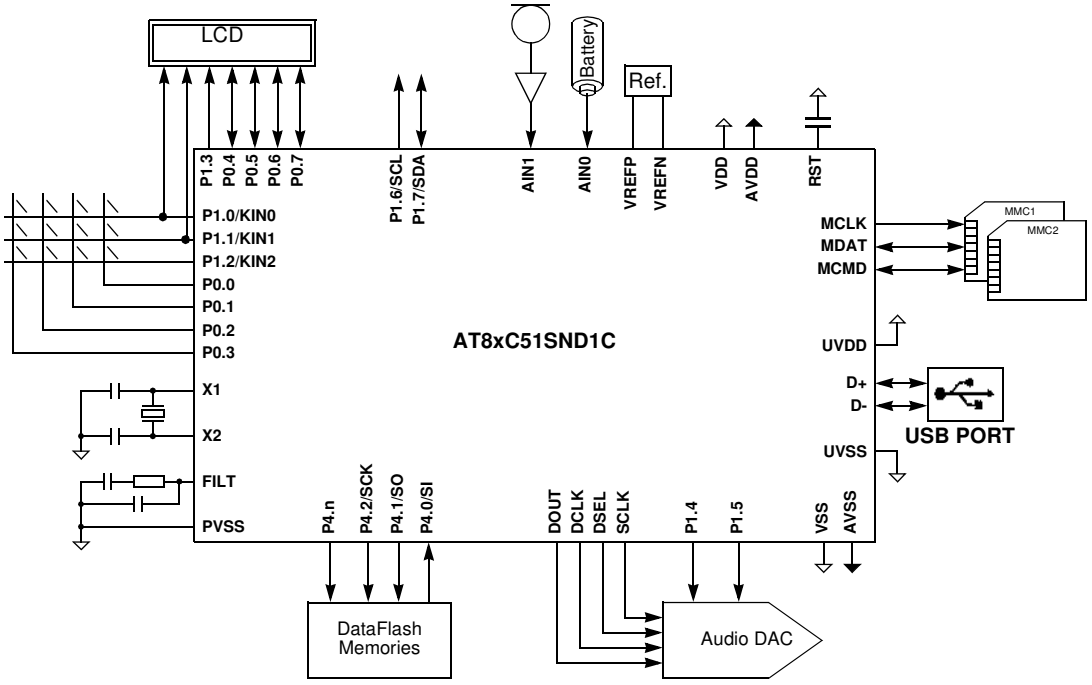


Figure 5-3. AT8xC51SND1C Typical Application with On-Board SSFDC Flash

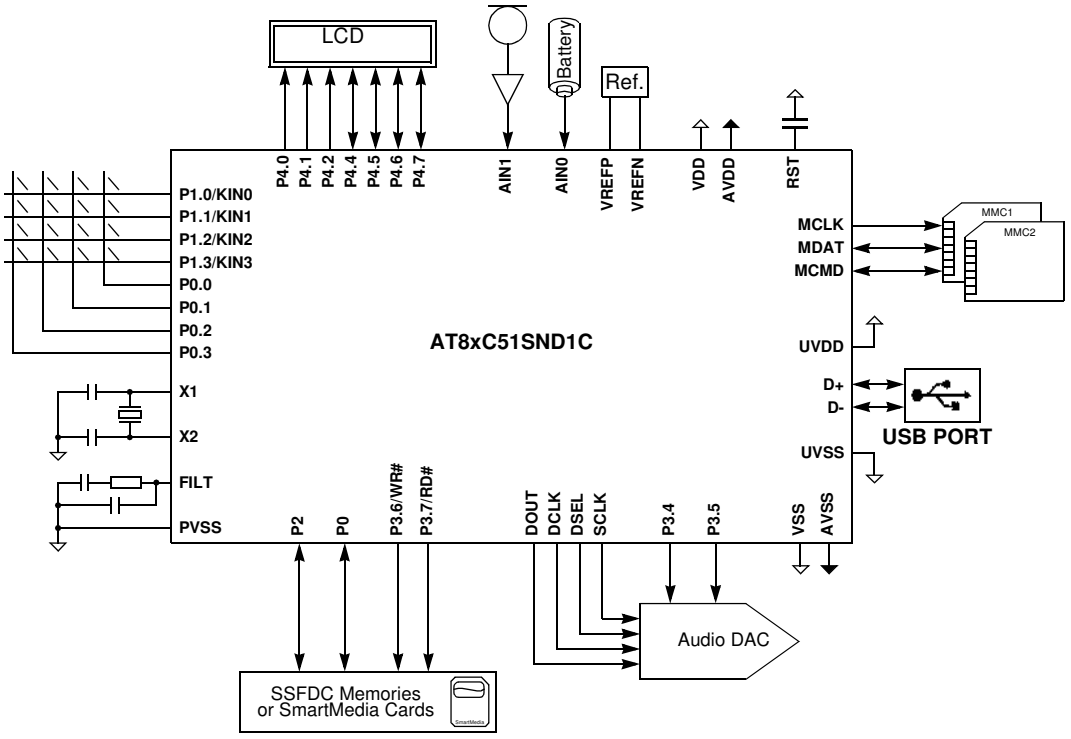
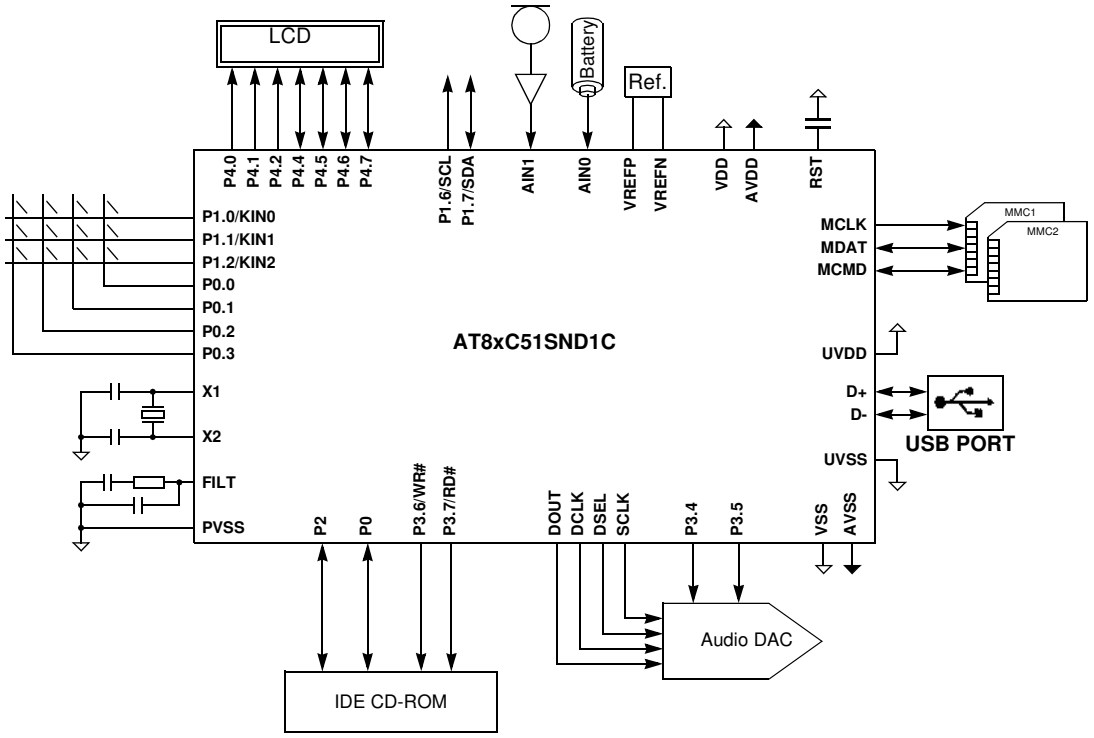


Figure 5-4. AT8xC51SND1C Typical Application with IDE CD-ROM Drive



6. Peripherals

The AT8xC51SND1C peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the AT8xC51SND1C design guide.

6.1 Clock Generator System

The AT8xC51SND1C internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the MP3 decoder, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The MP3 decoder clock is generated by dividing the PLL output clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

6.2 Ports

The AT8xC51SND1C implements five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/O, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/O and alternate functions.

6.3 Timers/Counters

The AT8xC51SND1C implements the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

6.4 Watchdog Timer

The AT8xC51SND1C implements a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

6.5 MP3 Decoder

The AT8xC51SND1C implements a MPEG I/II audio layer 3 decoder (known as MP3 decoder).
In MPEG I (ISO 11172-3) three layers of compression have been standardized supporting three sampling frequencies: 48, 44.1, and 32 KHz. Among these layers, layer 3 allows highest compression rate of about 12:1 while still maintaining CD audio quality. For example, 3 minutes of CD audio (16-bit PCM, 44.1 KHz) data, which needs about 32 MBytes of storage, can be encoded into only 2.7 MBytes of MPEG I audio layer 3 data.
In MPEG II (ISO 13818-3), three additional sampling frequencies: 24, 22.05, and 16 KHz are supported for low bit rates applications.
The AT8xC51SND1C can decode in real-time the MPEG I audio layer 3 encoded data into a PCM audio data, and also supports MPEG II audio layer 3 additional frequencies.

Additional features are supported by the AT8xC51SND1C MP3 decoder such as volume, bass, medium, and treble controls, bass boost effect and ancillary data extraction.

6.6 Audio Output Interface

The AT8xC51SND1C implements an audio output interface allowing the decoded audio bit-stream to be output in various formats. It is compatible with right and left justification PCM and I^2S formats and thanks to the on-chip PLL (see Section 6.1) allows connection of almost all of the commercial audio DAC families available on the market.

6.7 Universal Serial Bus Interface

The AT8xC51SND1C implements a full speed Universal Serial Bus Interface. It can be used for the following purposes:

- Download of MP3 encoded audio files by supporting the USB mass storage class.
- In System Programming by supporting the USB firmware upgrade class.

6.8 MultiMediaCard Interface

The AT8xC51SND1C implements a MultiMediaCard (MMC) interface compliant to the V2.2 specification in MultiMediaCard Mode. The MMC allows storage of MP3 encoded audio files in removable flash memory cards that can be easily plugged or removed from the application. It can also be used for In System Programming.

6.9 IDE/ATAPI interface

The AT8xC51SND1C provides an IDE/ATAPI interface allowing connexion of devices such as CD-ROM reader, CompactFlash cards, Hard Disk Drive… It consists in a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In System Programming using CD-ROM.

6.10 Serial I/O Interface

The AT8xC51SND1C implements a serial port with its own baud rate generator providing one single synchronous communication mode and three full-duplex Universal Asynchronous Receiver Transmitter (UART) communication modes. It is provided for the following purposes:

- In System Programming.
- Remote control of the AT8xC51SND1C by a host.

6.11 Serial Peripheral Interface

The AT8xC51SND1C implements a Serial Peripheral Interface (SPI) supporting master and slave modes. It is provided for the following purposes:

- Interfacing DataFlash memory for MP3 encoded audio files storage.
- Remote control of the AT8xC51SND1C by a host.
- In System Programming.

6.12 2-wire Controller

The AT8xC51SND1C implements a 2-wire controller supporting the four standard master and slave modes with multimaster capability. It is provided for the following purposes:

- Connection of slave devices like LCD controller, audio DAC…
- Remote control of the AT8xC51SND1C by a host.
- In System Programming.

6.13 A/D Controller

The AT8xC51SND1C implements a 2-channel 10-bit (8 true bits) analog to digital converter (ADC). It is provided for the following purposes:

- Battery monitoring.
- Voice recording.
- Corded remote control.

6.14 Keyboard Interface

The AT8xC51SND1C implements a keyboard interface allowing connection of 4 x n matrix keyboard. It is based on 4 inputs with programmable interrupt capability on both high or low level. These inputs are available as alternate function of P1.3:0 and allow exit from idle and power down modes.

7. Electrical Characteristics

7.1 Absolute Maximum Rating

Storage Temperature ..... -65 to +150°C Voltage on any other Pin to V_{SS} ..... -0.3 to +4.0 V I_{OL} per I/O Pin ..... 5 mA Power Dissipation ..... 1 W Operating Conditions Ambient Temperature Under Bias..... -40 to +85°C V_{DD} 4.0V	*NOTICE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

7.2 DC Characteristics

7.2.1 Digital Logic

Table 16. Digital DC Characteristics
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IH1}(2)	Input High Voltage (except RST, X1)	$0.2 \cdot V_{DD}$ + 1.1		V_{DD}	V	
V_{IH2}	Input High Voltage (RST, X1)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL1}	Output Low Voltage (except P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL}= 1.6 mA
V_{OL2}	Output Low Voltage (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL}= 3.2 mA
V_{OH1}	Output High Voltage (P1, P2, P3, P4 and P5)	V_{DD} - 0.7			V	I_{OH}= -30 µA
V_{OH2}	Output High Voltage (P0, P2 address mode, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT, D+, D-)	V_{DD} - 0.7			V	I_{OH}= -3.2 mA
I_{IL}	Logical 0 Input Current (P1, P2, P3, P4 and P5)			-50	µA	V_{IN}= 0.45 V
I_{LI}	Input Leakage Current (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			10	µA	0.45< V_{IN}< V_{DD}
I_{TL}	Logical 1 to 0 Transition Current (P1, P2, P3, P4 and P5)			-650	µA	V_{IN}= 2.0 V
R_{RST}	Pull-Down Resistor	50	90	200	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A= 25°C
V_{RET}	V_{DD} Data Retention Limit			1.8	V	

Table 16. Digital DC Characteristics
V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
I_{DD}	AT89C51SND1C Operating Current		(3)	X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT83SND1C Operating Current			X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT80C51SND1C Idle Mode Current			X1 / X2 mode 6.5 / 10.5 8 / 13.5 9.5 / 17	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{DL}	AT89C51SND1C Idle Mode Current		(3)	X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT83SND1C Idle Mode Current			X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
	AT80C51SND1C Idle Mode Current			X1 / X2 mode 5.3 / 8.1 6.4 / 10.3 7.5 / 13	mA	V_{DD} < 3.3 V 12 MHz 16 MHz 20 MHz
I_{PD}	AT89C51SND1C Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V
	AT83SND1C Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V
	AT80C51SND1C Power-Down Mode Current		20	500	µA	V_{RET} < V_{DD} < 3.3 V
I_{FP}	AT89C51SND1C Flash Programming Current			15	mA	V_{DD} < 3.3 V

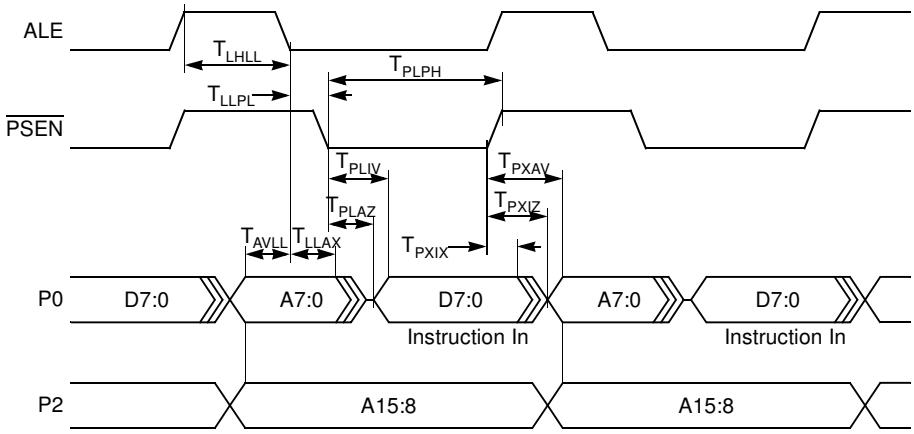
Notes:
1. Typical values are obtained using V_{DD}= 3 V and T_A= 25°C. They are not tested and there is no guarantee on these values.
2. Flash retention is guaranteed with the same formula for V_{DD} min down to 0V.
3. See Table 17 for typical consumption in player mode.

Table 17. Typical Reference Design AT89C51SND1C Power Consumption

Player Mode	I_{DD}	Test Conditions
Stop	10 mA	AT89C51SND1C at 16 MHz, X2 mode, V_{DD}= 3 V No song playing
Playing	30 mA	AT89C51SND1C at 16 MHz, X2 mode, V_{DD}= 3 V MP3 Song with Fs= 44.1 KHz, at any bit rates (Variable Bit Rate)

7.3.1.3 Waveforms

Figure 7-9. External Program Bus Cycle - Read Waveforms



7.3.2 External Data 8-bit Bus Cycles

7.3.2.1 Definition of Symbols

Table 26. External Data 8-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	$\overline{RD}$
W	$\overline{WR}$

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

7.3.2.2 Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 27. External Data 8-bit Bus Cycle - Read AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLRL}	ALE Low to $\overline{RD}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{RHLH}	$\overline{RD}$ high to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}-65$		$4.5 \cdot T_{CLCL}-65$	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}-30$		$2.5 \cdot T_{CLCL}-30$	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Data Float After $\overline{RD}$ High		$2 \cdot T_{CLCL}-25$		$T_{CLCL}-25$	ns

Table 28. External Data 8-bit Bus Cycle - Write AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}-30$		$1.5 \cdot T_{CLCL}-30$		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}-20$		$3.5 \cdot T_{CLCL}-20$		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	$T_{CLCL}-15$		$0.5 \cdot T_{CLCL}-15$		ns

7.4.0.5 Timings

Test conditions: capacitive load on all pins= 50 pF.

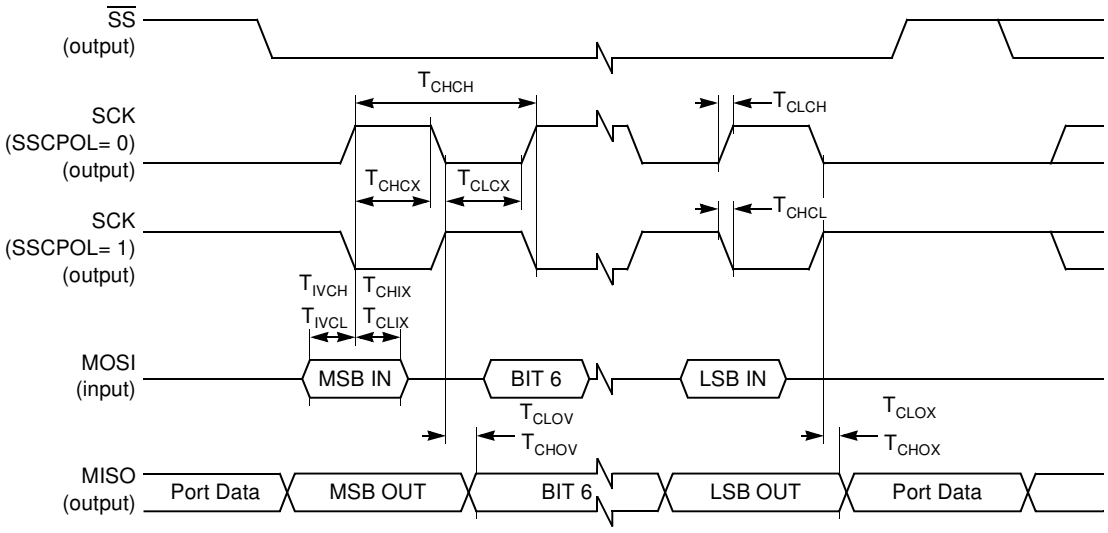
Table 33. SPI Interface Master AC Timing

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode				
T_{CHCH}	Clock Period	2		T_{PER}
T_{CHCX}	Clock High Time	0.8		T_{PER}
T_{CLCX}	Clock Low Time	0.8		T_{PER}
T_{SLCH}, T_{SLCL}	$\overline{SS}$ Low to Clock edge	100		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	40		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	40		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		40	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	$\overline{SS}$ High after Clock Edge	0		ns
T_{SLOV}	$\overline{SS}$ Low to Output Data Valid		50	ns
T_{SHOX}	Output Data Hold after $\overline{SS}$ High		50	ns
T_{SHSL}	$\overline{SS}$ High to $\overline{SS}$ Low	(1)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode				
T_{CHCH}	Clock Period	2		T_{PER}
T_{CHCX}	Clock High Time	0.8		T_{PER}
T_{CLCX}	Clock Low Time	0.8		T_{PER}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	20		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	20		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		40	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

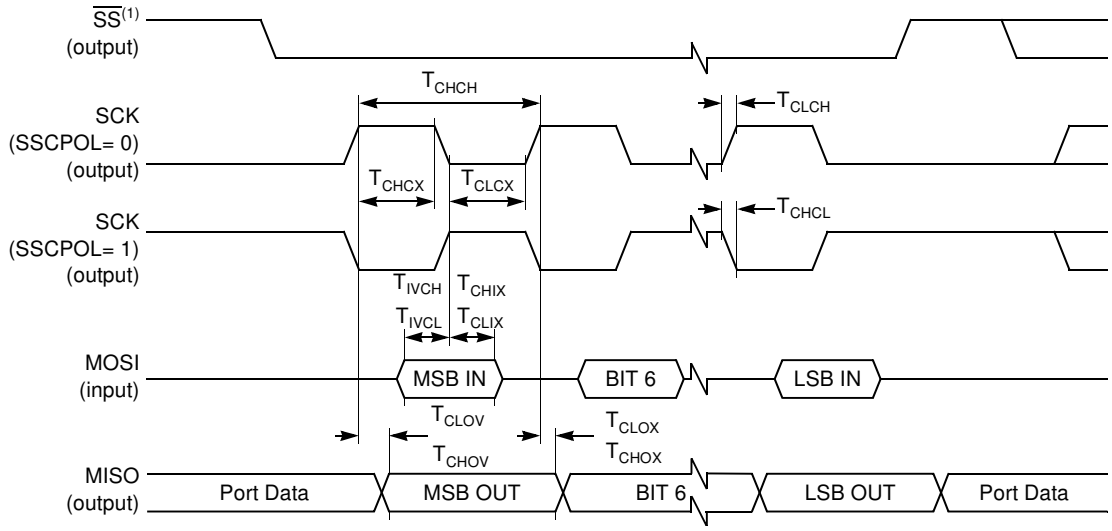
Note: 1. Value of this parameter depends on software.

Figure 7-16. SPI Master Waveforms (SSCPHA= 0)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Figure 7-17. SPI Master Waveforms (SSCPHA= 1)



Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

7.4.1 Two-wire Interface

7.4.1.1 Timings

Table 34. TWI Interface AC Timing

7.4.2 MMC Interface

7.4.2.1 *Definition of symbols*

Table 35. MMC Interface Timing Symbol Definitions

Signals	
C	Clock
D	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

7.4.2.2 *Timings*

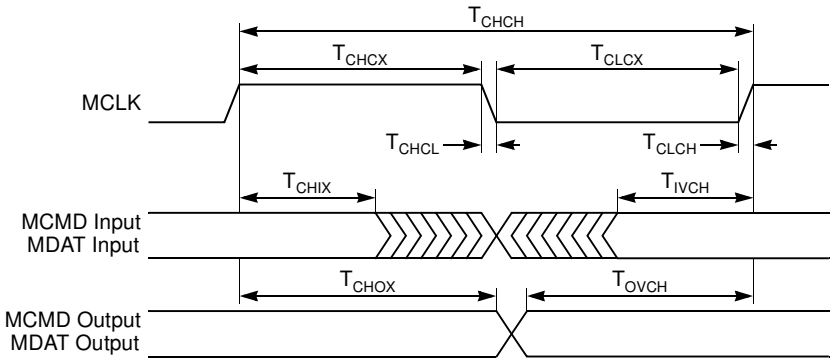
Table 36. MMC Interface AC timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C, CL ≤ 100pF (10 cards)

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period	50		ns
T_{CHCX}	Clock High Time	10		ns
T_{CLCX}	Clock Low Time	10		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{DVCH}	Input Data Valid to Clock High	3		ns
T_{CHDX}	Input Data Hold after Clock High	3		ns
T_{CHOX}	Output Data Hold after Clock High	5		ns
T_{OVCH}	Output Data Valid to Clock High	5		ns

7.4.2.3 *Waveforms*

Figure 7-19. MMC Input-Output Waveforms



7.4.4.3 Waveforms

Figure 7-21. Analog to Digital Converter Internal Waveforms

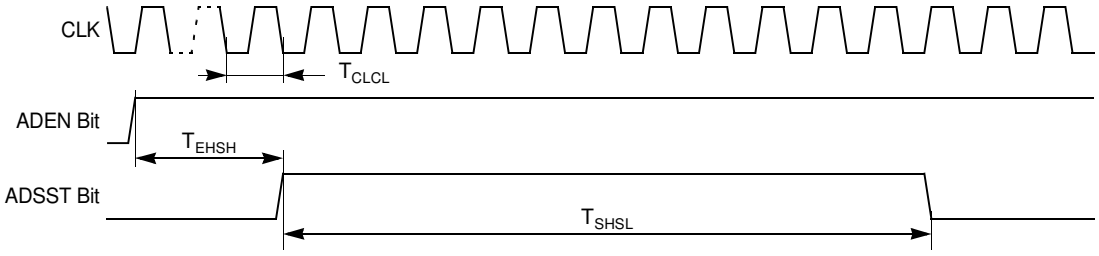
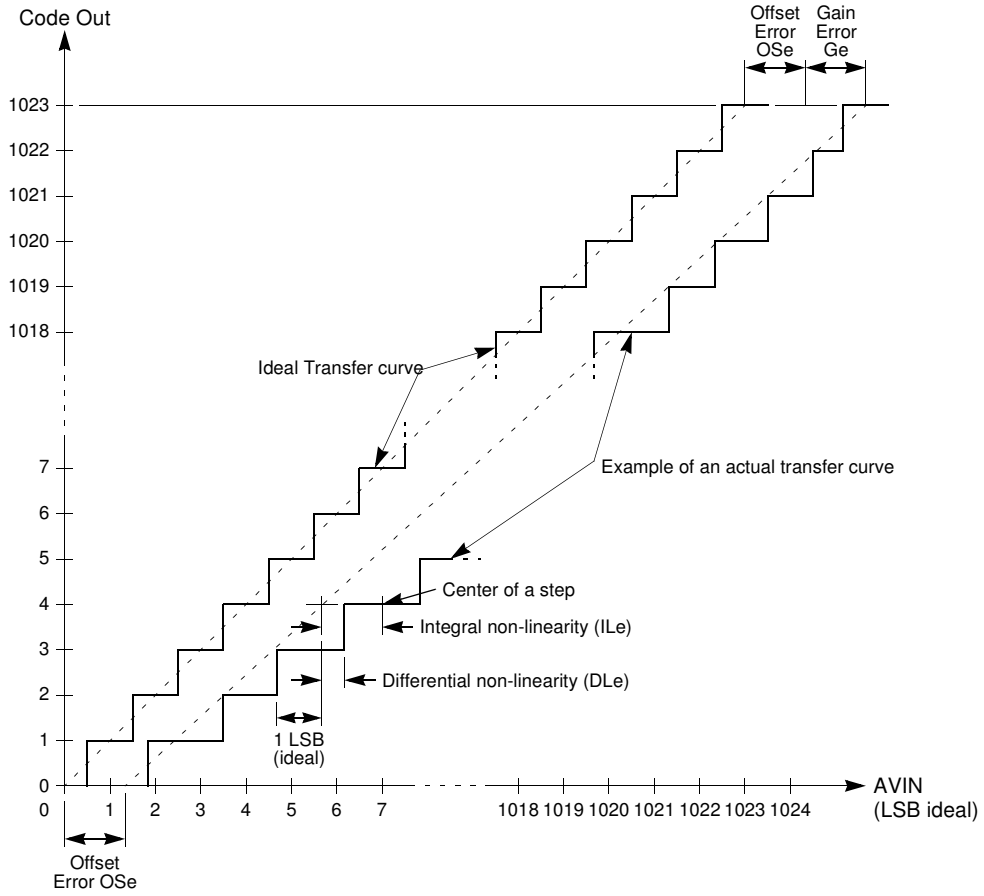


Figure 7-22. Analog to Digital Converter Characteristics



7.4.5 Flash Memory

7.4.5.1 Definition of symbols

Table 41. Flash Memory Timing Symbol Definitions

Signals	
S	$\overline{ISP}$
R	RST
B	FBUSY flag

Conditions	
L	Low
V	Valid
X	No Longer Valid

7.4.5.2 Timings

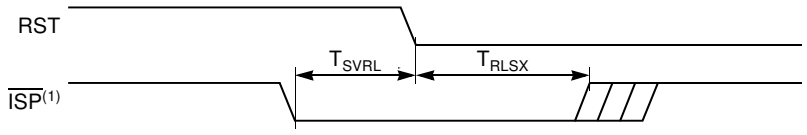
Table 42. Flash Memory AC Timing

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
T_{SVRL}	Input $\overline{ISP}$ Valid to RST Edge	50			ns
T_{RLSX}	Input $\overline{ISP}$ Hold after RST Edge	50			ns
T_{BHBL}	FLASH Internal Busy (Programming) Time		10		ms
N_{FCY}	Number of Flash Write Cycles	100K			Cycle
T_{FDR}	Flash Data Retention Time	10			Years

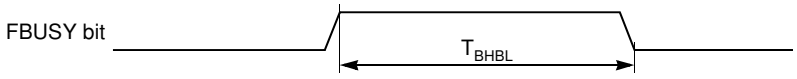
7.4.5.3 Waveforms

Figure 7-23. FLASH Memory - ISP Waveforms



Note: 1. $\overline{ISP}$ must be driven through a pull-down resistor (see Section “In System Programming”, page 23).

Figure 7-24. FLASH Memory - Internal Busy Waveforms



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