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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc8221friaafxuma1

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XC822/824

8-Bit Single-Chip Microcontroller

Data Sheet

V1.2 2011-10

Microcontrollers

XC822/824 Data Sheet

Revision History: V1.2 2011-10

Previous Versions: V1.1	
Page	Subjects (major changes since last revision)
Page 3	A new variant (SAK-XC822MT-0FRA) was added in Table 2.
Page 19	Added a new chip identification number for variant (SAK-XC822MT-0FRA) in Table 5.

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mcdocu.comments@infineon.com

1 Summary of Features

The XC822/824 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM, Library ROM and User routines
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 2/4 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 2.5 V - 5.5 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

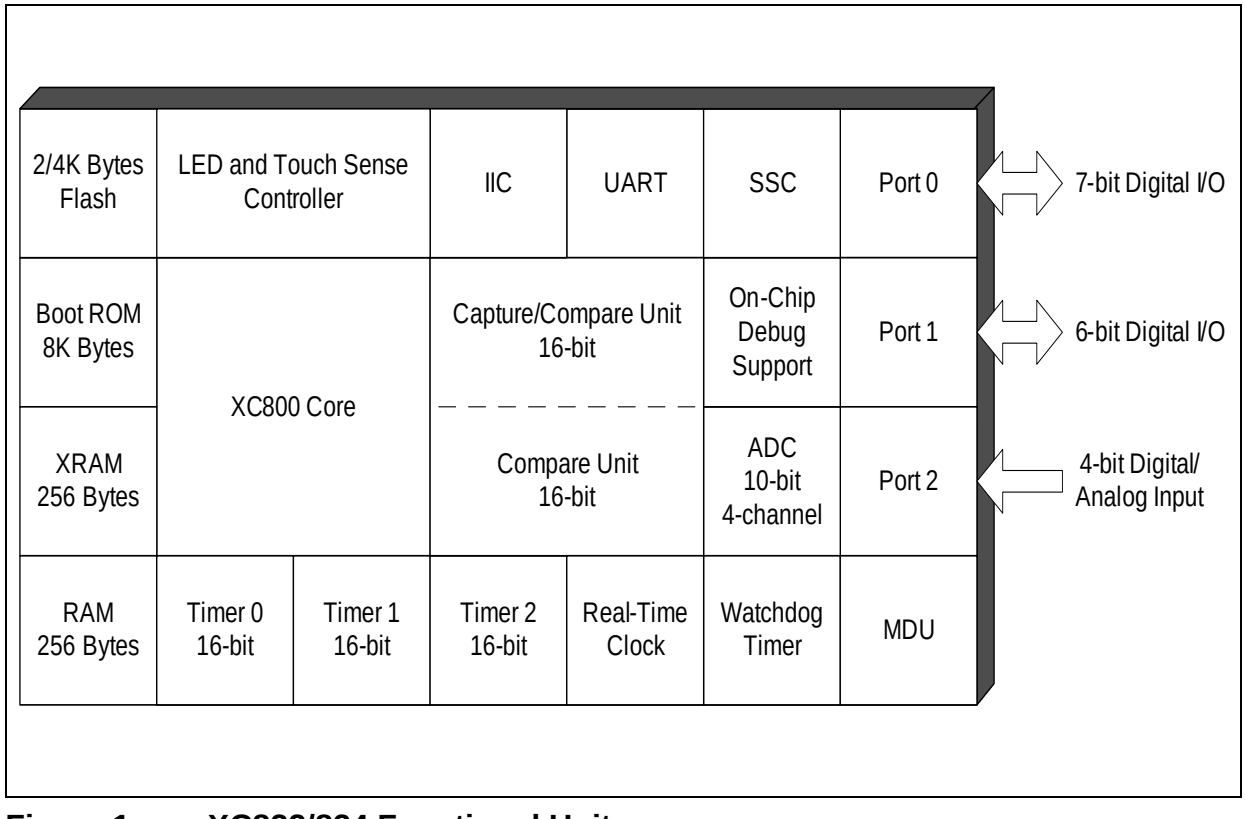


Figure 1 XC822/824 Functional Units

- Power-on reset generation
- Brownout detection for IO supply and core logic supply
- 48 MHz on-chip OSC for clock generation
  - Loss-of-Clock detection

(more features on next page)

2.3 Pin Configuration

The pin configuration of the XC822 in **Figure 4**.

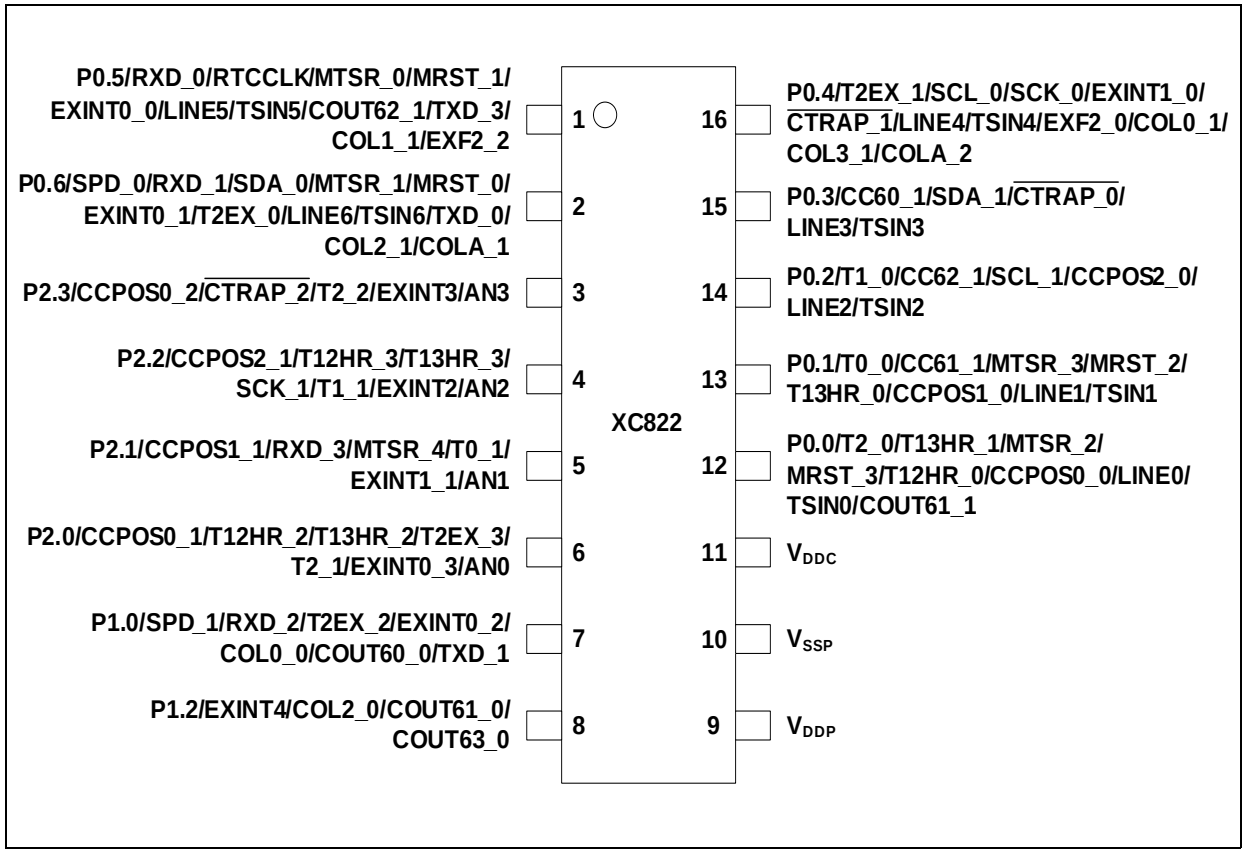


Figure 4 XC822 Pin Configuration, PG-TSSOP-16 Package (top view)

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.1	16/13		Hi-Z	T0_0	Timer 0 Input
				CC61_1	Input/Output of Capture/Compare channel 1
				MTSR_3	SSC Slave Receive Input
				MRST_2	SSC Master Receive Input/ Slave Transmit Output
				T13HR_0	CCU6 Timer 13 Hardware Run Input
				CCPOS1_0	CCU6 Hall Input 1
				TSIN1	Touch-sense Input 1
				LINE1	LED Line 1
P0.2	17/14		Hi-Z	T1_0	Timer 1 Input
				CC62_1	Input/Output of Capture/Compare channel 2
				SCL_1	IIC Clock Line
				CCPOS2_0	CCU6 Hall Input 2
				TSIN2	Touch-sense Input 2
				LINE2	LED Line 2
P0.3	18/15		Hi-Z	CC60_1	Input/Output of Capture/Compare channel 0
				SDA_1	IIC Data Line
				$\overline{\text{CTRAP\_0}}$	CCU6 Trap Input
				TSIN3	Touch-sense Input 3
				LINE3	LED Line 3

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.6	1/2		PU	SPD_0	SPD Input/Output
				RXD_1	UART Receive Input/ UART BSL Receive Input
				SDA_0	IIC Data Line
				MTSR_1	SSC Slave Receive Input
				MRST_0	SSC Master Receive Input/ Slave Transmit Output
				EXINT0_1	External Interrupt Input 0
				T2EX_0	Timer 2 External Trigger Input
				TSIN6	Touch-sense Input 6
				LINE6	LED Line 6
				TXD_0	UART Transmit Output/ 1-wire UART BSL Transmit Output
				COL2_1	LED Column 2
				COLA_1	LED Column A
P1		I/O		**Port 1** Port 1 is a bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, LEDTSCU, SPD, UART and Timer 2.	
P1.0	8/7		Hi-Z	SPD_1	SPD Input/Output
				RXD_2	UART Receive Input
				T2EX_2	Timer 2 External Trigger Input
				EXINT0_2	External Interrupt Input 0
				COL0_0	LED Column 0
				COUT60_0	Output of Capture/Compare Channel 0
				TXD_1	UART Transmit Output

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P2.3	4/3		Hi-Z	CCPOS0_2	CCU6 Hall Input 0
				$\overline{\text{CTRAP}}$_2	CCU6 Trap Input
				T2_2	Timer 2 Input
				EXINT3	External Interrupt Input 3
				AN3	Analog Input 3 / Out of range comparator channel 3
V_{DDP}	12/9	–		I/O Port Supply (2.5 V - 5.5 V)	
V_{DDC}	14/11	–		Core Supply Output (2.5 V)	
V_{SSP}/ V_{SSC}	13/10	–		I/O Port Ground/ Core Supply Ground	

2.5 Memory Organization

The XC822/824 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM, Library ROM and User routines
- 256 bytes of internal RAM
- 256 bytes of XRAM
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 2/4 Kbytes of Flash

Figure 6 illustrates the memory address spaces of the 2 Kbyte Flash devices. There are two 1-Kbyte sectors in this device. **Figure 7** illustrates the memory address spaces of the 4 Kbyte Flash devices. This device has two 1-Kbyte sectors, two 512-byte sectors, two 256-byte sectors and four 128-byte sectors. **Figure 8** shows the Flash sectorization for 2 Kbyte and 4 Kbyte Flash devices.

3 Electrical Parameters

Chapter 3 provides the characteristics of the electrical parameters which are implementation-specific for the XC822/824.

3.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 3.2** and **Section 3.3**.

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC822/824 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  - These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC822/824 and must be regarded for a system design.
- **SR**
  - These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC822/824 is designed in.

3.2.3 ADC Characteristics

The values in **Table 10** are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performances. In the reduced voltage mode (2.5 V < V_{DDP} < 3 V), the ADC is not recommended to be used.

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog reference voltage	V_{AREF}		–	V_{DDP}	–	V	Connect internally to V_{DDP}
Analog reference ground	V_{AGND}		–	V_{SSP}	–	V	Connect internally to V_{SSP}
Alternate analog reference ground	$V_{AGNDALT}$	SR	V_{SSP} - 0.1	–	2.5[1]	V	Connect to AN0 in differential mode, See **Figure 10**.
Internal voltage reference	V_{INTREF}	SR	1.19	1.23	1.28	V	[3]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	–
ADC clock	f_{ADCI}		8	–	16	MHz	internal analog clock
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	–
Conversion time	t_C	CC	See **Section 3.2.3.1**			µs	–
Total unadjusted error	*TUE*[2]	CC	–	–	±1	LSB8	8-bit conversion with internal reference[3]
			–	–	+4/-1	LSB10	10-bit conversion with internal reference[3][4]
			–	–	+14/-2	LSB12	12-bit conversion using the Low Pass Filter [3]
Differential Nonlinearity	EA_{DNL}	CC	–	–	+1.5/ -1	LSB	10-bit conversion[3]

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Integral Nonlinearity	EA_{INL}	CC	–	–	±1.5	LSB	10-bit conversion[3]
Offset	EA_{OFF}	CC	–	+4	–	LSB	10-bit conversion[3]
Gain	EA_{GAIN}	CC	–	-4	–	LSB	10-bit conversion[3]
Switched capacitance at an analog input	C_{AINSW}	CC	–	2	3	pF	3)5)
Total capacitance at an analog input	C_{AINT}	CC	–	–	12	pF	3)5)
Input resistance of an analog input	R_{AIN}	CC	–	1.5	2	kΩ	3)

1) 1.2 V at V_{DDP} = 3.0 V.

2) TUE is tested at V_{AREF} = V_{DDP} = 5.0 V and CPU clock ($f_{SCLK, CCLK}$) = 8 MHz.

3) Not subject to production test, verified by design/characterization.

4) If a reduced positive reference voltage is used, TUE will increase. If the positive reference is reduced by a factor of K, the TUE will increased by 1/K. Example:K = 0.8, 1/K = 1.25; 1.25 X TUE = 2.5 LSB10.

5) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.

3.2.4 Flash Memory Parameters

The XC822/824 is delivered with all Flash sectors erased (read all zeros).

The data retention time of the XC822/824's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: Flash memory parameters are not subject to production test but verified by design and/or characterization.

Table 12 Flash Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Read access time (per byte)	t_{ACC}	CC	–	125	–	ns	
Programming time (per wordline)	t_{PR}	CC	–	2.2	–	ms	
Erase time (one or more sectors)	t_{ER}	CC	–	120	–	ms	
Flash wait states	$N_{WSFLASH}$	CC	0				CPU clock = 8 MHz
			1				CPU clock = 24 MHz

Table 13 Flash Data Retention and Endurance (Operating Conditions apply)

Retention	Endurance[1)]	Size	Remarks
20 years	1,000 cycles	up to 8 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 13** is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)[1)]

Retention	Endurance[2)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) EEPROM Emulation ROM Library can only be used in the 4 Kbyte Flash variant.

2) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

3.2.5 Power Supply Current

Table 15 provides the characteristics of the power supply current in the XC822/824.

Table 15 Power Consumption Parameters[1) 2)](Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Typ.	Max.		
Active Mode	I_{DDPA}	21	25	mA	5 V / 3.3 V [3)]
		14	18	mA	5 V / 3.3 V [4)]
		–	5	mA	2.5 V[5)]
Idle Mode	I_{DDPI}	16	20	mA	5 V / 3.3 V [6)]
		–	5	mA	2.5 V [5)]
Power Down Mode 1	I_{PDP1}	3	5	µA	T_A = 25 °C[7)]
		–	28	µA	T_A = 85 °C[7)8)9)]
Power Down Mode 2	I_{PDP2}	5	7	µA	T_A = 25 °C[7)]
		–	30	µA	T_A = 85 °C[7)8)]

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V and 3.3 V.

2) The maximum values are measured under worst case conditions (T_A = + 125 °C and V_{DDC} = 5 V) unless stated otherwise.

3) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz (CLKMODE=0).

4) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz (CLKMODE=1).

5) This value is based on the maximum load capacity of EVR during V_{DDP} = 2.5 V. Not subject to production test, verified by design/characterisation.

6) I_{DDPI} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz (CLKMODE=0).

7) I_{PDP1} and I_{PDP2} is measured at 5 V and 3.3 V with: wake-up port is programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

8) Not subject to production test, verified by design/characterisation.

9) I_{PDP1} and I_{PDP2} has a maximum values of 100 uA at T_A = + 125 °C.

3.3.3 Oscillator Timing and Wake-up Timing

Table 19 provides the characteristics of the power-on reset, PLL and Wake-up timings in the XC822/824.

Table 19 Power-On Reset Wake-up Timing[1] (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
48 MHz Oscillator start-up time	$t_{48MOSCST}$	CC	–	–	13	µs	
75 KHz Oscillator start-up time	$t_{75KOSCST}$	CC	–	–	800	µs	
Flash initialization time	t_{FINT}	CC	–	160	–	µs	

1) Not subject to production test, verified by design/characterisation.

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 48 MHz oscillator in the XC822/824.

Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-0.5 %	48	+0.5%	MHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-2.0	–	3.0	%	with respect to f_{NOM}, over lifetime and temperature (0 °C to 85 °C)
			-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation (over core supply voltage[2])	Δf_{ST}	CC	-1	–	1	%	with respect to f_{NOM}, within one LIN message (< 10 ms … 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

2) Core voltage supply, V_{DDC} = 2.5 V ± 7.5%.

Table 21 provides the characteristics of the 75 kHz oscillator in the XC822/824.

Table 21 75 kHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-1%	75	+1%	KHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation	Δf_{ST}	CC	-1.5	–	1.5	%	with respect to f_{NOM}, over core supply voltage of 2.5 V ± 7.5%

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

3.3.5.2 SSC Slave Mode Timing

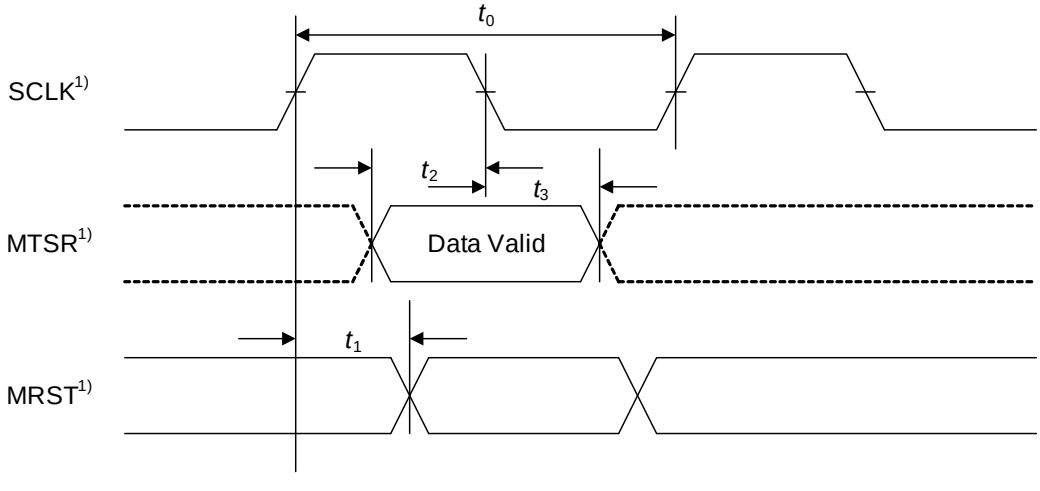
Table 23 provides the SSC slave mode timing in the XC822/824.

Table 23 SSC Slave Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	SR	4 * T_{SSC}[2]	–	ns
MRST delay from SCLK	t_1	CC	0	20	ns
MTSR setup to SCLK	t_2	SR	46	–	ns
MTSR hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 166.7 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup : CON.PH = CON.PO = 0.

Figure 17 SSC Slave Mode Timing

4.2 Package Outline

Figure 18 and **Figure 19** shows the package outlines of the XC822 (TSSOP-16) and XC824 (DSO-20) devices respectively.

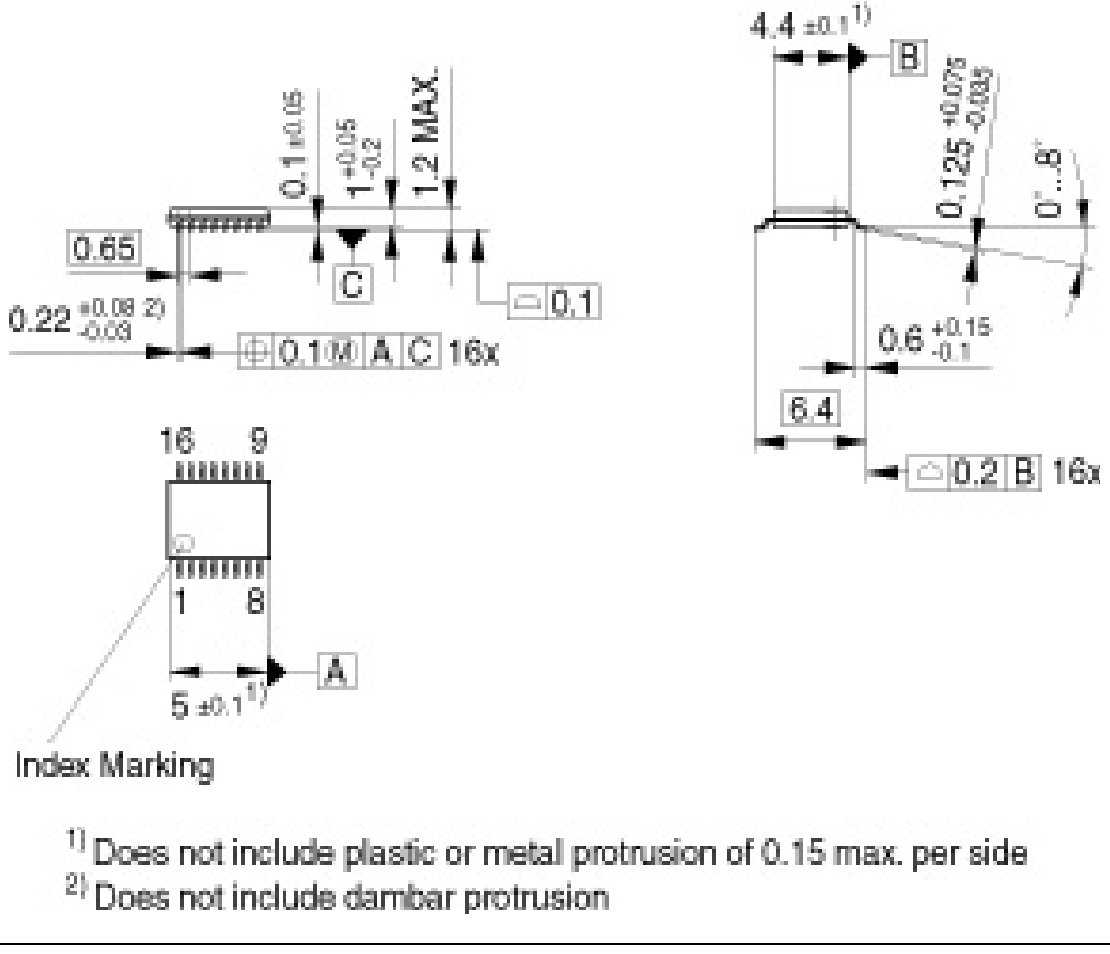


Figure 18 PG-TSSOP-16-1 Package Outline

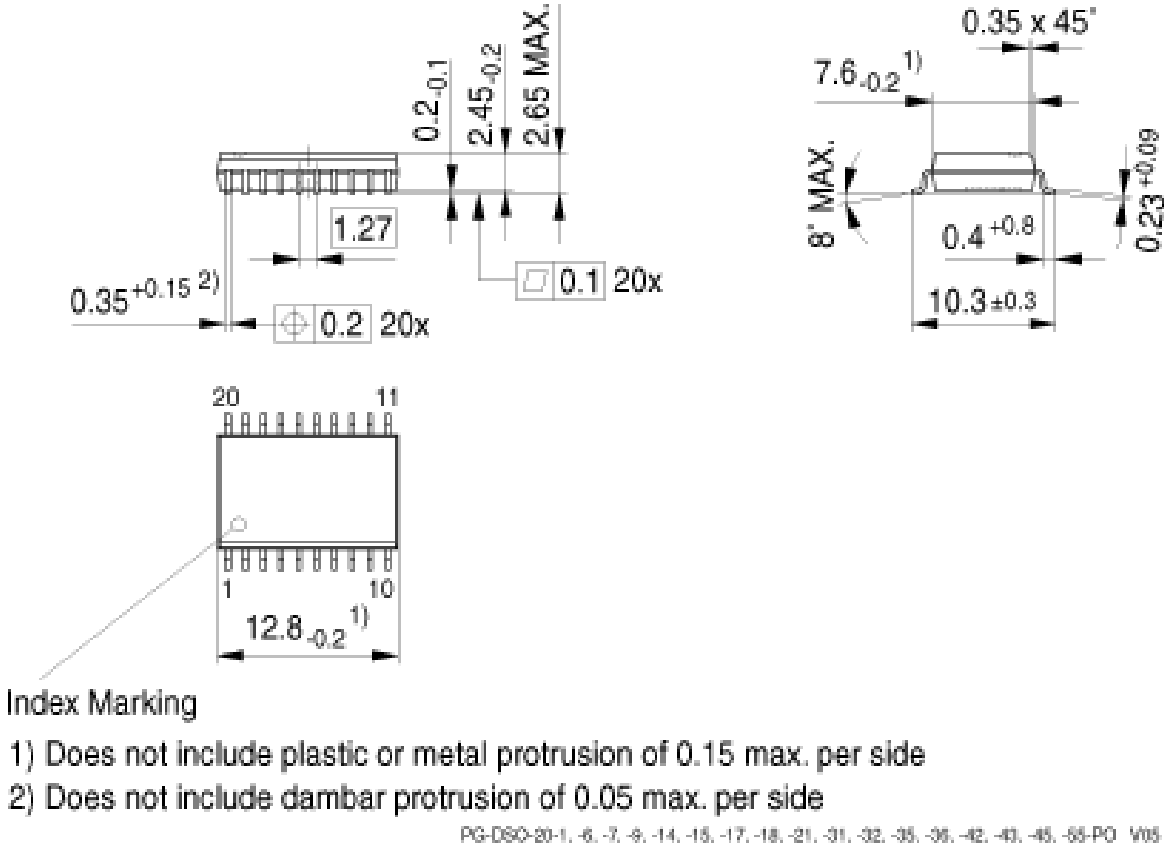


Figure 19 PG-DSO-20-45 Package Outline

4.3 Quality Declaration

Table 25 shows the characteristics of the quality parameters in the XC822/824.

Table 25 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operation Lifetime when the device is used at the three stated T_J [1]	t_{OP1}	-	1500	hours	T_J = 150°C
		-	15000	hours	T_J = 110°C
		-	1500	hours	T_J = -40°C
Operation Lifetime when the device is used at the stated T_J [1]	t_{OP2}	-	131400	hours	T_J = 27°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C

1) This lifetime refers only to the time when device is powered-on.