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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc822m1friaafxuma1

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XC822/824

8-Bit Single-Chip Microcontroller

Data Sheet

V1.2 2011-10

Microcontrollers

XC822/824 Data Sheet

Revision History: V1.2 2011-10

Previous Versions: V1.1	
Page	Subjects (major changes since last revision)
Page 3	A new variant (SAK-XC822MT-0FRA) was added in Table 2.
Page 19	Added a new chip identification number for variant (SAK-XC822MT-0FRA) in Table 5.

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Is there any information in this document that you feel is wrong, unclear or missing? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Features: (continued)

- Power saving modes
  - idle mode
  - power-down mode with wake-up capability via real-time clock interrupt
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT) running on independent oscillator with programmable window feature for refresh operation and warning prior to overflow
- Three ports
  - Up to 17 pins as digital I/O
  - 4 pin as digital/analog input
- 4-channel, 10-bit ADC
  - support up to 3 differential input channel
  - results filtering by data reduction or digital low-pass filter, for up to 13-bit results
- Up to 4 channels, Out of range comparator
- Three 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 (T2)
- Periodic wake-up timer
- Multiplication/Division Unit for arithmetic operations (MDU)
- Capture and Compare unit for PWM signal generation (CCU6)
- A full-duplex or half-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- Inter-IC (IIC) serial interface
- LED and Touch-sense Controller (LEDTSCU)
- On-chip debug support via single pin DAP interface (SPD)
- Packages:
  - PG-DSO-20
  - PG-TSSOP-16
- Temperature range T_A:
  - SAF (-40 to 85 °C)
  - SAX (-40 to 105 °C)
  - SAK (-40 to 125 °C)

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC822/824 throughout this document.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC822/824, please refer to your responsible sales representative or your local distributor.

The pin configuration of the XC824 in **Figure 5**.

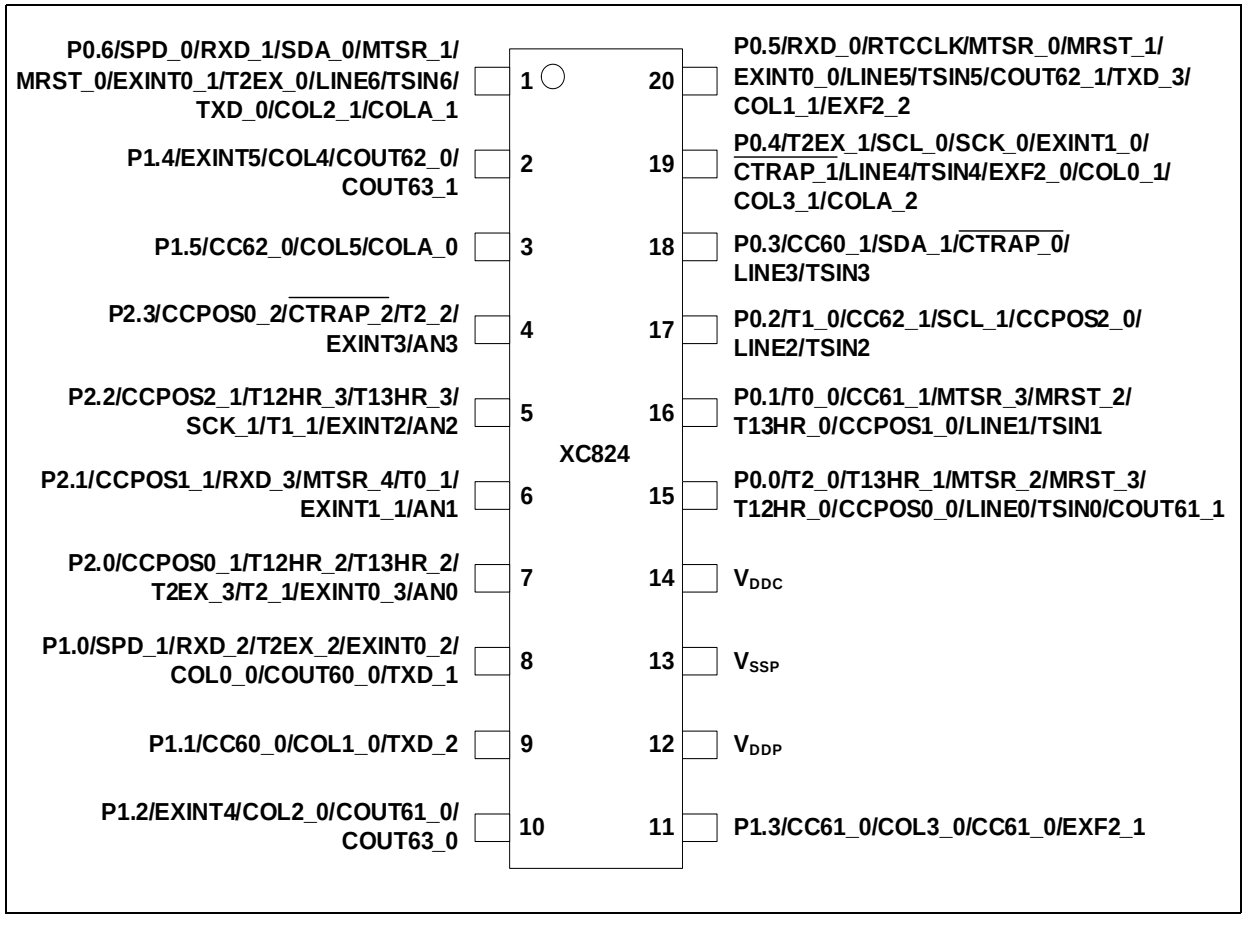


Figure 5 XC824 Pin Configuration, PG-DSO-20 Package (top view)

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.1	16/13		Hi-Z	T0_0	Timer 0 Input
				CC61_1	Input/Output of Capture/Compare channel 1
				MTSR_3	SSC Slave Receive Input
				MRST_2	SSC Master Receive Input/ Slave Transmit Output
				T13HR_0	CCU6 Timer 13 Hardware Run Input
				CCPOS1_0	CCU6 Hall Input 1
				TSIN1	Touch-sense Input 1
				LINE1	LED Line 1
P0.2	17/14		Hi-Z	T1_0	Timer 1 Input
				CC62_1	Input/Output of Capture/Compare channel 2
				SCL_1	IIC Clock Line
				CCPOS2_0	CCU6 Hall Input 2
				TSIN2	Touch-sense Input 2
				LINE2	LED Line 2
P0.3	18/15		Hi-Z	CC60_1	Input/Output of Capture/Compare channel 0
				SDA_1	IIC Data Line
				$\overline{\text{CTRAP\_0}}$	CCU6 Trap Input
				TSIN3	Touch-sense Input 3
				LINE3	LED Line 3

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.4	19/16		PD	T2EX_1	Timer 2 External Trigger Input
				SCK_0	SSC Clock Input/Output
				SCL_0	IIC Clock Line
				$\overline{\text{CTRAP}}$_1	CCU6 Trap Input
				EXINT1_0	External Interrupt Input 1
				TSIN4	Touch-sense Input 4
				LINE4	LED Line 4
				EXF2_0	Timer 2 Overflow Flag
				COL0_1	LED Column 0
				COL3_1	LED Column 3
				COLA_2	LED Column A
P0.5	20/1		Hi-Z	RXD_0	UART Receive Input
				RTCCLK	RTC External Clock Input
				MTSR_0	SSC Master Transmit Output/ Slave Receive Input
				MRST_1	SSC Master Receive Input
				EXINT0_0	External Interrupt Input 0
				TSIN5	Touch-sense Input 5
				LINE5	LED Line 5
				COUT62_1	Output of Capture/Compare Channel 2
				TXD_3	UART Transmit Output/ 2-wire UART BSL Transmit Output
				COL1_1	LED Column 1
				EXF2_2	Timer 2 Overflow Flag

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P2.3	4/3		Hi-Z	CCPOS0_2	CCU6 Hall Input 0
				$\overline{\text{CTRAP}}$_2	CCU6 Trap Input
				T2_2	Timer 2 Input
				EXINT3	External Interrupt Input 3
				AN3	Analog Input 3 / Out of range comparator channel 3
V_{DDP}	12/9	–		I/O Port Supply (2.5 V - 5.5 V)	
V_{DDC}	14/11	–		Core Supply Output (2.5 V)	
V_{SSP}/ V_{SSC}	13/10	–		I/O Port Ground/ Core Supply Ground	

2.5 Memory Organization

The XC822/824 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM, Library ROM and User routines
- 256 bytes of internal RAM
- 256 bytes of XRAM
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 2/4 Kbytes of Flash

Figure 6 illustrates the memory address spaces of the 2 Kbyte Flash devices. There are two 1-Kbyte sectors in this device. **Figure 7** illustrates the memory address spaces of the 4 Kbyte Flash devices. This device has two 1-Kbyte sectors, two 512-byte sectors, two 256-byte sectors and four 128-byte sectors. **Figure 8** shows the Flash sectorization for 2 Kbyte and 4 Kbyte Flash devices.

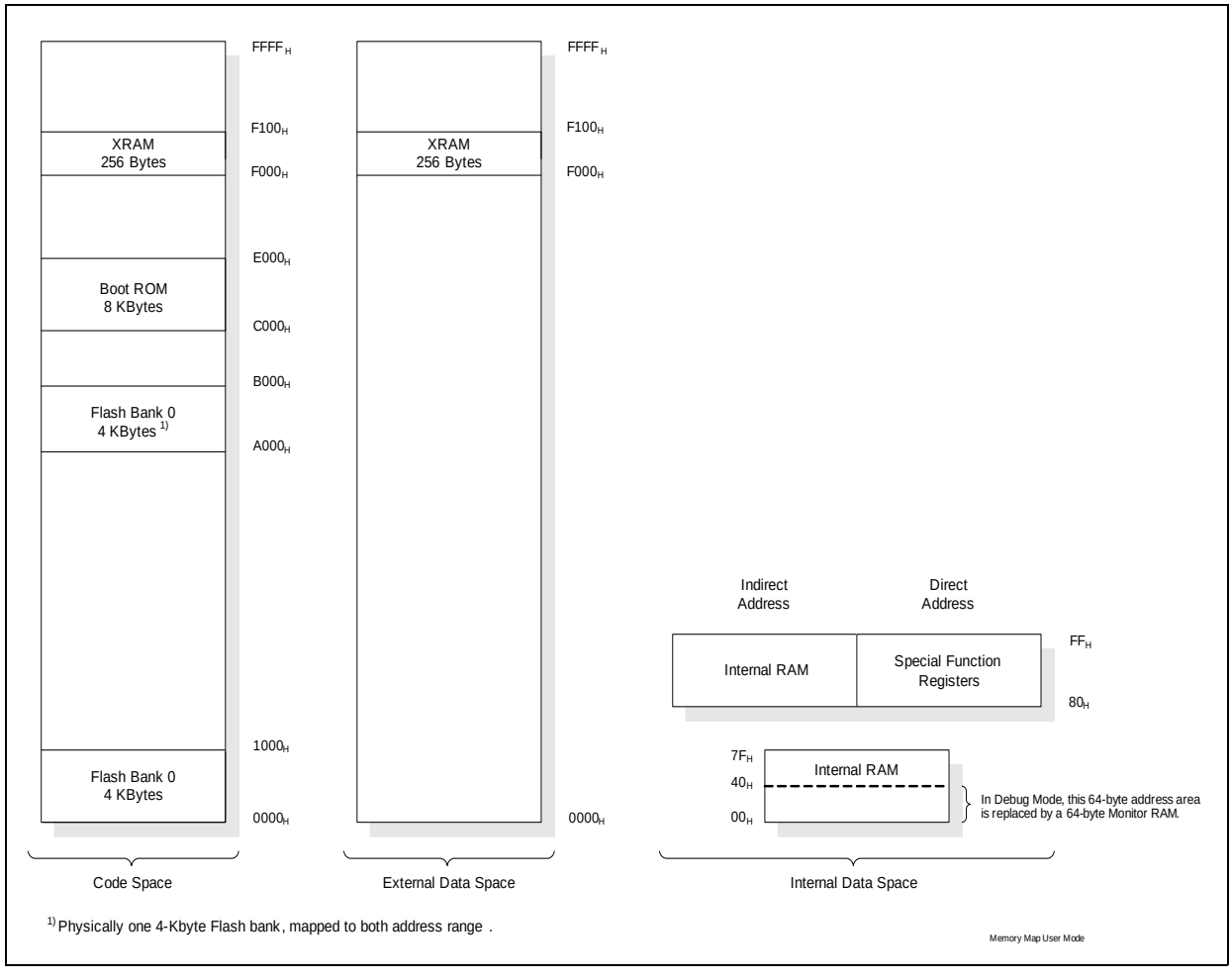


Figure 7 Memory Map of XC822/824 with 4 Kbytes of Flash memory

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC822/824 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

3.2.2 Supply Threshold Characteristics

Table 9 provides the characteristics of the supply threshold in the XC822/824.

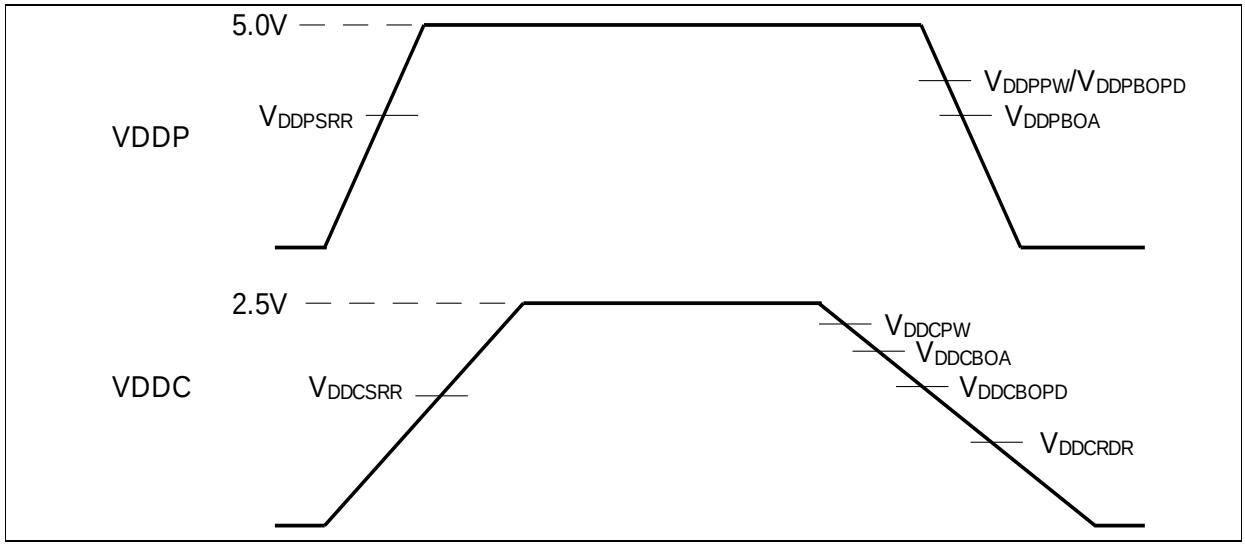


Figure 9 Supply Threshold Parameters

Table 9 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
V_{DDP} prewarning voltage[1)2)]	V_{DDPPW}	CC	3.0	3.6	4.5	V
V_{DDP} brownout voltage in active mode[3)2)]	V_{DDPBOA}	CC	2.65	2.75	2.87	V
V_{DDP} brownout voltage in power down mode[2)3)]	$V_{DDPBOPD}$	CC	3.0	3.6	4.5	V
V_{DDP} system reset release voltage[2)4)]	V_{DDPSRR}	CC	2.7	2.8	2.92	V
V_{DDC} prewarning voltage[2)5)]	V_{DDCPW}	CC	2.3	2.4	2.48	V
V_{DDC} brownout voltage in active mode[2)]	V_{DDCBOA}	CC	2.25	2.3	2.42	V
V_{DDC} brownout voltage in power down mode[2)]	$V_{DDCBOPD}$	CC	1.35	1.5	1.95	V
V_{DDC} system reset release voltage[2)4)]	V_{DDCSRR}	CC	2.28	2.3	2.47	V
RAM data retention voltage	V_{DDCRDR}	CC	1.1	–	–	V

1) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode. Detection should be disabled for V_{DDP} less than maximum of V_{DDPPW}.

2) This parameter has a hysteresis of 50 mV.

3) Detection is enabled via SDCON register. Detection must be disabled for application with V_{DDP} less than the specified values.

4) V_{DDPSRR} and V_{DDCSRR} must be met before the system reset is released.

5) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode.

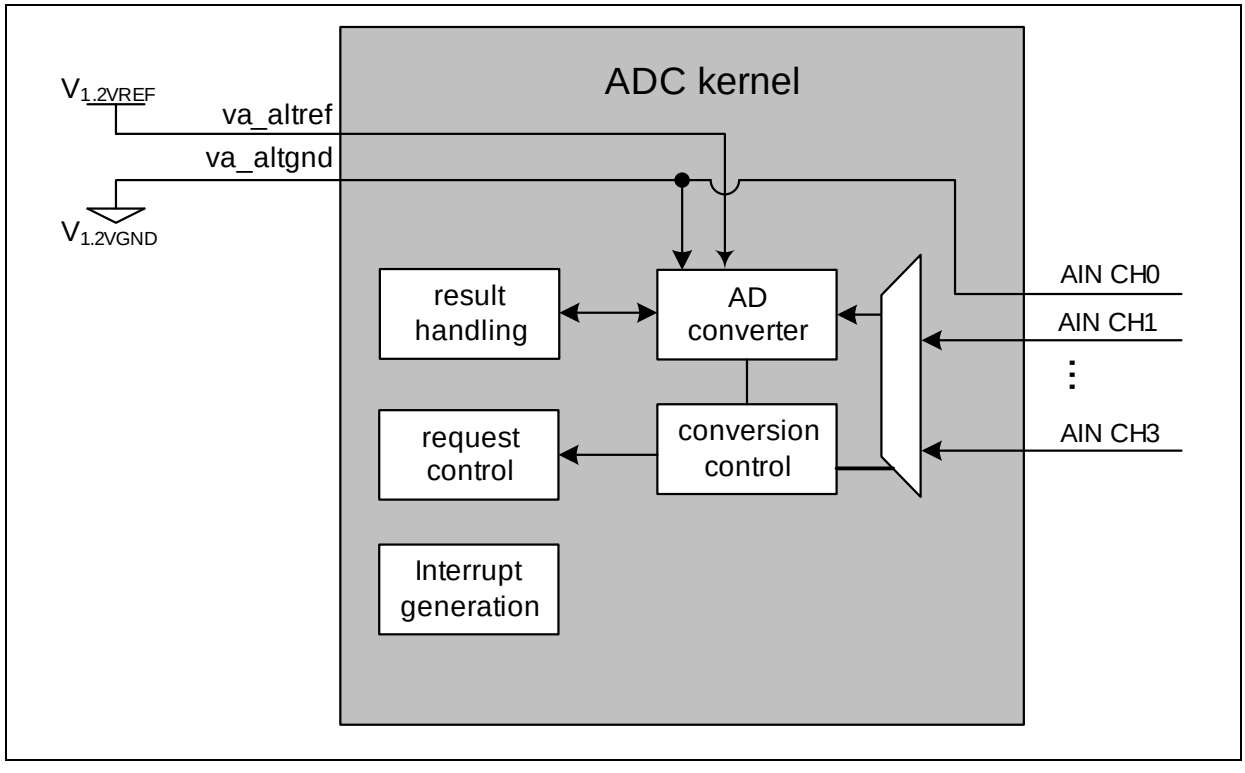


Figure 10 Differential like measurement with internal 1.2V voltage reference, and CH0 gnd.

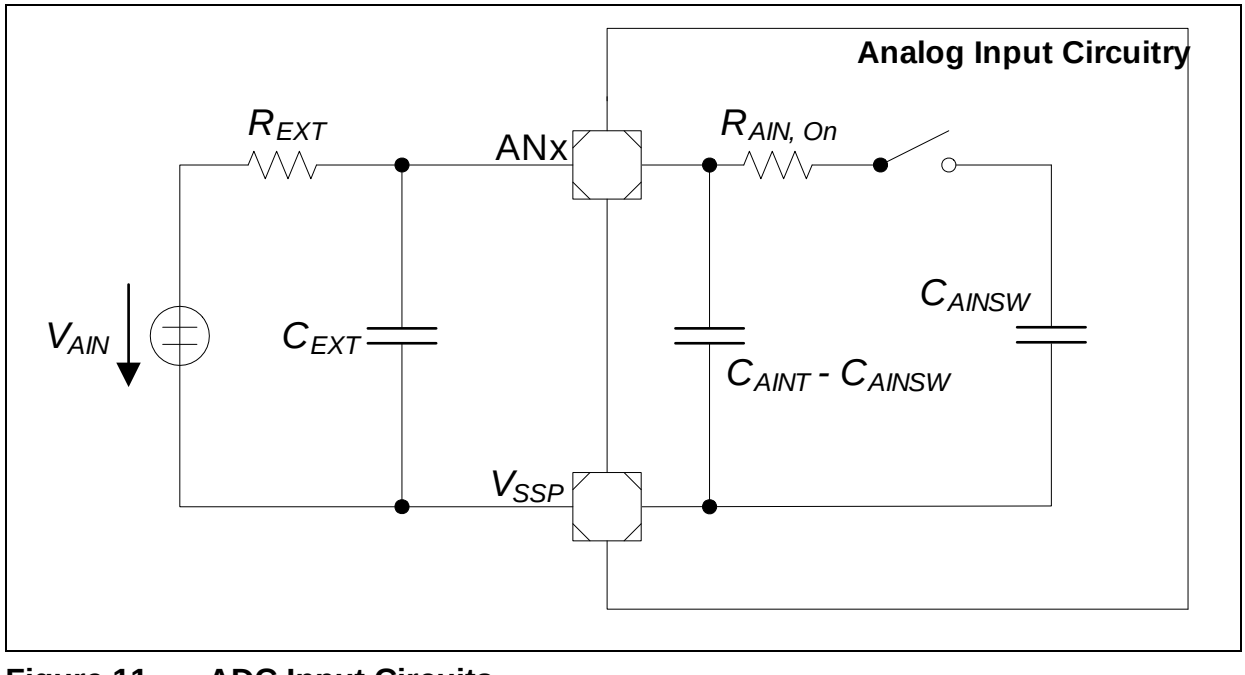


Figure 11 ADC Input Circuits

3.2.3.1 ADC Conversion Timing

Conversion time, $t_C = t_{ADC} \times (1 + r \times (3 + n + STC))$, where

- r = CTC + 3,
- CTC = Conversion Time Control (GLOBCTR.CTC),
- STC = Sample Time Control (INPCR0.STC),
- n = 8 or 10 (for 8-bit and 10-bit conversion respectively),
- $t_{ADC} = 1 / f_{ADC}$

3.2.3.2 Out of Range Comparator Characteristics

Table 11 below shows the Out of Range Comparator characteristics.

Table 11 Out of Range Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
DC Switching Level	$V_{SenseDC}$	SR	60	125	270	mV	Above V_{DDP}
DC Hysteresis	$V_{SenseHys}$	CC	30	–	–	mV	1)
Pulse Width	$t_{SensePW}$	SR	300	–	–	ns	ANx > V_{DDP} 1)
Switching Delay	$t_{SenseSD}$	CC	–	–	400	ns	ANx >= V_{DDP} + 350 mV 1)
Pulse Switching Level	$t_{SensePSL}$	SR	–	250	–	mV	@ 300 nsec 1)
		SR	–	60	–	mV	@ 800 usec 1)

1) Not subject to production test, verified by design/characterization.

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)[1)]

Retention	Endurance[2)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) EEPROM Emulation ROM Library can only be used in the 4 Kbyte Flash variant.

2) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

3.2.5 Power Supply Current

Table 15 provides the characteristics of the power supply current in the XC822/824.

Table 15 Power Consumption Parameters[1) 2)](Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Typ.	Max.		
Active Mode	I_{DDPA}	21	25	mA	5 V / 3.3 V [3)]
		14	18	mA	5 V / 3.3 V [4)]
		–	5	mA	2.5 V[5)]
Idle Mode	I_{DDPI}	16	20	mA	5 V / 3.3 V [6)]
		–	5	mA	2.5 V [5)]
Power Down Mode 1	I_{PDP1}	3	5	µA	T_A = 25 °C[7)]
		–	28	µA	T_A = 85 °C[7)8)9)]
Power Down Mode 2	I_{PDP2}	5	7	µA	T_A = 25 °C[7)]
		–	30	µA	T_A = 85 °C[7)8)]

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V and 3.3 V.

2) The maximum values are measured under worst case conditions (T_A = + 125 °C and V_{DDC} = 5 V) unless stated otherwise.

3) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz (CLKMODE=0).

4) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz (CLKMODE=1).

5) This value is based on the maximum load capacity of EVR during V_{DDP} = 2.5 V. Not subject to production test, verified by design/characterisation.

6) I_{DDPI} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz (CLKMODE=0).

7) I_{PDP1} and I_{PDP2} is measured at 5 V and 3.3 V with: wake-up port is programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

8) Not subject to production test, verified by design/characterisation.

9) I_{PDP1} and I_{PDP2} has a maximum values of 100 uA at T_A = + 125 °C.

3.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

3.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 12**, **Figure 13** and **Figure 14**.

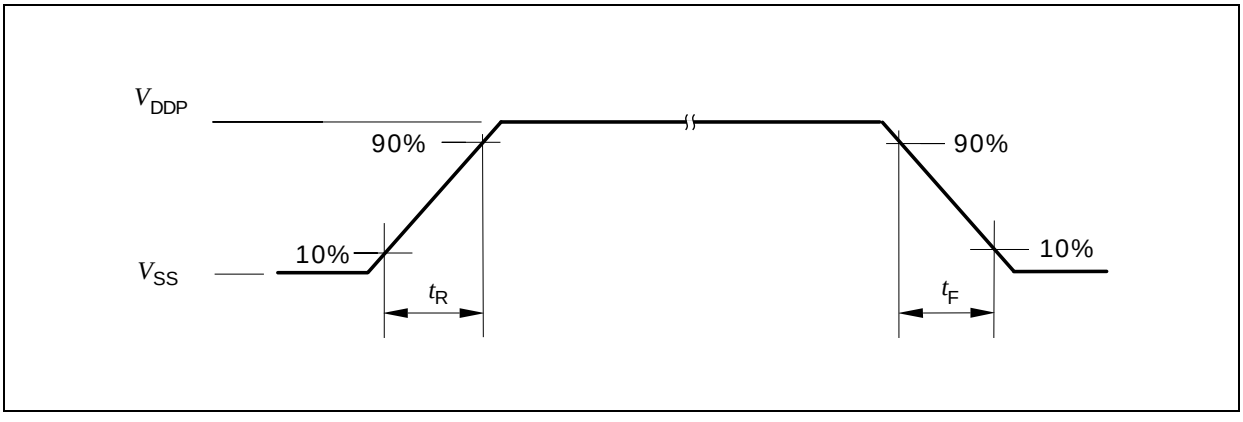


Figure 12 Rise/Fall Time Parameters

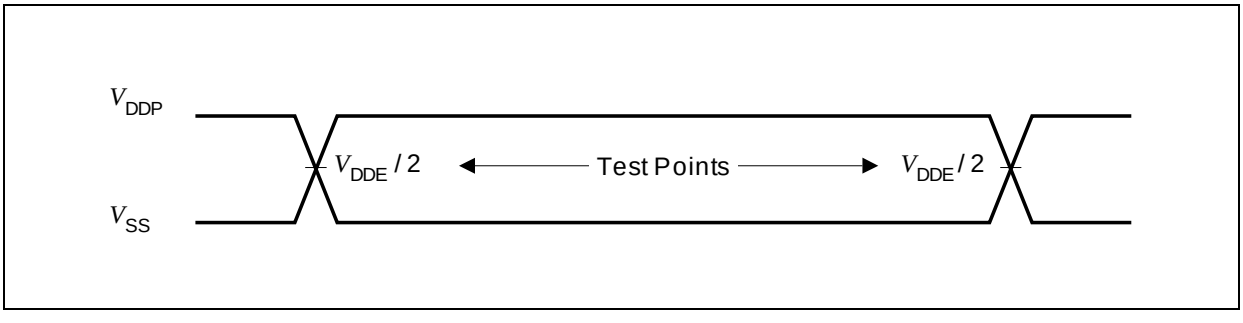


Figure 13 Testing Waveform, Output Delay

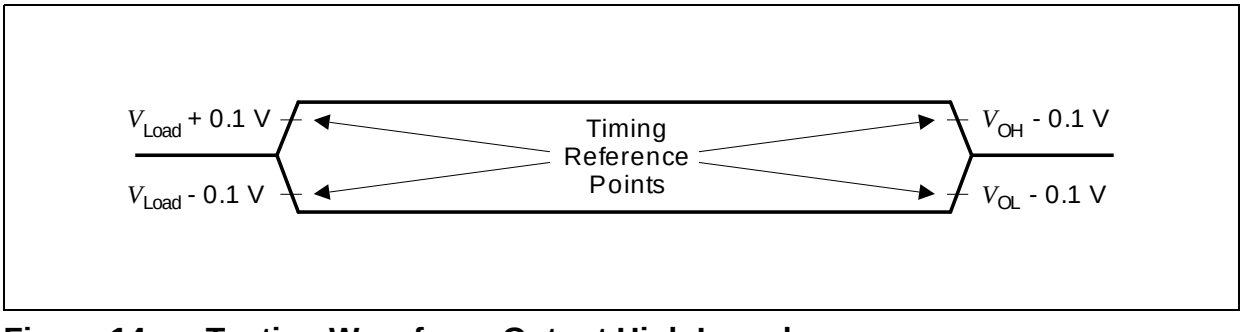


Figure 14 Testing Waveform, Output High Impedance

3.3.5 SSC Timing

3.3.5.1 SSC Master Mode Timing

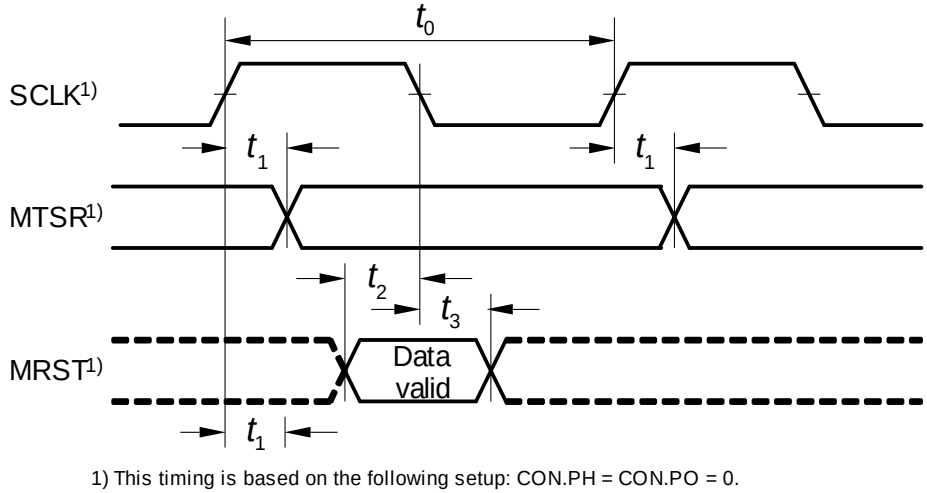
Table 22 provides the SSC master mode timing in the XC822/824.

Table 22 SSC Master Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	CC	2 * T_{SSC}[2]	–	ns
MTSR delay from SCLK	t_1	CC	0	6	ns
MRST setup to SCLK	t_2	SR	20	–	ns
MRST hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_Tmg1

Figure 16 SSC Master Mode Timing

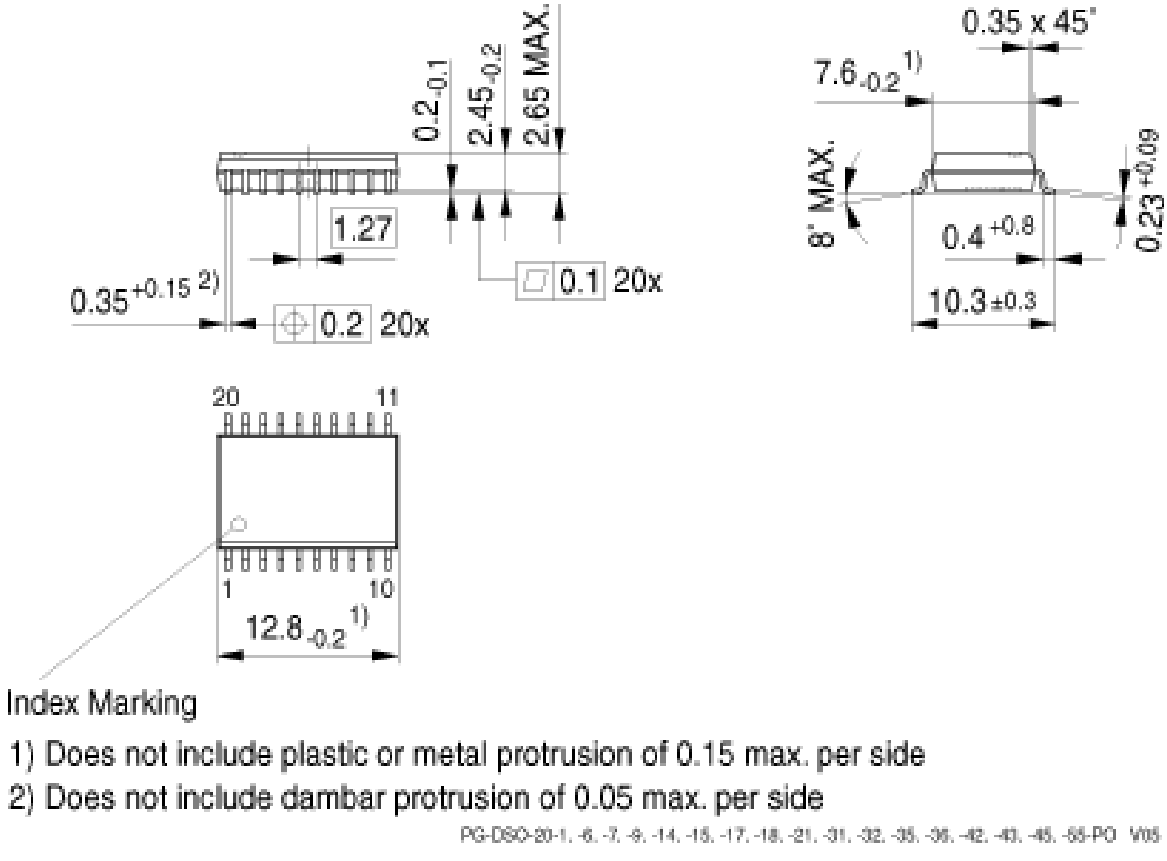


Figure 19 PG-DSO-20-45 Package Outline

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