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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc822mt1fraaakxuma1

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Table of Contents

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC822/824.

2.1 Block Diagram

The block diagram of the XC822/824 is shown in **Figure 2**.

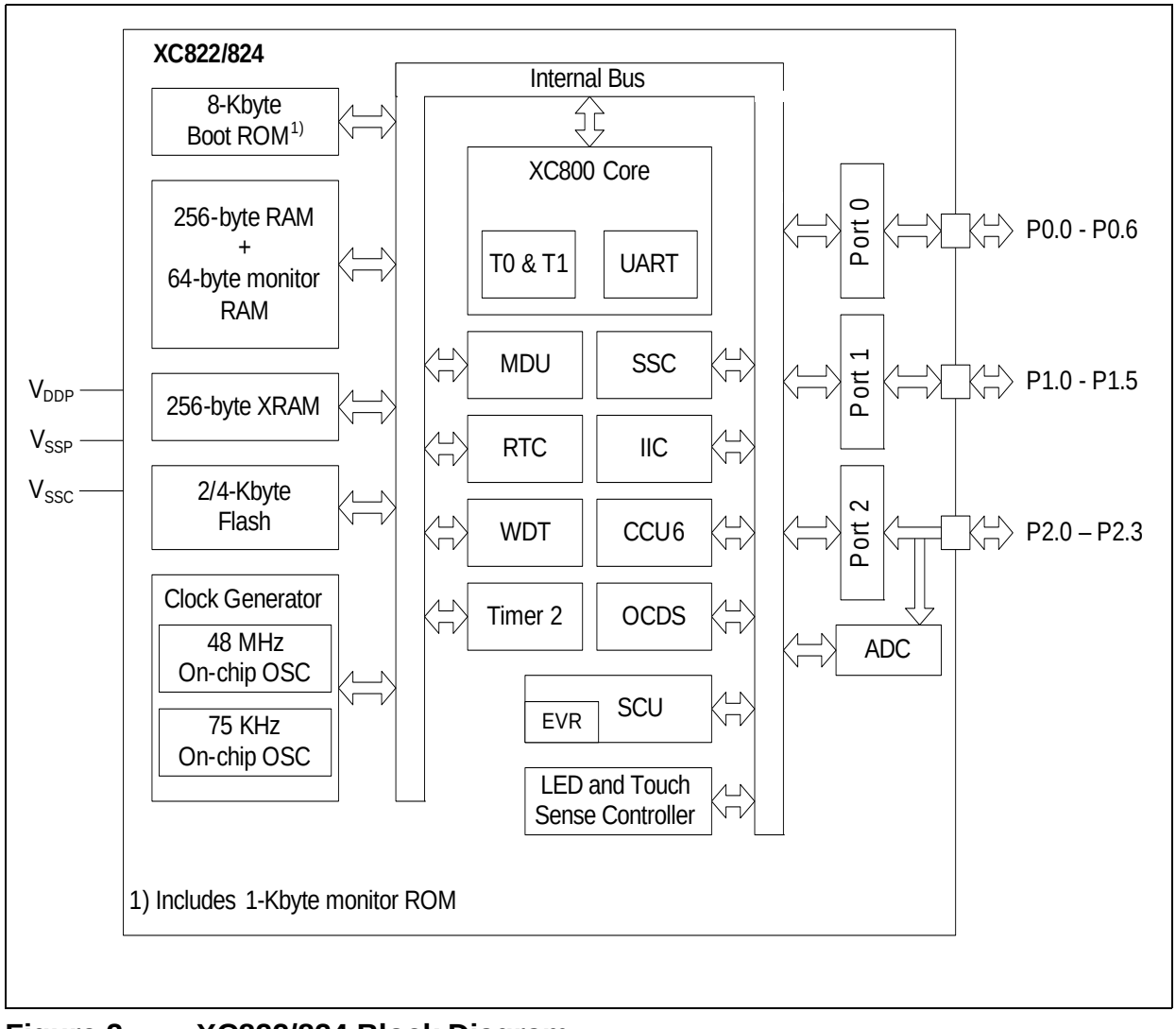


Figure 2 XC822/824 Block Diagram

2.2 Logic Symbol

The logic symbol of the XC822/824 is shown in **Figure 3**.

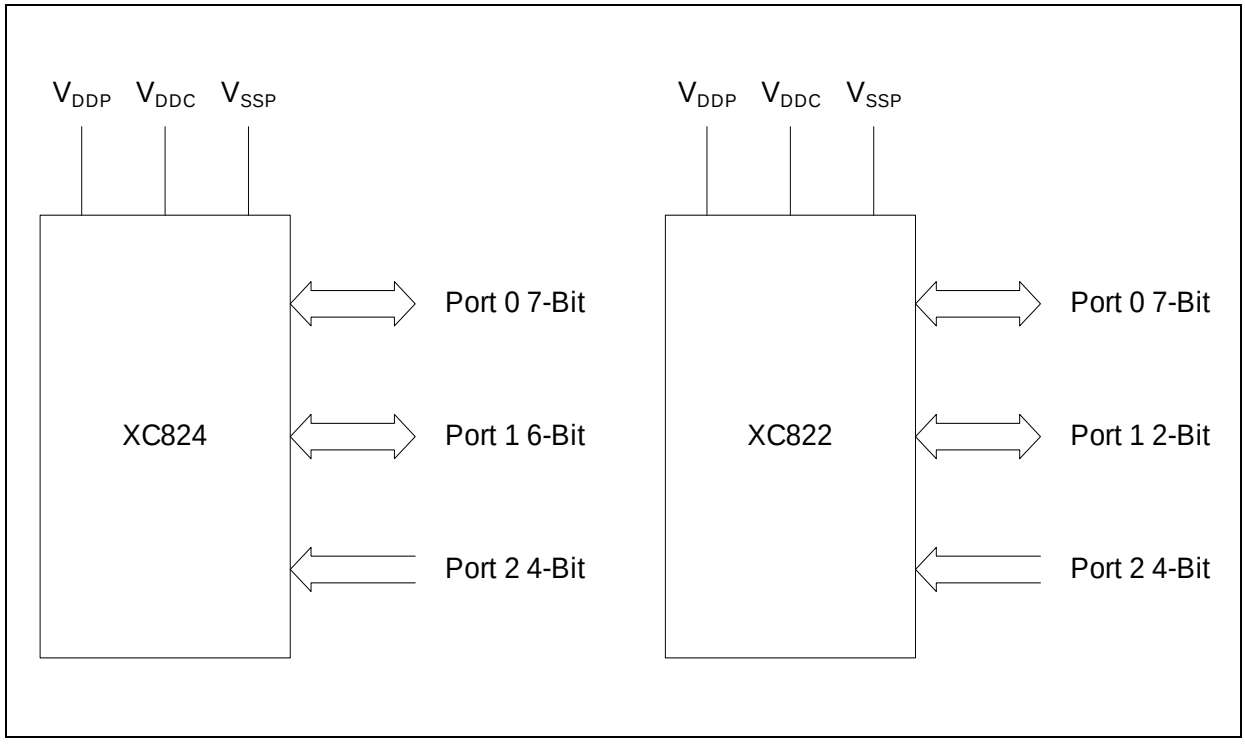


Figure 3 XC822/824 Logic Symbol

The pin configuration of the XC824 in **Figure 5**.

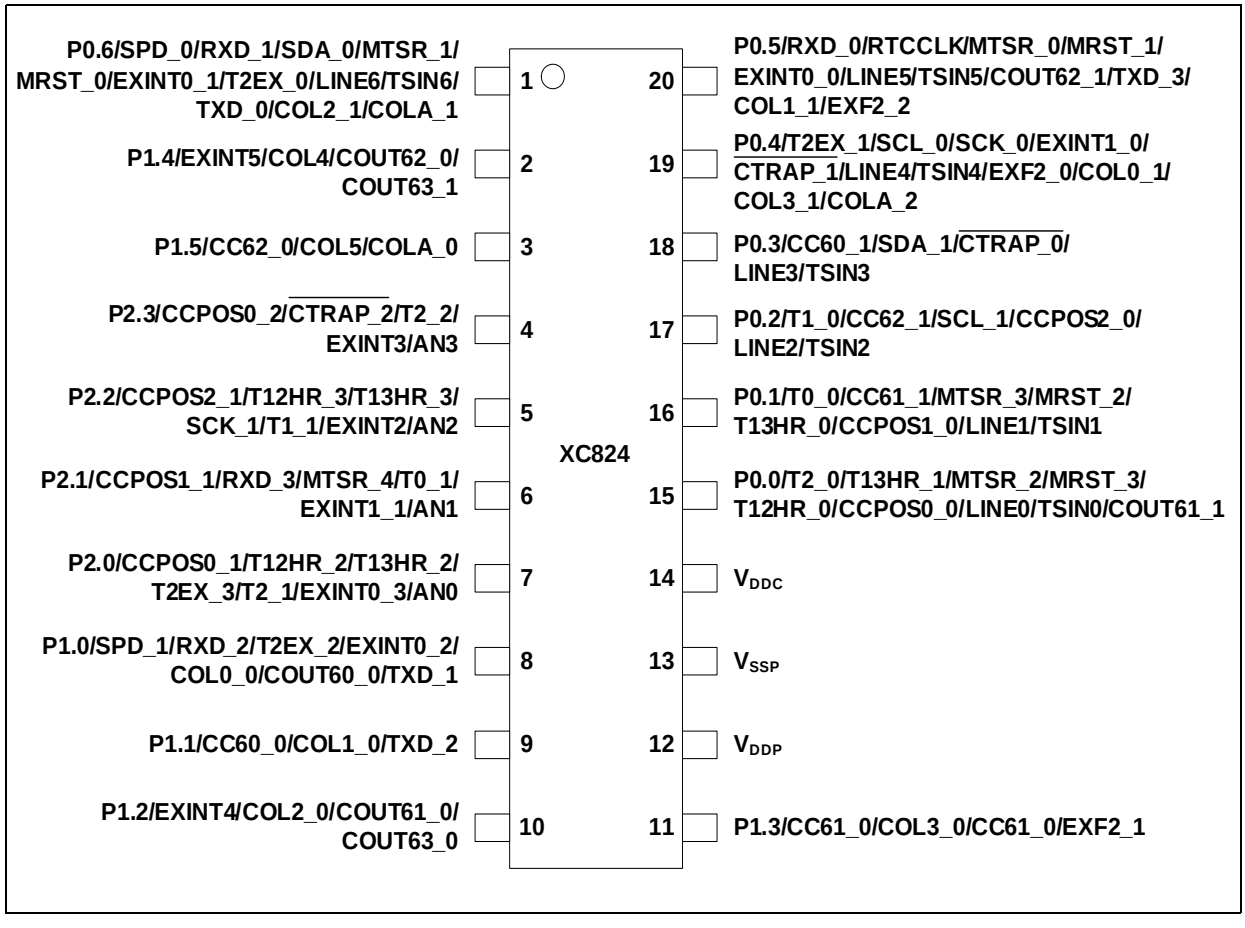


Figure 5 XC824 Pin Configuration, PG-DSO-20 Package (top view)

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.4	19/16		PD	T2EX_1	Timer 2 External Trigger Input
				SCK_0	SSC Clock Input/Output
				SCL_0	IIC Clock Line
				$\overline{\text{CTRAP}}$_1	CCU6 Trap Input
				EXINT1_0	External Interrupt Input 1
				TSIN4	Touch-sense Input 4
				LINE4	LED Line 4
				EXF2_0	Timer 2 Overflow Flag
				COL0_1	LED Column 0
				COL3_1	LED Column 3
				COLA_2	LED Column A
P0.5	20/1		Hi-Z	RXD_0	UART Receive Input
				RTCCLK	RTC External Clock Input
				MTSR_0	SSC Master Transmit Output/ Slave Receive Input
				MRST_1	SSC Master Receive Input
				EXINT0_0	External Interrupt Input 0
				TSIN5	Touch-sense Input 5
				LINE5	LED Line 5
				COUT62_1	Output of Capture/Compare Channel 2
				TXD_3	UART Transmit Output/ 2-wire UART BSL Transmit Output
				COL1_1	LED Column 1
				EXF2_2	Timer 2 Overflow Flag

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P1.1	9/-		Hi-Z	CC60_0	Input/Output of Capture/Compare channel 0
				COL1_0	LED Column 1
				TXD_2	UART Transmit Output
P1.2	10/8		Hi-Z	EXINT4	External Interrupt Input 4
				COL2_0	LED Column 2
				COUT61_0	Output of Capture/Compare channel 1
				COUT63_0	Output of Capture/Compare channel 3
P1.3	11/-		Hi-Z	CC61_0	Input/Output of Capture/Compare channel 1
				COL3_0	LED Column 3
				EXF2_1	Timer 2 Overflow Flag
P1.4	2/-		Hi-Z	EXINT5	External Interrupt Input 5
				COL4	LED Column 4
				COUT62_0	Output of Capture/Compare channel 2
				COUT63_1	Output of Capture/Compare channel 3
P1.5	3/-		Hi-Z	CC62_0	Input/Output of Capture/Compare channel 2
				COL5	LED Column 5
				COLA_0	LED Column A
P2		I		**Port 2** Port 2 is a general purpose input-only port. It can be used as inputs for A/D Converter and out of range comparator, CCU6, Timer 2, SSC and UART.	

3.1.3 Operating Condition

The following operating conditions must not be exceeded in order to ensure correct operation of the XC822/824. All parameters mentioned in the following tables refer to these operating conditions, unless otherwise noted.

Table 7 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		Min.	Max.		
Digital power supply voltage	V_{DDP}	3.0	5.5	V	
		2.5	3.0	V	1)
CPU Clock Frequency	f_{CCLK}	22.5	25.6	MHz	typ. 24 MHz
		7.5	8.5	MHz	typ. 8 MHz
Ambient temperature	T_A	-40	85	°C	SAF-XC822/824...
		-40	105	°C	SAX-XC824...
		-40	125	°C	SAK-XC824...

1) In this voltage range, limited operations are available in active mode. Operations in power save modes are fully supported.

3.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

3.2.1 Input/Output Characteristics

Table 8 provides the characteristics of the input/output pins of the XC822/XC824.

Table 8 Input/Output Characteristics of XC822/XC824 (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins	V_{OLP}	CC	–	1.0	V	I_{OL} = 25 mA (5 V) I_{OL} = 13 mA (3.3 V)
			–	0.4	V	I_{OL} = 10 mA (5 V) I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -15 mA (5 V) I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Input low voltage on port pins	V_{ILP}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input high voltage on port pins	V_{IHP}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input Hysteresis[1)]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V)
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V)
			0.01 × V_{DDP}	–	V	CMOS Mode (2.5 V)
Pull-up current on port pins	I_{PUP}	CC	–	-20	µA	$V_{IH,min}$ (5 V)
			-150	–	µA	$V_{IL,max}$ (5 V)
			–	-5	µA	$V_{IH,min}$ (3.3 V)
			-100	–	µA	$V_{IL,max}$ (3.3 V)

3.2.3 ADC Characteristics

The values in **Table 10** are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performances. In the reduced voltage mode (2.5 V < V_{DDP} < 3 V), the ADC is not recommended to be used.

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog reference voltage	V_{AREF}		–	V_{DDP}	–	V	Connect internally to V_{DDP}
Analog reference ground	V_{AGND}		–	V_{SSP}	–	V	Connect internally to V_{SSP}
Alternate analog reference ground	$V_{AGNDALT}$	SR	V_{SSP} - 0.1	–	2.5[1]	V	Connect to AN0 in differential mode, See **Figure 10**.
Internal voltage reference	V_{INTREF}	SR	1.19	1.23	1.28	V	[3]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	–
ADC clock	f_{ADCI}		8	–	16	MHz	internal analog clock
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	–
Conversion time	t_C	CC	See **Section 3.2.3.1**			µs	–
Total unadjusted error	*TUE*[2]	CC	–	–	±1	LSB8	8-bit conversion with internal reference[3]
			–	–	+4/-1	LSB10	10-bit conversion with internal reference[3][4]
			–	–	+14/-2	LSB12	12-bit conversion using the Low Pass Filter [3]
Differential Nonlinearity	EA_{DNL}	CC	–	–	+1.5/ -1	LSB	10-bit conversion[3]

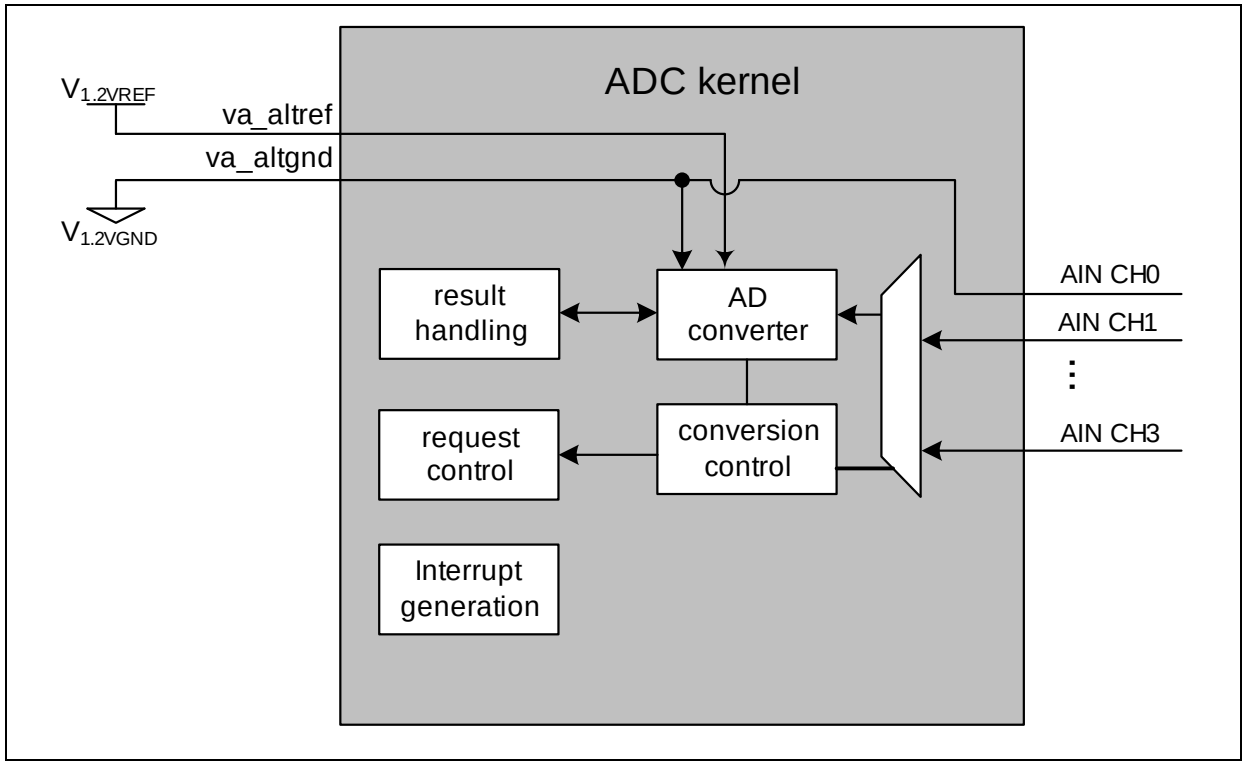


Figure 10 Differential like measurement with internal 1.2V voltage reference, and CH0 gnd.

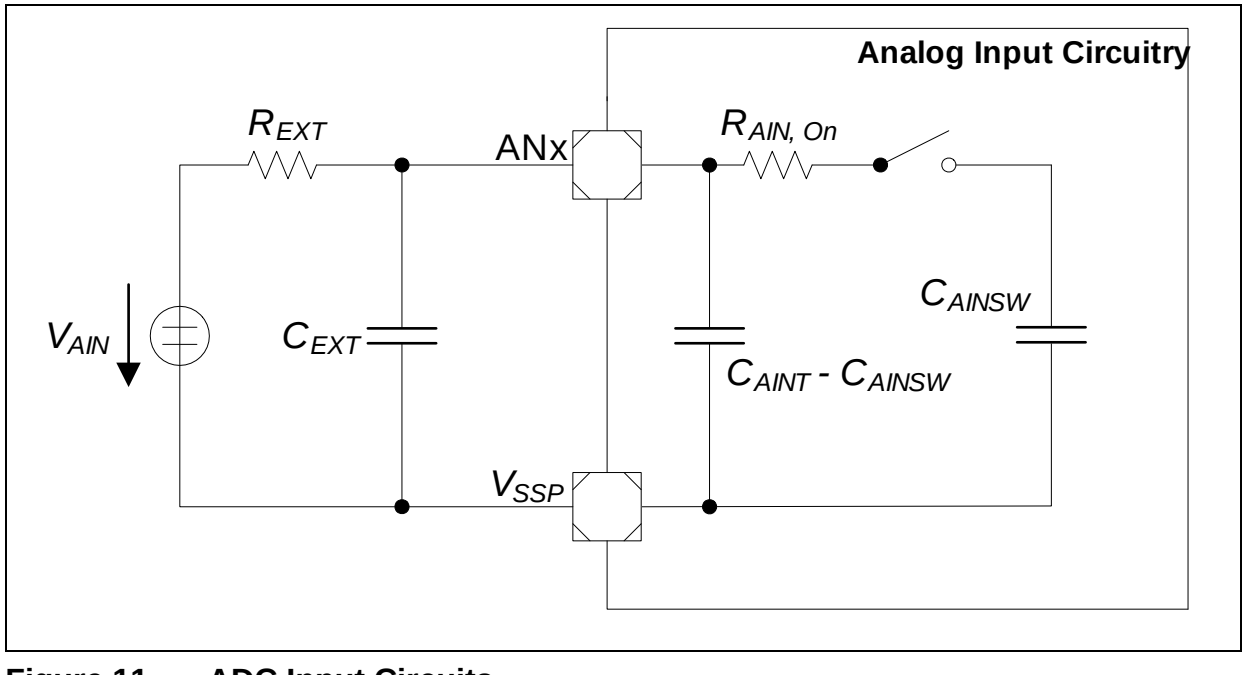


Figure 11 ADC Input Circuits

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)[1)]

Retention	Endurance[2)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) EEPROM Emulation ROM Library can only be used in the 4 Kbyte Flash variant.

2) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

3.2.5 Power Supply Current

Table 15 provides the characteristics of the power supply current in the XC822/824.

Table 15 Power Consumption Parameters[1) 2)](Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Typ.	Max.		
Active Mode	I_{DDPA}	21	25	mA	5 V / 3.3 V [3)]
		14	18	mA	5 V / 3.3 V [4)]
		–	5	mA	2.5 V[5)]
Idle Mode	I_{DDPI}	16	20	mA	5 V / 3.3 V [6)]
		–	5	mA	2.5 V [5)]
Power Down Mode 1	I_{PDP1}	3	5	µA	T_A = 25 °C[7)]
		–	28	µA	T_A = 85 °C[7)8)9)]
Power Down Mode 2	I_{PDP2}	5	7	µA	T_A = 25 °C[7)]
		–	30	µA	T_A = 85 °C[7)8)]

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V and 3.3 V.

2) The maximum values are measured under worst case conditions (T_A = + 125 °C and V_{DDC} = 5 V) unless stated otherwise.

3) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz (CLKMODE=0).

4) I_{DDPA} (active mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz (CLKMODE=1).

5) This value is based on the maximum load capacity of EVR during V_{DDP} = 2.5 V. Not subject to production test, verified by design/characterisation.

6) I_{DDPI} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz (CLKMODE=0).

7) I_{PDP1} and I_{PDP2} is measured at 5 V and 3.3 V with: wake-up port is programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

8) Not subject to production test, verified by design/characterisation.

9) I_{PDP1} and I_{PDP2} has a maximum values of 100 uA at T_A = + 125 °C.

9) LEDTSCU active curent is measured with: module enabled, counter running in 8 MHz.

10) IIC active current is measured with: module enabled, performing a master transmit with the master clock running at 400 KHz.

3.3.3 Oscillator Timing and Wake-up Timing

Table 19 provides the characteristics of the power-on reset, PLL and Wake-up timings in the XC822/824.

Table 19 Power-On Reset Wake-up Timing[1] (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
48 MHz Oscillator start-up time	$t_{48MOSCST}$	CC	–	–	13	µs	
75 KHz Oscillator start-up time	$t_{75KOSCST}$	CC	–	–	800	µs	
Flash initialization time	t_{FINT}	CC	–	160	–	µs	

1) Not subject to production test, verified by design/characterisation.

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 48 MHz oscillator in the XC822/824.

Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-0.5 %	48	+0.5%	MHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-2.0	–	3.0	%	with respect to f_{NOM}, over lifetime and temperature (0 °C to 85 °C)
			-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation (over core supply voltage[2])	Δf_{ST}	CC	-1	–	1	%	with respect to f_{NOM}, within one LIN message (< 10 ms … 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

2) Core voltage supply, V_{DDC} = 2.5 V ± 7.5%.

Table 21 provides the characteristics of the 75 kHz oscillator in the XC822/824.

Table 21 75 kHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-1%	75	+1%	KHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation	Δf_{ST}	CC	-1.5	–	1.5	%	with respect to f_{NOM}, over core supply voltage of 2.5 V ± 7.5%

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

3.3.5.2 SSC Slave Mode Timing

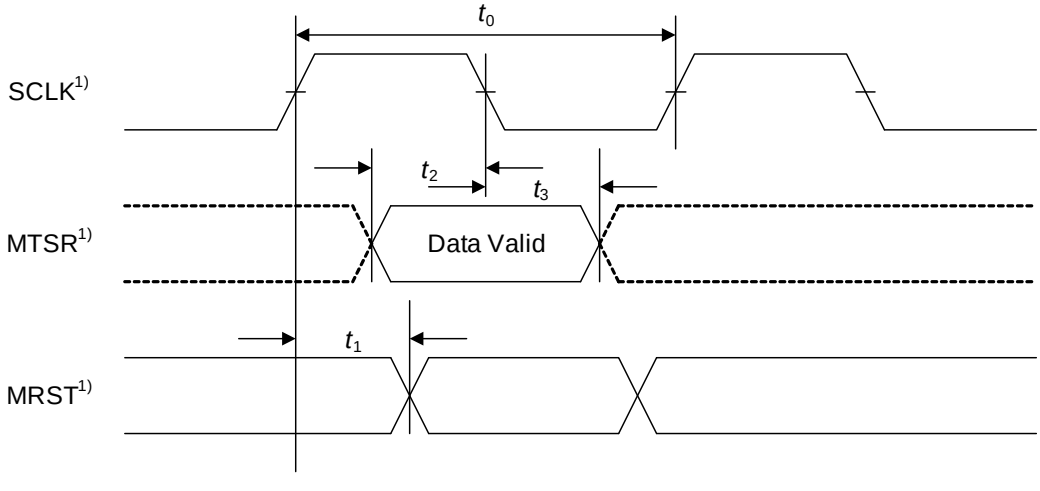
Table 23 provides the SSC slave mode timing in the XC822/824.

Table 23 SSC Slave Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	SR	4 * T_{SSC}[2]	–	ns
MRST delay from SCLK	t_1	CC	0	20	ns
MTSR setup to SCLK	t_2	SR	46	–	ns
MTSR hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 166.7 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup : CON.PH = CON.PO = 0.

Figure 17 SSC Slave Mode Timing

3.3.6 SPD Timing

The SPD interface will work with standard SPD tools having a sample/output clock frequency deviation of +/- 5% or less. For further details please refer to application note AP24004 in section SPD Timing Requirements.

Note: These parameters are no subject to product test but verified by design and/or characterization.

Note: Operating Conditions apply.

4 Package and Quality Declaration

Chapter 4 provides the information of the XC822/824 package and reliability section.

4.1 Package Parameters

Table 24 provides the thermal characteristics of the packages used in XC822 and XC824 respectively.

Table 24 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Package Types
			Min.	Max.		
Thermal resistance junction case[1)]	R_{TJC}	CC	-	36.2	K/W	PG-TSSOP-16-1
			-	34.3	K/W	PG-DSO-20-45
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	356.6	K/W	PG-TSSOP-16-1
			-	36.2	K/W	PG-DSO-20-45

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.

4.2 Package Outline

Figure 18 and **Figure 19** shows the package outlines of the XC822 (TSSOP-16) and XC824 (DSO-20) devices respectively.

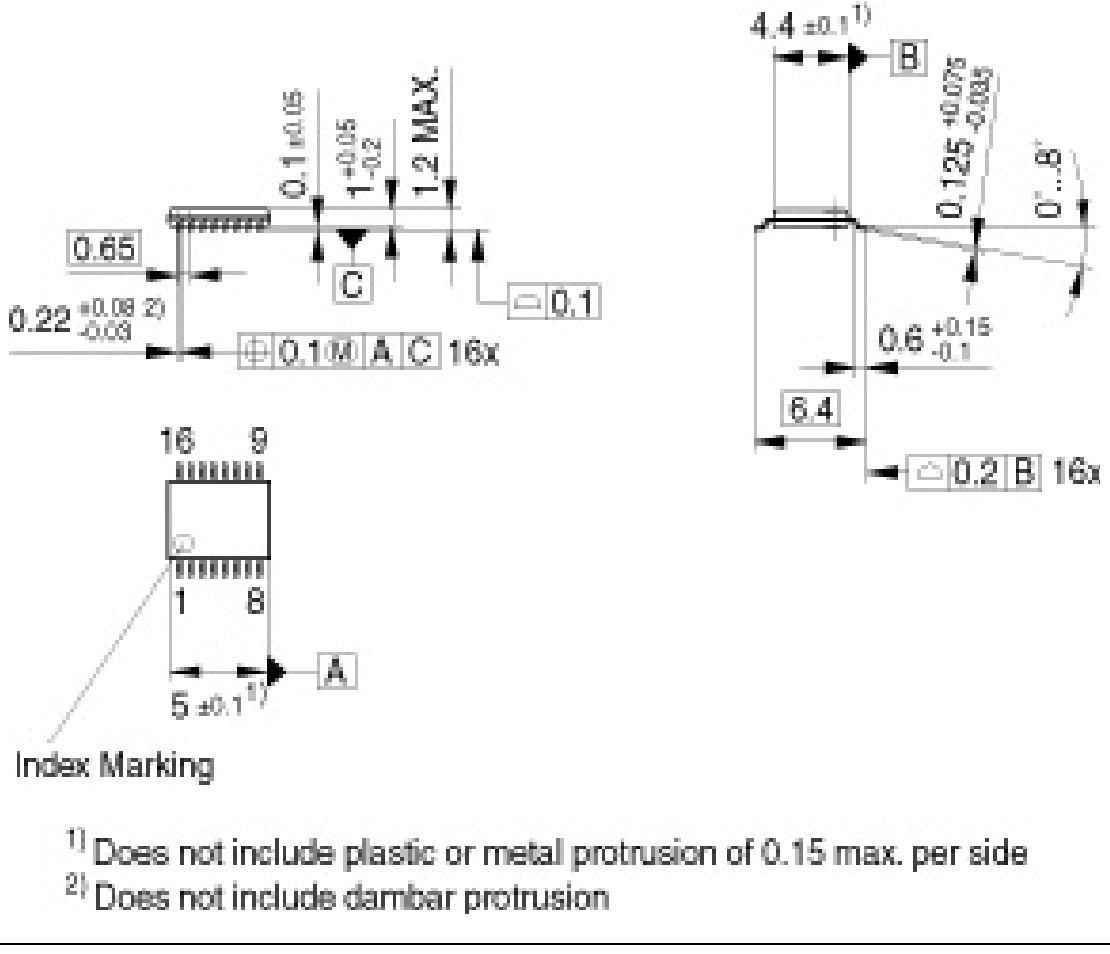


Figure 18 PG-TSSOP-16-1 Package Outline