Infineon Technologies - XC822MT1FRIAAFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc822mt1friaafxuma1

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XC822/824 Variant Devices

The XC822/824 product family features devices with different configurations, program memory sizes, packages options and temperature profiles, to offer cost-effective solutions for different application requirements.

The list of XC822/824 device configurations are summarized in **Table 1**. The type of packages available are TSSOP-16 for XC822 and DSO-20 for XC824.

Table 1 Device Configuration

Device Name	MDU Module	LEDTSCU Module
XC822/824	No	No
XC822/824M	Yes	No
XC822/824T	No	Yes
XC822/824MT	Yes	Yes

Table 2 shows the device sales type available, based on above device.

Table 2 Device Profile

Sales Type	Device Type	Program Memory (Kbytes)	Temp-erature Profile (°C)	Package Type	Quality Profile
SAF-XC822T-0FRI	Flash	2	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822T-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822M-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822MT-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC824M-1FGI	Flash	4	-40 to 85	PG-DSO-20	Industrial
SAF-XC824MT-1FGI	Flash	4	-40 to 85	PG-DSO-20	Industrial
SAX-XC824M-1FGI	Flash	4	-40 to 105	PG-DSO-20	Industrial
SAK-XC824M-1FGI	Flash	4	-40 to 125	PG-DSO-20	Industrial
SAF-XC822-1FRA	Flash	4	-40 to 85	PG-TSSOP-16	Automotive
SAF-XC822MT-1FRA	Flash	4	-40 to 85	PG-TSSOP-16	Automotive
SAK-XC822MT-0FRA	Flash	2	-40 to 125	PG-TSSOP-16	Automotive
SAK-XC822-1FRA	Flash	4	-40 to 125	PG-TSSOP-16	Automotive
SAK-XC822MT-1FRA	Flash	4	-40 to 125	PG-TSSOP-16	Automotive

2.2 Logic Symbol

The logic symbol of the XC822/824 is shown in **Figure 3**.

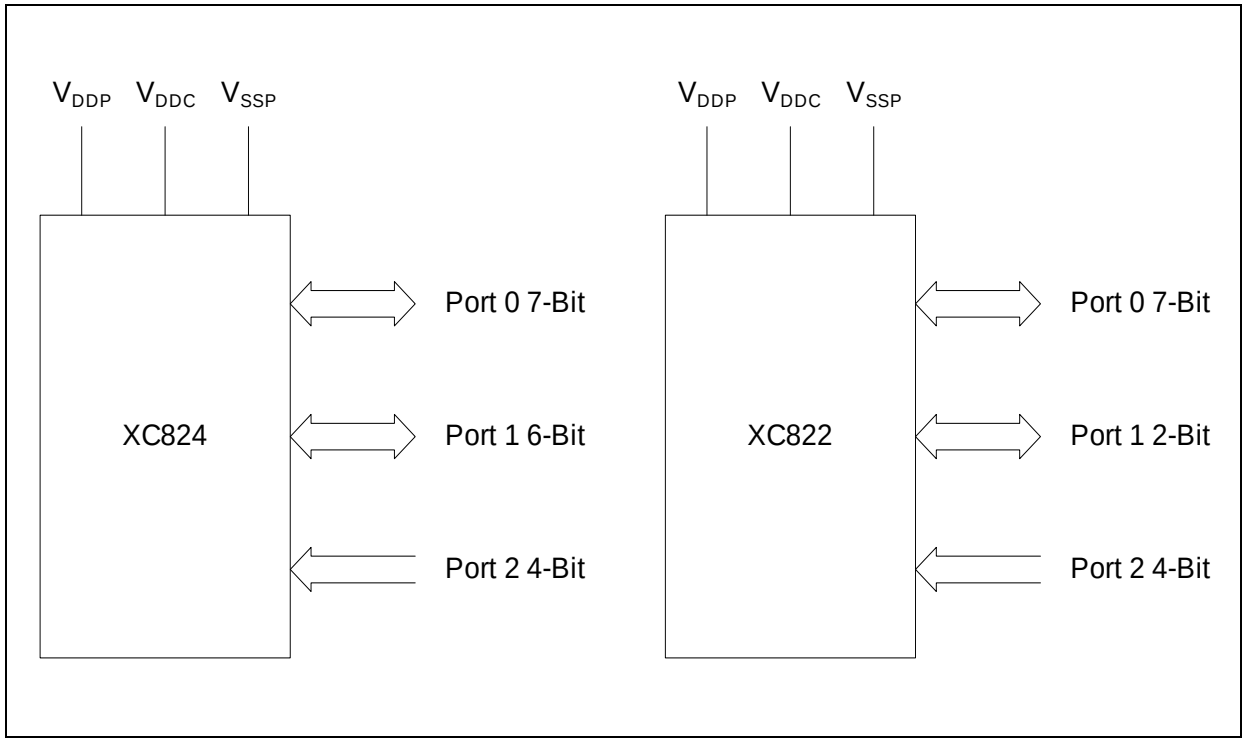


Figure 3 XC822/824 Logic Symbol

2.4 Pin Definitions and Functions

The functions and default states of the XC822/824 external pins are provided in **Table 3**.

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0		I/O		**Port 0** Port 0 is a bidirectional general purpose I/O port. It can be used as alternate functions for LEDTSCU, Timer 0, 1 and 2, SSC, CCU6, IIC, SPD and UART.	
P0.0	15/12		Hi-Z	T2_0	Timer 2 Input
				T13HR_1	CCU6 Timer 13 Hardware Run Input
				MTSR_2	SSC Master Transmit Output/ Slave Receive Input
				MRST_3	SSC Master Receive Input
				T12HR_0	CCU6 Timer 12 Hardware Run Input
				CCPOS0_0	CCU6 Hall Input 0
				TSIN0	Touch-sense Input 0
				LINE0	LED Line 0
				COUT61_1	Output of Capture/Compare Channel 1

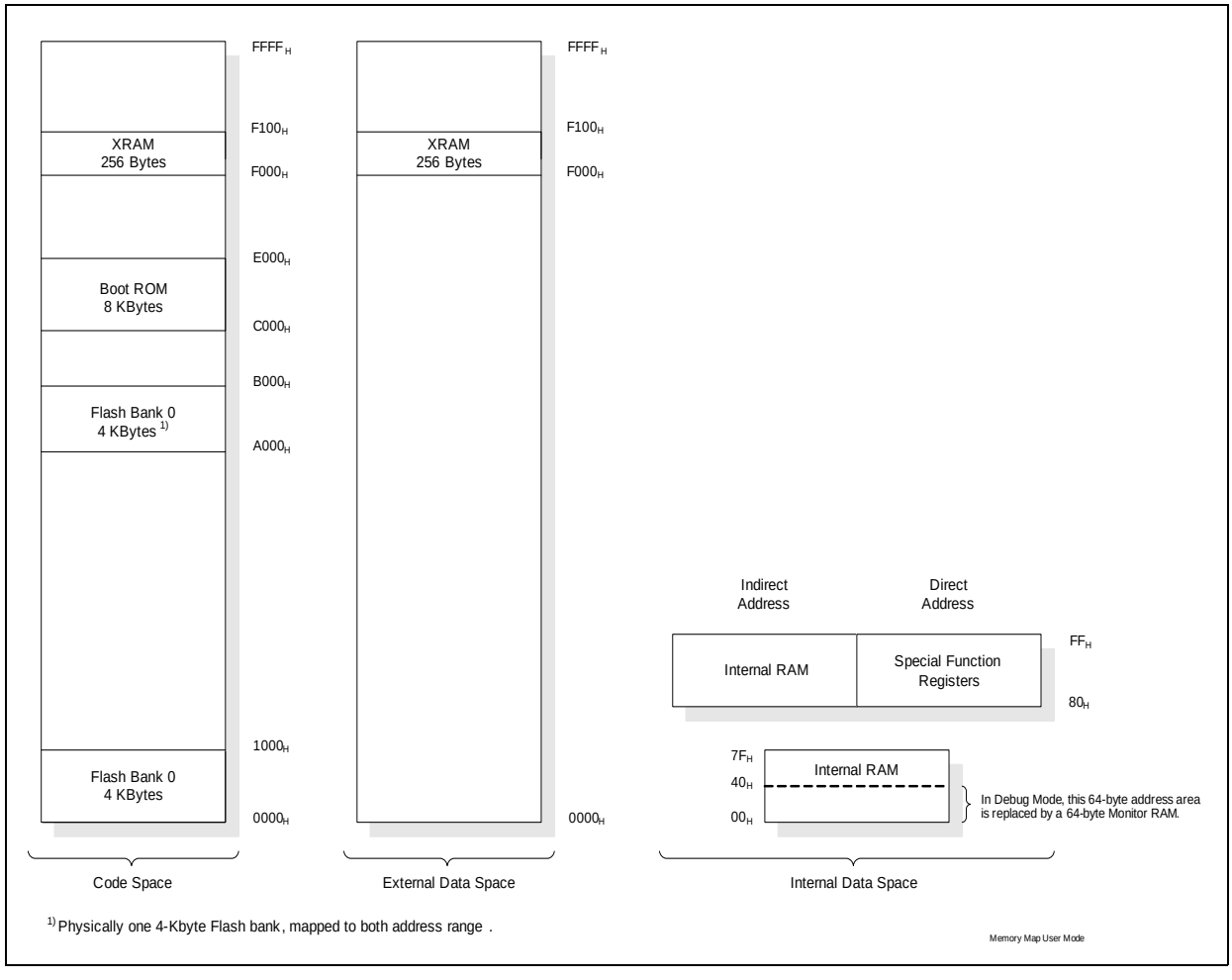
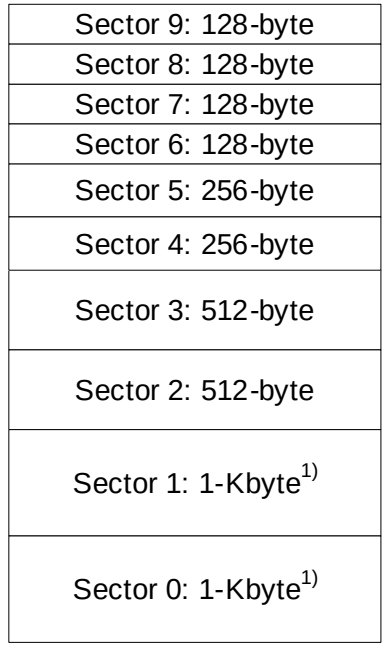


Figure 7 Memory Map of XC822/824 with 4 Kbytes of Flash memory



1) 2 Kbyte Flash devices only has sector 0 and sector 1.

Figure 8 Flash Bank Sectorization

2.6 JTAG ID

JTAG ID register is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC822/824 Flash devices are given in **Table 4**.

Table 4 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC822/824*	101B C083$_H$

Note: The asterisk (*) above denotes all possible device configurations.

2.7 Chip Identification Number

The XC822/824 identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is 51_H. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product and variant type information.

Two methods are provided to read a device's Chip Identification number:

- In-application subroutine, GET_CHIP_INFO
- Boot-loader (BSL) mode A

Table 5 lists the Chip Identification numbers of XC822/824 device variants.

Table 5 Chip Identification Number

Product Variant	Chip Identification Number
XC822T-0FR	51080343_H
XC822MT-0FR	51080303_H
XC822-1FR	51080163_H
XC822T-1FR	51080143_H
XC822M-1FR	51080123_H
XC822MT-1FR	51080103_H
XC824M-1FG	51080122_H
XC824MT-1FG	51080102_H

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC822/824 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

3.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

3.2.1 Input/Output Characteristics

Table 8 provides the characteristics of the input/output pins of the XC822/XC824.

Table 8 Input/Output Characteristics of XC822/XC824 (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins	V_{OLP}	CC	–	1.0	V	I_{OL} = 25 mA (5 V) I_{OL} = 13 mA (3.3 V)
			–	0.4	V	I_{OL} = 10 mA (5 V) I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -15 mA (5 V) I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Input low voltage on port pins	V_{ILP}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input high voltage on port pins	V_{IHP}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input Hysteresis[1)]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V)
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V)
			0.01 × V_{DDP}	–	V	CMOS Mode (2.5 V)
Pull-up current on port pins	I_{PUP}	CC	–	-20	µA	$V_{IH,min}$ (5 V)
			-150	–	µA	$V_{IL,max}$ (5 V)
			–	-5	µA	$V_{IH,min}$ (3.3 V)
			-100	–	µA	$V_{IL,max}$ (3.3 V)

Table 8 Input/Output Characteristics of XC822/XC824 (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Pull-down current on port pins	I_{PDP}	CC	–	20	µA	$V_{IL,max}$ (5 V)
			150	–	µA	$V_{IH,min}$ (5 V)
			–	5	µA	$V_{IL,max}$ (3.3 V)
			100	–	µA	$V_{IH,min}$ (3.3 V)
Input leakage current on port pins[2)]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125$ °C
Overload current on any pin	I_{OVP}	SR	-5	5	mA	3)
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$	SR	–	25	mA	3)
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	4)
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M	SR	-15	25	mA	–
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	80	mA	3)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	80	mA	3)

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Supply Threshold Characteristics

Table 9 provides the characteristics of the supply threshold in the XC822/824.

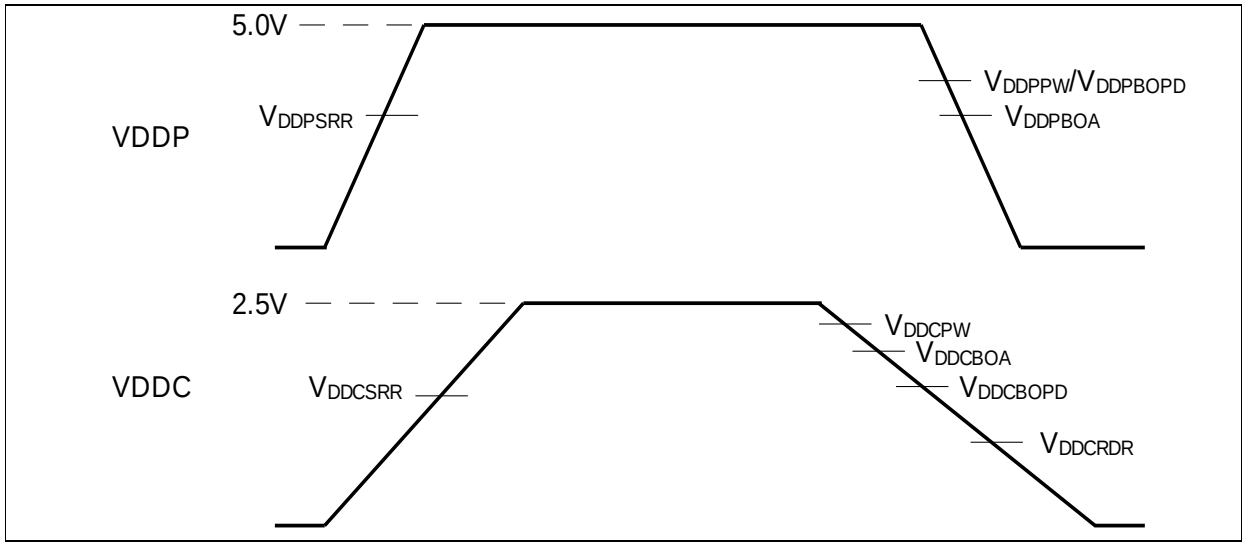


Figure 9 Supply Threshold Parameters

Table 9 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
V_{DDP} prewarning voltage[1)2)]	V_{DDPPW}	CC	3.0	3.6	4.5	V
V_{DDP} brownout voltage in active mode[3)2)]	V_{DDPBOA}	CC	2.65	2.75	2.87	V
V_{DDP} brownout voltage in power down mode[2)3)]	$V_{DDPBOPD}$	CC	3.0	3.6	4.5	V
V_{DDP} system reset release voltage[2)4)]	V_{DDPSRR}	CC	2.7	2.8	2.92	V
V_{DDC} prewarning voltage[2)5)]	V_{DDCPW}	CC	2.3	2.4	2.48	V
V_{DDC} brownout voltage in active mode[2)]	V_{DDCBOA}	CC	2.25	2.3	2.42	V
V_{DDC} brownout voltage in power down mode[2)]	$V_{DDCBOPD}$	CC	1.35	1.5	1.95	V
V_{DDC} system reset release voltage[2)4)]	V_{DDCSRR}	CC	2.28	2.3	2.47	V
RAM data retention voltage	V_{DDCRDR}	CC	1.1	–	–	V

1) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode. Detection should be disabled for V_{DDP} less than maximum of V_{DDPPW}.

2) This parameter has a hysteresis of 50 mV.

3) Detection is enabled via SDCON register. Detection must be disabled for application with V_{DDP} less than the specified values.

4) V_{DDPSRR} and V_{DDCSRR} must be met before the system reset is released.

5) Detection is enabled via SDCON register in active mode. It is automatically disabled in power down mode.

3.2.4 Flash Memory Parameters

The XC822/824 is delivered with all Flash sectors erased (read all zeros).

The data retention time of the XC822/824's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: Flash memory parameters are not subject to production test but verified by design and/or characterization.

Table 12 Flash Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Read access time (per byte)	t_{ACC}	CC	–	125	–	ns	
Programming time (per wordline)	t_{PR}	CC	–	2.2	–	ms	
Erase time (one or more sectors)	t_{ER}	CC	–	120	–	ms	
Flash wait states	$N_{WSFLASH}$	CC	0				CPU clock = 8 MHz
			1				CPU clock = 24 MHz

Table 13 Flash Data Retention and Endurance (Operating Conditions apply)

Retention	Endurance[1)]	Size	Remarks
20 years	1,000 cycles	up to 8 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in **Table 13** is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

3.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

3.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 12**, **Figure 13** and **Figure 14**.

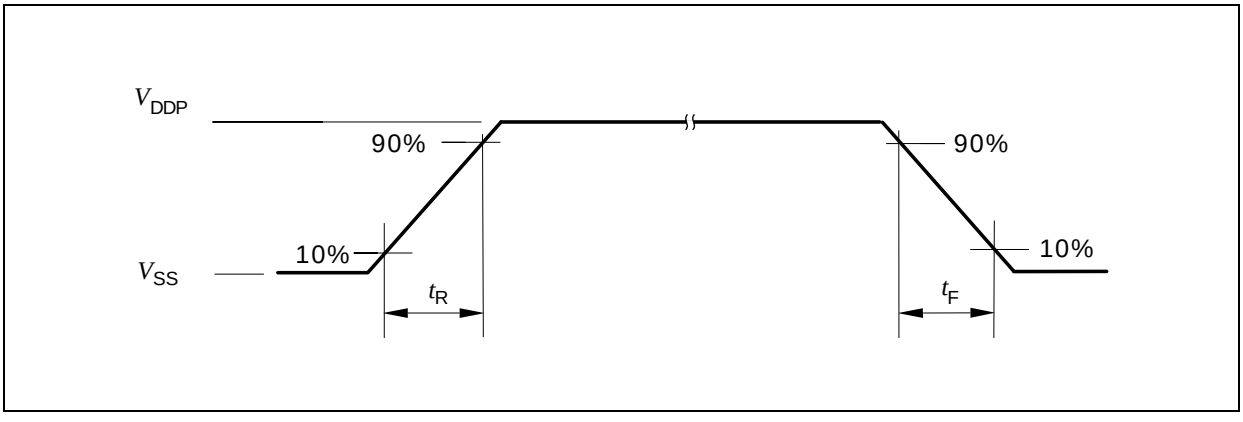


Figure 12 Rise/Fall Time Parameters

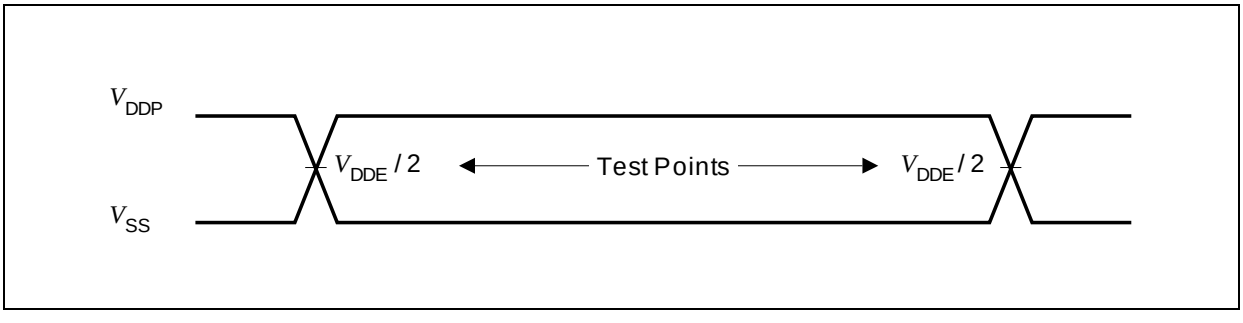


Figure 13 Testing Waveform, Output Delay

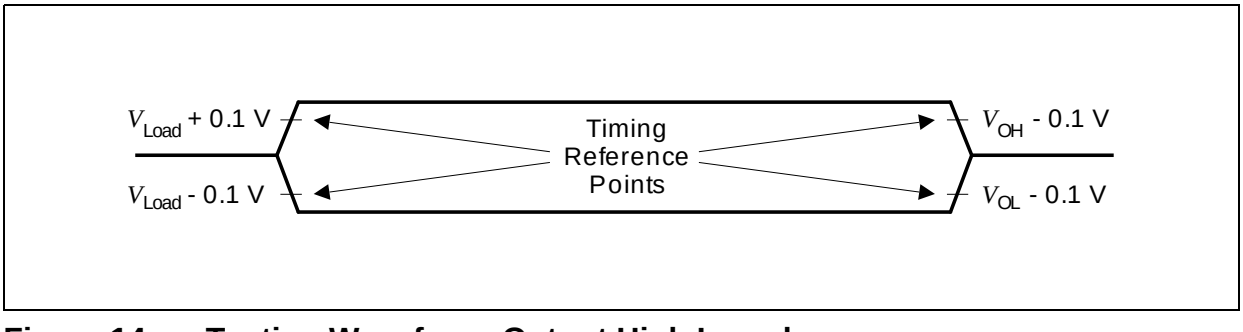


Figure 14 Testing Waveform, Output High Impedance

3.3.3 Oscillator Timing and Wake-up Timing

Table 19 provides the characteristics of the power-on reset, PLL and Wake-up timings in the XC822/824.

Table 19 Power-On Reset Wake-up Timing[1] (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
48 MHz Oscillator start-up time	$t_{48MOSCST}$	CC	–	–	13	µs	
75 KHz Oscillator start-up time	$t_{75KOSCST}$	CC	–	–	800	µs	
Flash initialization time	t_{FINT}	CC	–	160	–	µs	

1) Not subject to production test, verified by design/characterisation.

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 48 MHz oscillator in the XC822/824.

Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-0.5 %	48	+0.5%	MHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-2.0	–	3.0	%	with respect to f_{NOM}, over lifetime and temperature (0 °C to 85 °C)
			-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation (over core supply voltage[2])	Δf_{ST}	CC	-1	–	1	%	with respect to f_{NOM}, within one LIN message (< 10 ms … 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

2) Core voltage supply, V_{DDC} = 2.5 V ± 7.5%.

Table 21 provides the characteristics of the 75 kHz oscillator in the XC822/824.

Table 21 75 kHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-1%	75	+1%	KHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation	Δf_{ST}	CC	-1.5	–	1.5	%	with respect to f_{NOM}, over core supply voltage of 2.5 V ± 7.5%

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

3.3.5 SSC Timing

3.3.5.1 SSC Master Mode Timing

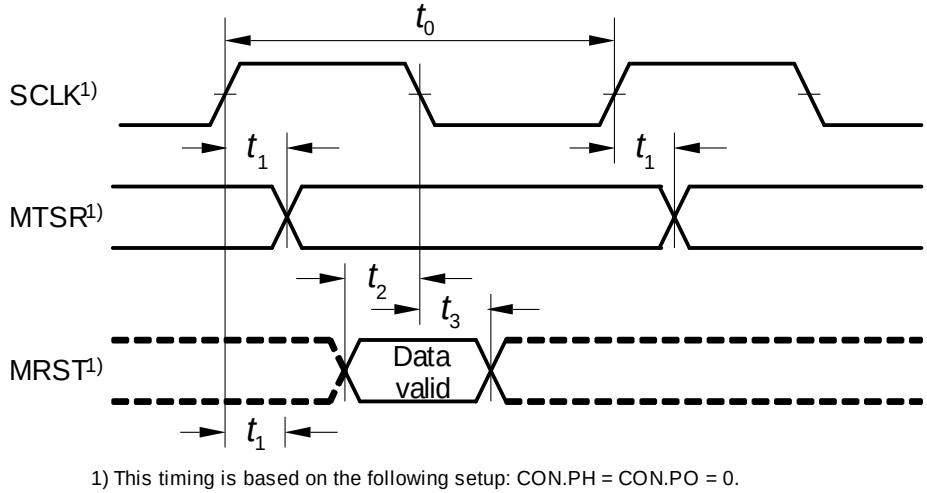
Table 22 provides the SSC master mode timing in the XC822/824.

Table 22 SSC Master Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	CC	2 * T_{SSC}[2]	–	ns
MTSR delay from SCLK	t_1	CC	0	6	ns
MRST setup to SCLK	t_2	SR	20	–	ns
MRST hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 83.3 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_Tmg1

Figure 16 SSC Master Mode Timing

4 Package and Quality Declaration

Chapter 4 provides the information of the XC822/824 package and reliability section.

4.1 Package Parameters

Table 24 provides the thermal characteristics of the packages used in XC822 and XC824 respectively.

Table 24 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Package Types
			Min.	Max.		
Thermal resistance junction case[1)]	R_{TJC}	CC	-	36.2	K/W	PG-TSSOP-16-1
			-	34.3	K/W	PG-DSO-20-45
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	356.6	K/W	PG-TSSOP-16-1
			-	36.2	K/W	PG-DSO-20-45

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.

4.2 Package Outline

Figure 18 and **Figure 19** shows the package outlines of the XC822 (TSSOP-16) and XC824 (DSO-20) devices respectively.

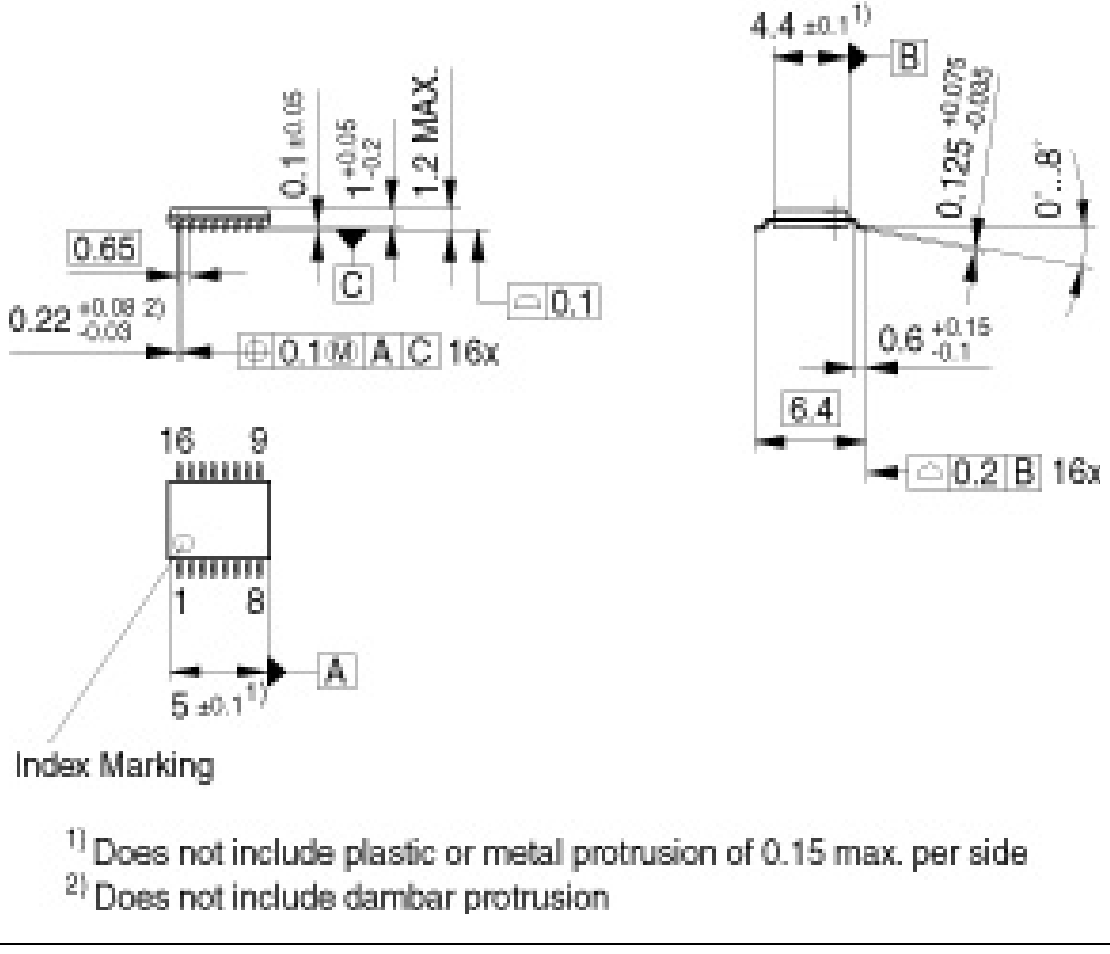


Figure 18 PG-TSSOP-16-1 Package Outline

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