Infineon Technologies - XC822T0FRIAAFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	13
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc822t0friaafxuma1

XC822/824

8-Bit Single-Chip Microcontroller

Data Sheet

V1.2 2011-10

Microcontrollers

Table of Contents

1 Summary of Features

The XC822/824 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM, Library ROM and User routines
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 2/4 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 2.5 V - 5.5 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

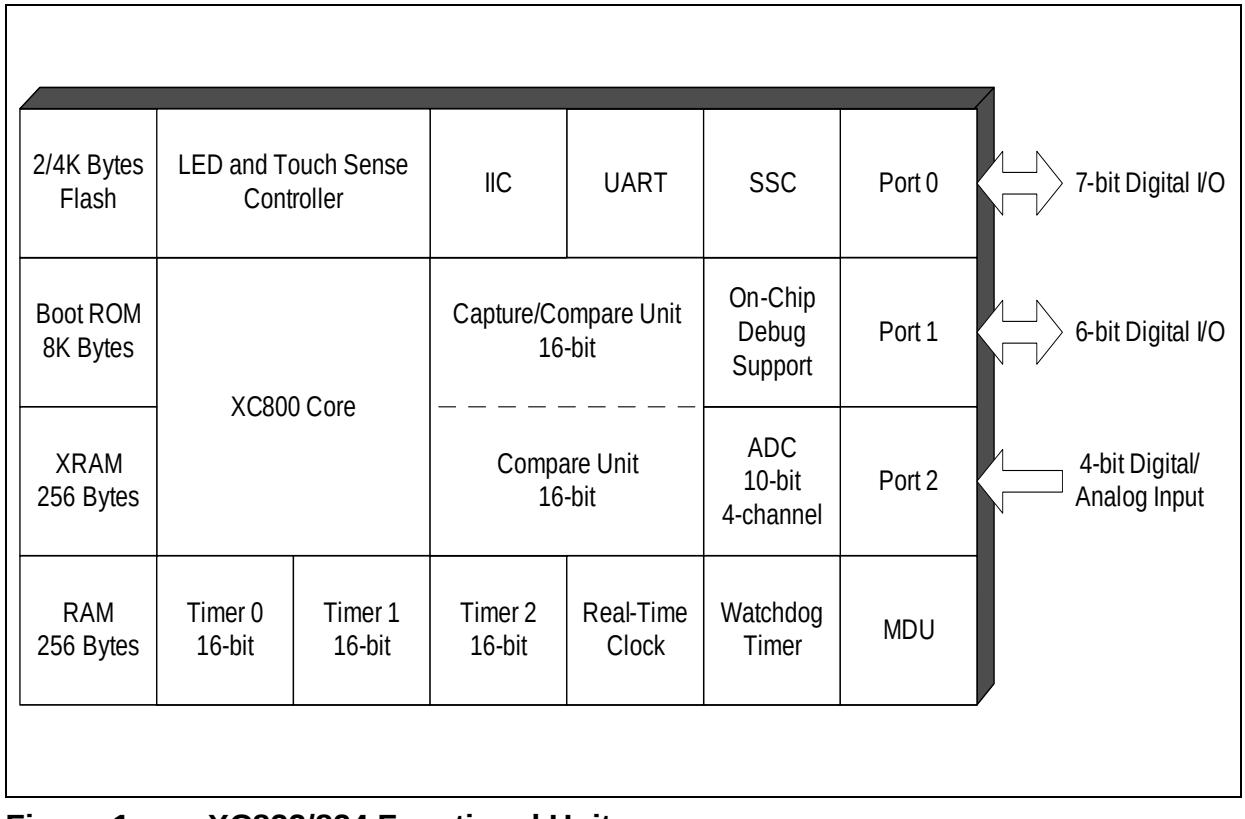


Figure 1 XC822/824 Functional Units

- Power-on reset generation
- Brownout detection for IO supply and core logic supply
- 48 MHz on-chip OSC for clock generation
  - Loss-of-Clock detection

(more features on next page)

XC822/824 Variant Devices

The XC822/824 product family features devices with different configurations, program memory sizes, packages options and temperature profiles, to offer cost-effective solutions for different application requirements.

The list of XC822/824 device configurations are summarized in **Table 1**. The type of packages available are TSSOP-16 for XC822 and DSO-20 for XC824.

Table 1 Device Configuration

Device Name	MDU Module	LEDTSCU Module
XC822/824	No	No
XC822/824M	Yes	No
XC822/824T	No	Yes
XC822/824MT	Yes	Yes

Table 2 shows the device sales type available, based on above device.

Table 2 Device Profile

Sales Type	Device Type	Program Memory (Kbytes)	Temp-erature Profile (°C)	Package Type	Quality Profile
SAF-XC822T-0FRI	Flash	2	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822T-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822M-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC822MT-1FRI	Flash	4	-40 to 85	PG-TSSOP-16	Industrial
SAF-XC824M-1FGI	Flash	4	-40 to 85	PG-DSO-20	Industrial
SAF-XC824MT-1FGI	Flash	4	-40 to 85	PG-DSO-20	Industrial
SAX-XC824M-1FGI	Flash	4	-40 to 105	PG-DSO-20	Industrial
SAK-XC824M-1FGI	Flash	4	-40 to 125	PG-DSO-20	Industrial
SAF-XC822-1FRA	Flash	4	-40 to 85	PG-TSSOP-16	Automotive
SAF-XC822MT-1FRA	Flash	4	-40 to 85	PG-TSSOP-16	Automotive
SAK-XC822MT-0FRA	Flash	2	-40 to 125	PG-TSSOP-16	Automotive
SAK-XC822-1FRA	Flash	4	-40 to 125	PG-TSSOP-16	Automotive
SAK-XC822MT-1FRA	Flash	4	-40 to 125	PG-TSSOP-16	Automotive

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC822/824.

2.1 Block Diagram

The block diagram of the XC822/824 is shown in **Figure 2**.

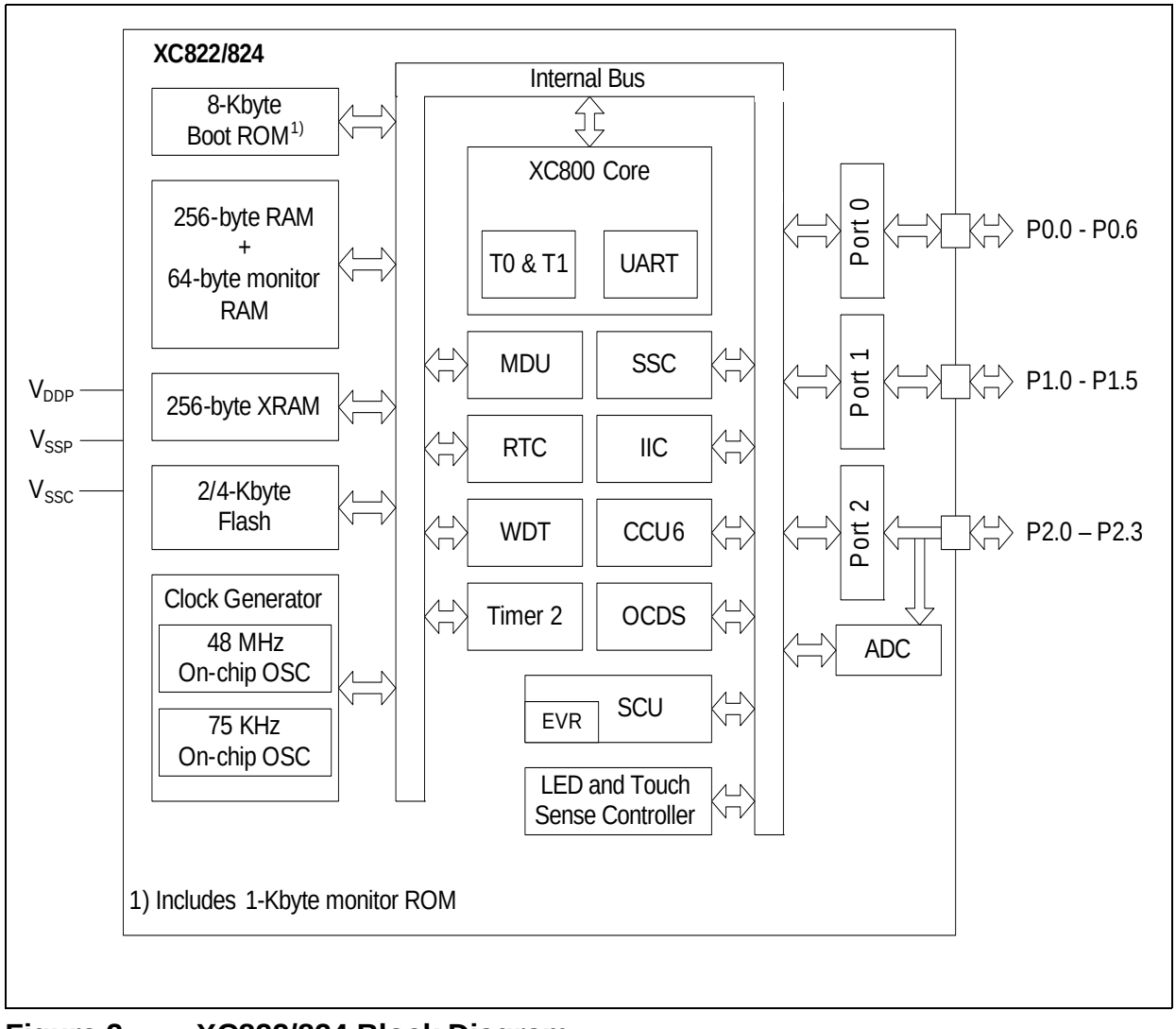


Figure 2 XC822/824 Block Diagram

2.2 Logic Symbol

The logic symbol of the XC822/824 is shown in **Figure 3**.

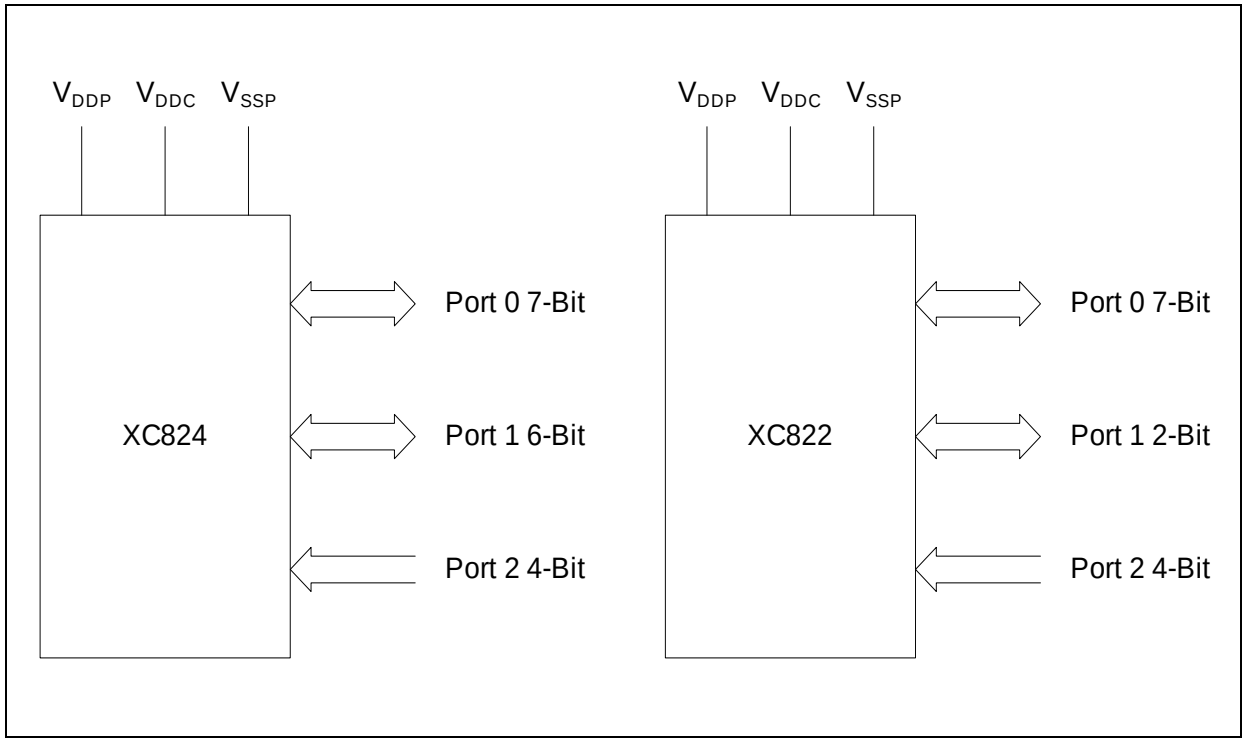


Figure 3 XC822/824 Logic Symbol

The pin configuration of the XC824 in **Figure 5**.

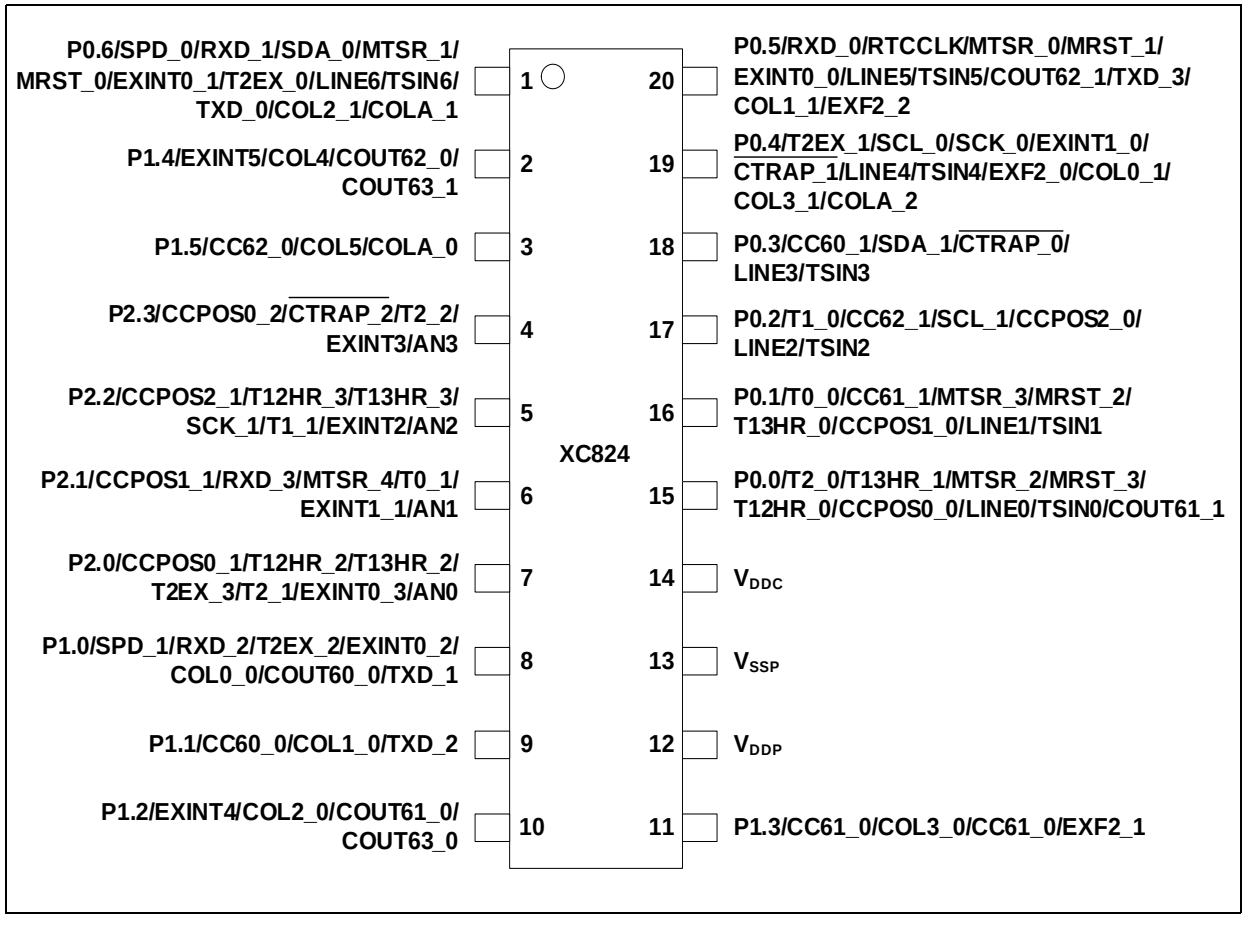


Figure 5 XC824 Pin Configuration, PG-DSO-20 Package (top view)

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.1	16/13		Hi-Z	T0_0	Timer 0 Input
				CC61_1	Input/Output of Capture/Compare channel 1
				MTSR_3	SSC Slave Receive Input
				MRST_2	SSC Master Receive Input/ Slave Transmit Output
				T13HR_0	CCU6 Timer 13 Hardware Run Input
				CCPOS1_0	CCU6 Hall Input 1
				TSIN1	Touch-sense Input 1
				LINE1	LED Line 1
P0.2	17/14		Hi-Z	T1_0	Timer 1 Input
				CC62_1	Input/Output of Capture/Compare channel 2
				SCL_1	IIC Clock Line
				CCPOS2_0	CCU6 Hall Input 2
				TSIN2	Touch-sense Input 2
				LINE2	LED Line 2
P0.3	18/15		Hi-Z	CC60_1	Input/Output of Capture/Compare channel 0
				SDA_1	IIC Data Line
				$\overline{\text{CTRAP\_0}}$	CCU6 Trap Input
				TSIN3	Touch-sense Input 3
				LINE3	LED Line 3

2.7 Chip Identification Number

The XC822/824 identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is 51_H. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product and variant type information.

Two methods are provided to read a device's Chip Identification number:

- In-application subroutine, GET_CHIP_INFO
- Boot-loader (BSL) mode A

Table 5 lists the Chip Identification numbers of XC822/824 device variants.

Table 5 Chip Identification Number

Product Variant	Chip Identification Number
XC822T-0FR	51080343_H
XC822MT-0FR	51080303_H
XC822-1FR	51080163_H
XC822T-1FR	51080143_H
XC822M-1FR	51080123_H
XC822MT-1FR	51080103_H
XC824M-1FG	51080122_H
XC824MT-1FG	51080102_H

3 Electrical Parameters

Chapter 3 provides the characteristics of the electrical parameters which are implementation-specific for the XC822/824.

3.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 3.2** and **Section 3.3**.

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC822/824 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  - These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC822/824 and must be regarded for a system design.
- **SR**
  - These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC822/824 is designed in.

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC822/824 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

3.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

3.2.1 Input/Output Characteristics

Table 8 provides the characteristics of the input/output pins of the XC822/XC824.

Table 8 Input/Output Characteristics of XC822/XC824 (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins	V_{OLP}	CC	–	1.0	V	I_{OL} = 25 mA (5 V) I_{OL} = 13 mA (3.3 V)
			–	0.4	V	I_{OL} = 10 mA (5 V) I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -15 mA (5 V) I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Input low voltage on port pins	V_{ILP}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input high voltage on port pins	V_{IHP}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input Hysteresis[1)]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V)
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V)
			0.01 × V_{DDP}	–	V	CMOS Mode (2.5 V)
Pull-up current on port pins	I_{PUP}	CC	–	-20	µA	$V_{IH,min}$ (5 V)
			-150	–	µA	$V_{IL,max}$ (5 V)
			–	-5	µA	$V_{IH,min}$ (3.3 V)
			-100	–	µA	$V_{IL,max}$ (3.3 V)

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Integral Nonlinearity	EA_{INL}	CC	–	–	±1.5	LSB	10-bit conversion[3]
Offset	EA_{OFF}	CC	–	+4	–	LSB	10-bit conversion[3]
Gain	EA_{GAIN}	CC	–	-4	–	LSB	10-bit conversion[3]
Switched capacitance at an analog input	C_{AINSW}	CC	–	2	3	pF	3)5)
Total capacitance at an analog input	C_{AINT}	CC	–	–	12	pF	3)5)
Input resistance of an analog input	R_{AIN}	CC	–	1.5	2	kΩ	3)

1) 1.2 V at V_{DDP} = 3.0 V.

2) TUE is tested at V_{AREF} = V_{DDP} = 5.0 V and CPU clock ($f_{SCLK, CCLK}$) = 8 MHz.

3) Not subject to production test, verified by design/characterization.

4) If a reduced positive reference voltage is used, TUE will increase. If the positive reference is reduced by a factor of K, the TUE will increased by 1/K. Example:K = 0.8, 1/K = 1.25; 1.25 X TUE = 2.5 LSB10.

5) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.

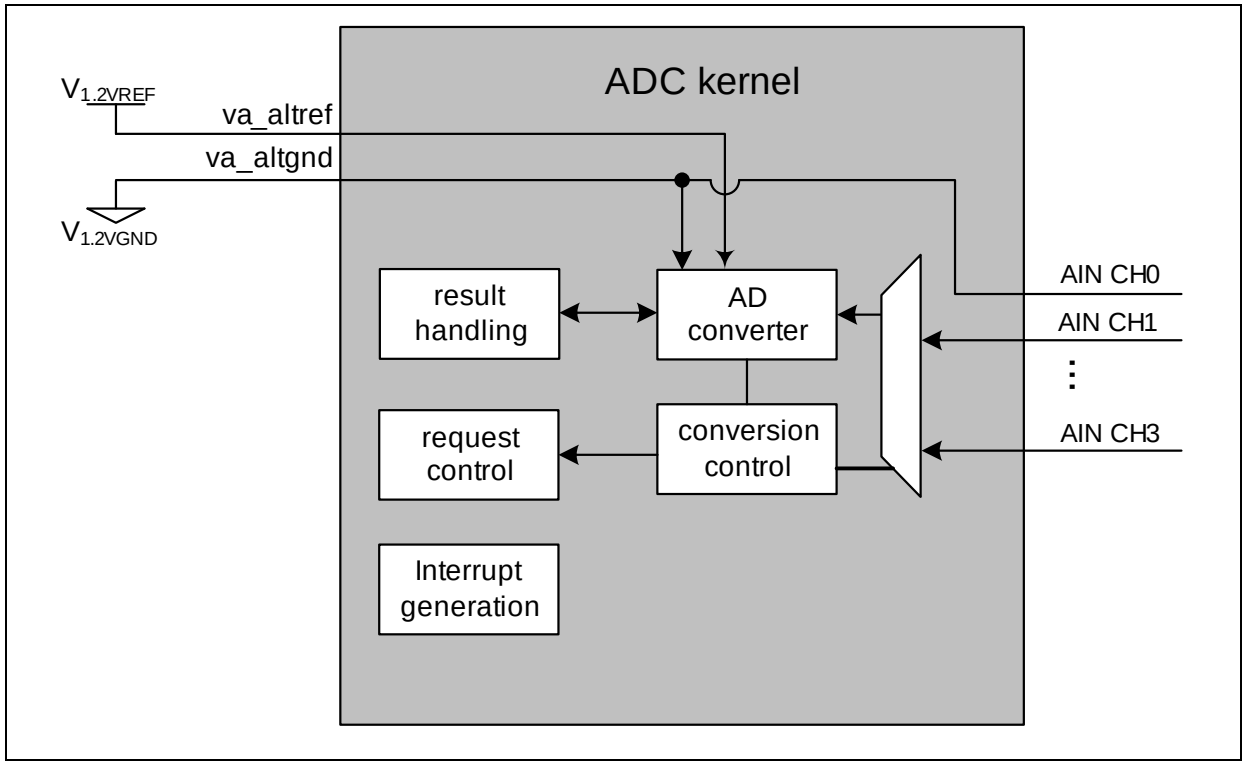


Figure 10 Differential like measurement with internal 1.2V voltage reference, and CH0 gnd.

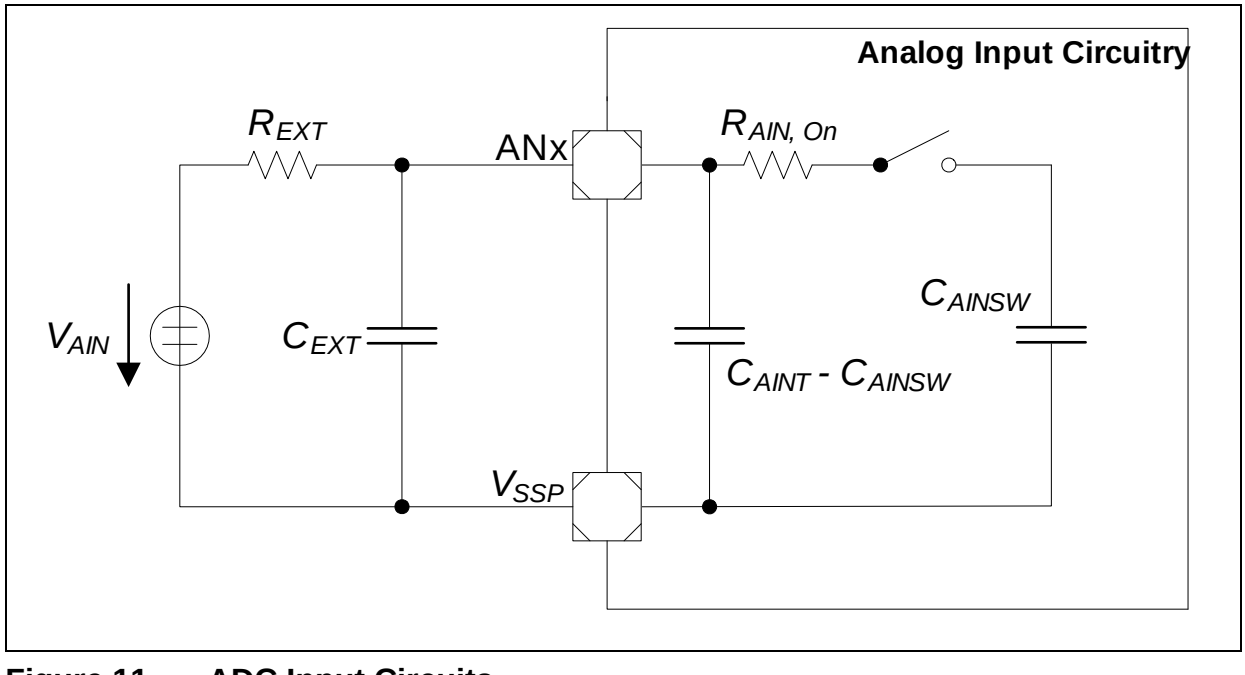


Figure 11 ADC Input Circuits

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)[1)]

Retention	Endurance[2)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) EEPROM Emulation ROM Library can only be used in the 4 Kbyte Flash variant.

2) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

9) LEDTSCU active curent is measured with: module enabled, counter running in 8 MHz.

10) IIC active current is measured with: module enabled, performing a master transmit with the master clock running at 400 KHz.

3.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

3.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 12**, **Figure 13** and **Figure 14**.

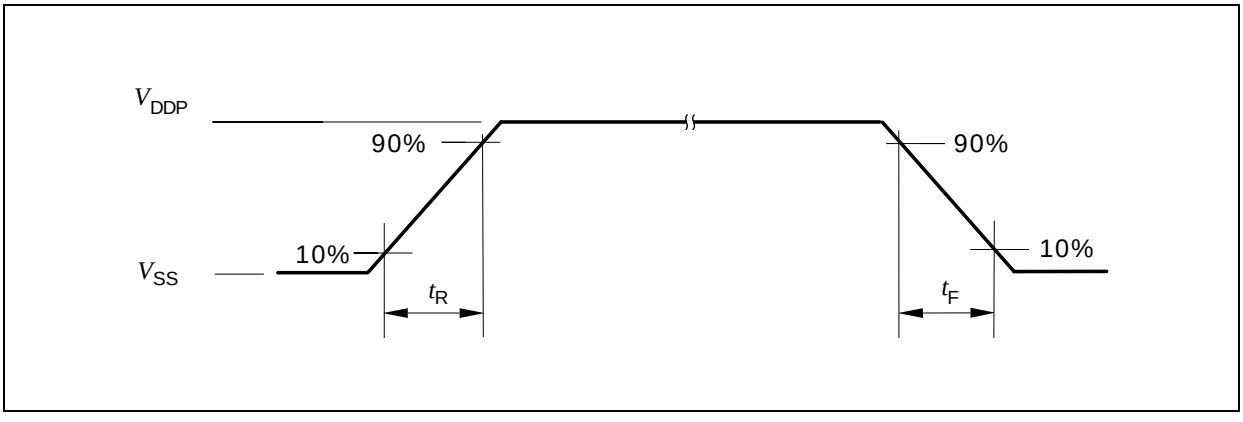


Figure 12 Rise/Fall Time Parameters

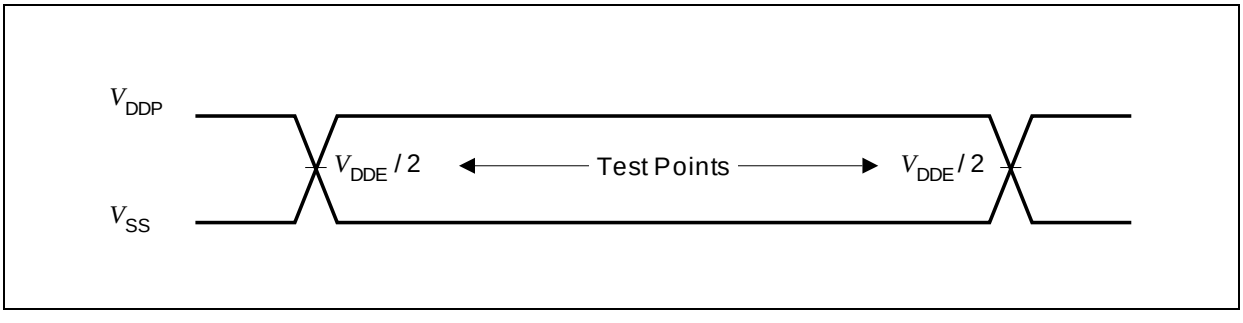


Figure 13 Testing Waveform, Output Delay

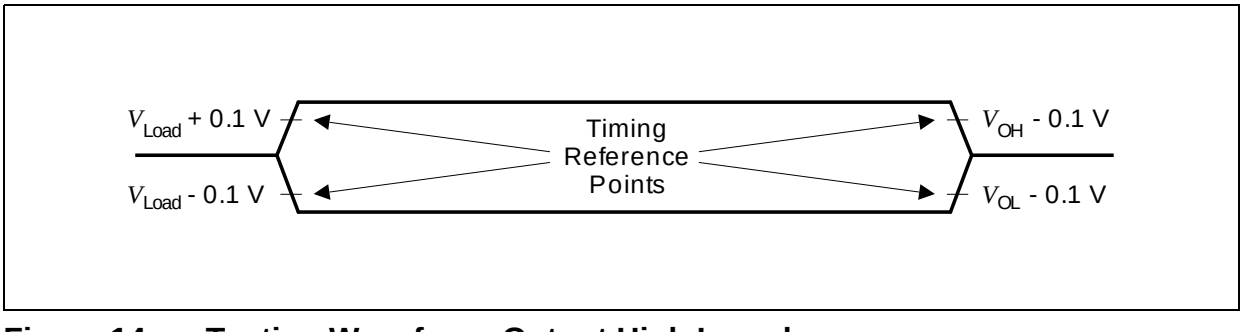


Figure 14 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 18 provides the characteristics of the output rise/fall times in the XC822/824.

Table 18 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	10	ns	20 pF[3)4)] (5 V & 3.3 V).

1) Rise/Fall time parameters are taken with 10% - 90% of supply.

2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

3) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF @ 0.125 ns/pF at 5 V supply voltage.

4) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF.@ 0.225 ns/pF at 3.3 V supply voltage.

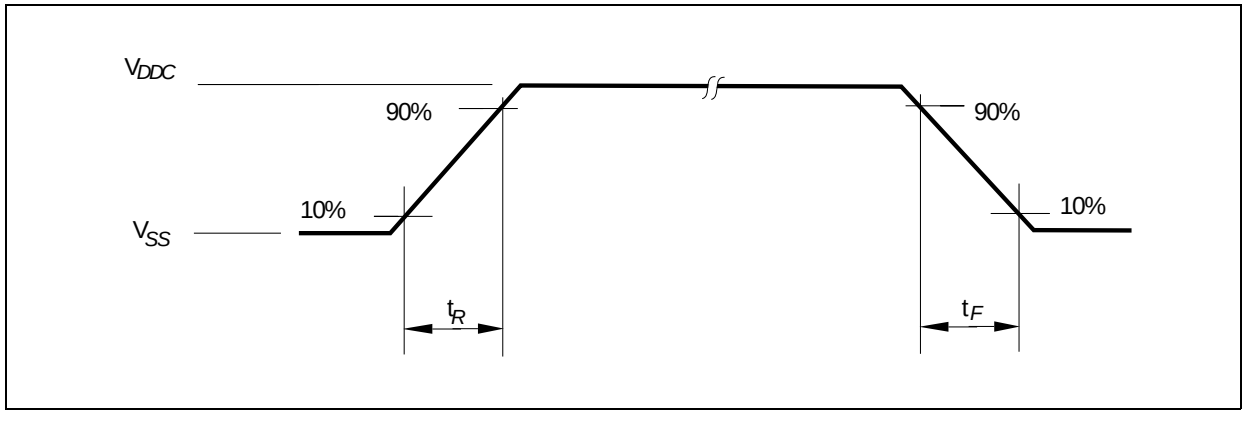


Figure 15 Rise/Fall Times Parameters

3.3.3 Oscillator Timing and Wake-up Timing

Table 19 provides the characteristics of the power-on reset, PLL and Wake-up timings in the XC822/824.

Table 19 Power-On Reset Wake-up Timing[1] (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
48 MHz Oscillator start-up time	$t_{48MOSCST}$	CC	–	–	13	µs	
75 KHz Oscillator start-up time	$t_{75KOSCST}$	CC	–	–	800	µs	
Flash initialization time	t_{FINT}	CC	–	160	–	µs	

1) Not subject to production test, verified by design/characterisation.

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 48 MHz oscillator in the XC822/824.

Table 20 48 MHz Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	-0.5 %	48	+0.5%	MHz	under nominal conditions[1] after trimming
Long term frequency deviation	Δf_{LT}	CC	-2.0	–	3.0	%	with respect to f_{NOM}, over lifetime and temperature (0 °C to 85 °C)
			-4.5	–	4.5	%	with respect to f_{NOM}, over lifetime and temperature (-40 °C to 125 °C)
Short term frequency deviation (over core supply voltage[2])	Δf_{ST}	CC	-1	–	1	%	with respect to f_{NOM}, within one LIN message (< 10 ms … 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

2) Core voltage supply, V_{DDC} = 2.5 V ± 7.5%.

3.3.5.2 SSC Slave Mode Timing

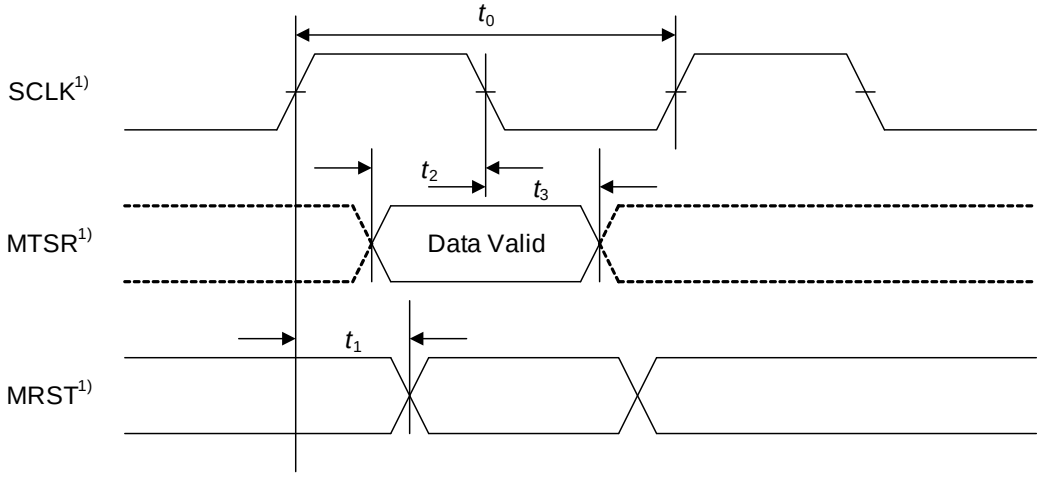
Table 23 provides the SSC slave mode timing in the XC822/824.

Table 23 SSC Slave Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	SR	4 * T_{SSC}[2]	–	ns
MRST delay from SCLK	t_1	CC	0	20	ns
MTSR setup to SCLK	t_2	SR	46	–	ns
MTSR hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 166.7 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup : CON.PH = CON.PO = 0.

Figure 17 SSC Slave Mode Timing