Infineon Technologies - XC822T1FRIAAFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc822t1friaafxuma1

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC822/824.

2.1 Block Diagram

The block diagram of the XC822/824 is shown in **Figure 2**.

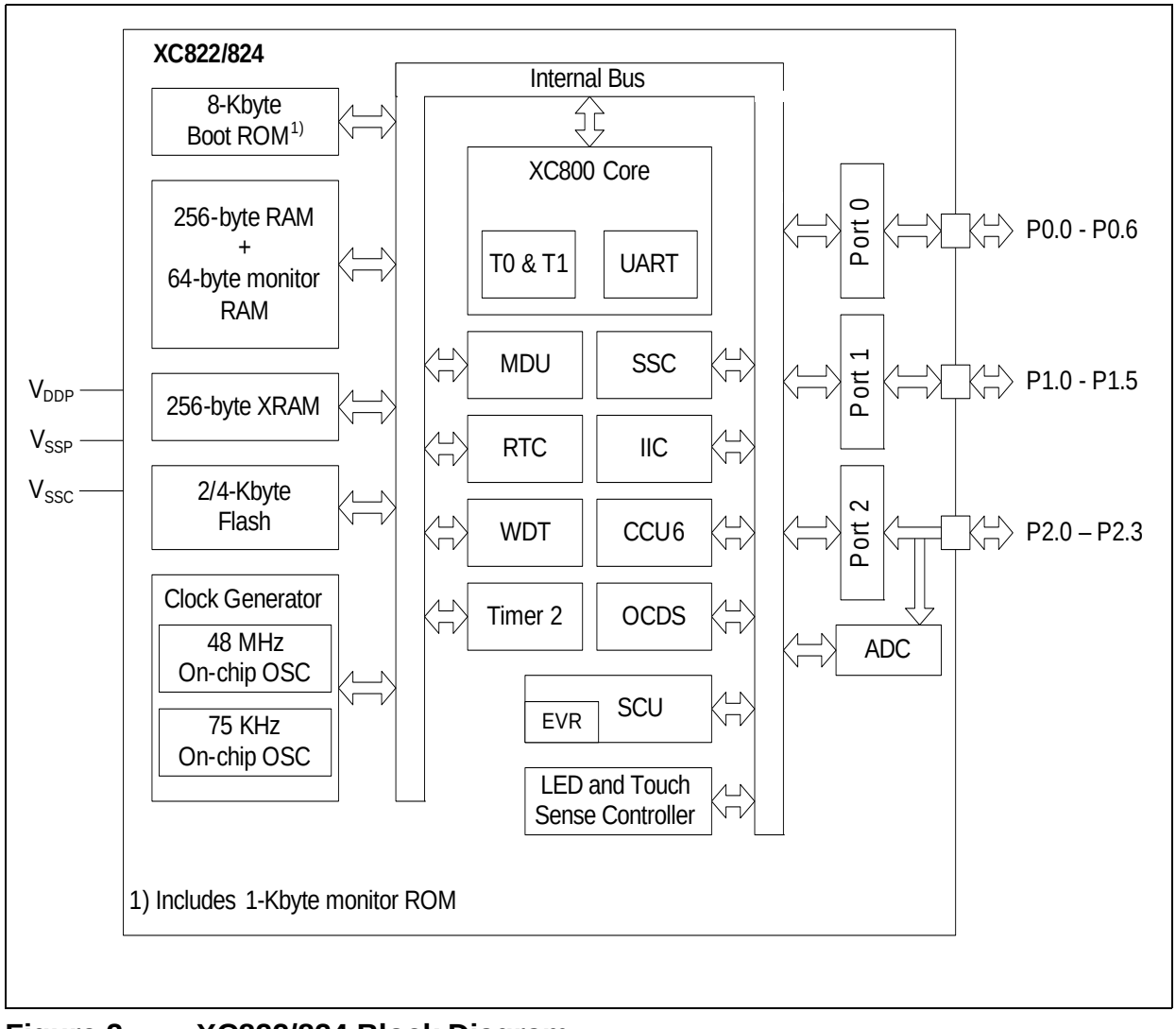


Figure 2 XC822/824 Block Diagram

2.3 Pin Configuration

The pin configuration of the XC822 in **Figure 4**.

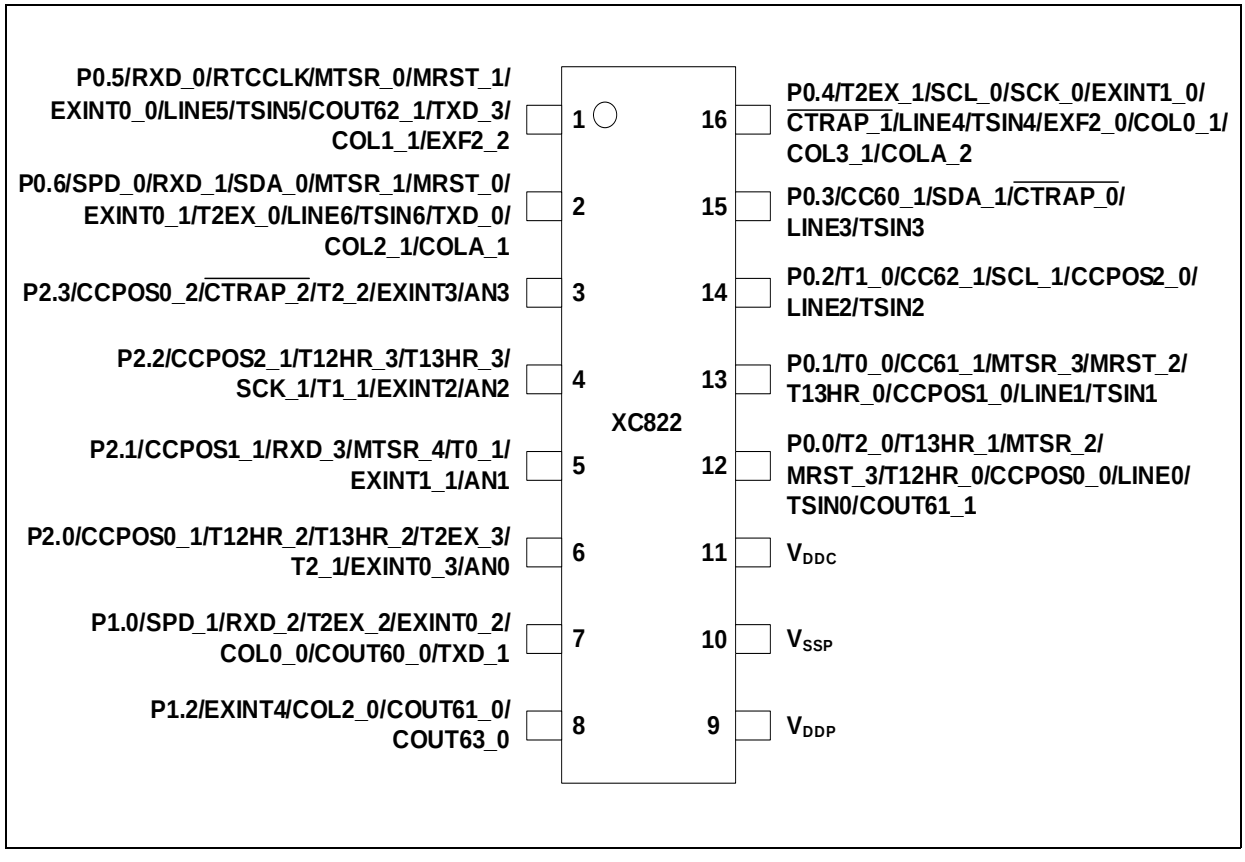


Figure 4 XC822 Pin Configuration, PG-TSSOP-16 Package (top view)

The pin configuration of the XC824 in **Figure 5**.

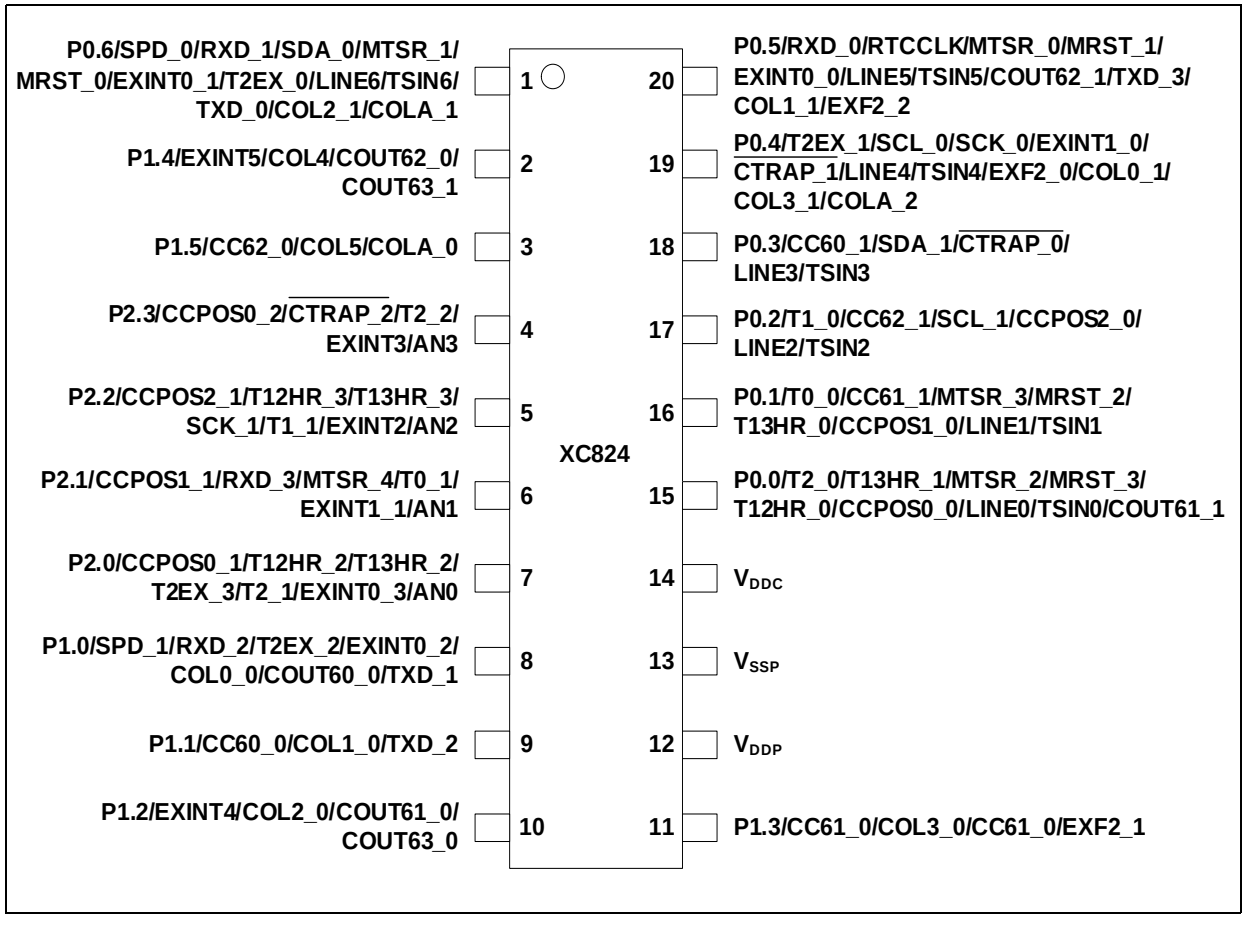


Figure 5 XC824 Pin Configuration, PG-DSO-20 Package (top view)

2.4 Pin Definitions and Functions

The functions and default states of the XC822/824 external pins are provided in **Table 3**.

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0		I/O		**Port 0** Port 0 is a bidirectional general purpose I/O port. It can be used as alternate functions for LEDTSCU, Timer 0, 1 and 2, SSC, CCU6, IIC, SPD and UART.	
P0.0	15/12		Hi-Z	T2_0	Timer 2 Input
				T13HR_1	CCU6 Timer 13 Hardware Run Input
				MTSR_2	SSC Master Transmit Output/ Slave Receive Input
				MRST_3	SSC Master Receive Input
				T12HR_0	CCU6 Timer 12 Hardware Run Input
				CCPOS0_0	CCU6 Hall Input 0
				TSIN0	Touch-sense Input 0
				LINE0	LED Line 0
				COUT61_1	Output of Capture/Compare Channel 1

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.4	19/16		PD	T2EX_1	Timer 2 External Trigger Input
				SCK_0	SSC Clock Input/Output
				SCL_0	IIC Clock Line
				$\overline{\text{CTRAP}}$_1	CCU6 Trap Input
				EXINT1_0	External Interrupt Input 1
				TSIN4	Touch-sense Input 4
				LINE4	LED Line 4
				EXF2_0	Timer 2 Overflow Flag
				COL0_1	LED Column 0
				COL3_1	LED Column 3
				COLA_2	LED Column A
P0.5	20/1		Hi-Z	RXD_0	UART Receive Input
				RTCCLK	RTC External Clock Input
				MTSR_0	SSC Master Transmit Output/ Slave Receive Input
				MRST_1	SSC Master Receive Input
				EXINT0_0	External Interrupt Input 0
				TSIN5	Touch-sense Input 5
				LINE5	LED Line 5
				COUT62_1	Output of Capture/Compare Channel 2
				TXD_3	UART Transmit Output/ 2-wire UART BSL Transmit Output
				COL1_1	LED Column 1
				EXF2_2	Timer 2 Overflow Flag

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P0.6	1/2		PU	SPD_0	SPD Input/Output
				RXD_1	UART Receive Input/ UART BSL Receive Input
				SDA_0	IIC Data Line
				MTSR_1	SSC Slave Receive Input
				MRST_0	SSC Master Receive Input/ Slave Transmit Output
				EXINT0_1	External Interrupt Input 0
				T2EX_0	Timer 2 External Trigger Input
				TSIN6	Touch-sense Input 6
				LINE6	LED Line 6
				TXD_0	UART Transmit Output/ 1-wire UART BSL Transmit Output
				COL2_1	LED Column 2
				COLA_1	LED Column A
P1		I/O		**Port 1** Port 1 is a bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, LEDTSCU, SPD, UART and Timer 2.	
P1.0	8/7		Hi-Z	SPD_1	SPD Input/Output
				RXD_2	UART Receive Input
				T2EX_2	Timer 2 External Trigger Input
				EXINT0_2	External Interrupt Input 0
				COL0_0	LED Column 0
				COUT60_0	Output of Capture/Compare Channel 0
				TXD_1	UART Transmit Output

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P2.0	7/6		Hi-Z	CCPOS0_1	CCU6 Hall Input 0
				T12HR_2	CCU6 Timer 12 Hardware Run Input
				T13HR_2	CCU6 Timer 13 Hardware Run Input
				T2EX_3	Timer 2 External Trigger Input
				T2_1	Timer 2 Input
				EXINT0_3	External Interrupt Input 0
				AN0	Analog Input 0 / Out of range comparator channel 0
P2.1	6/5		Hi-Z	CCPOS1_1	CCU6 Hall Input 1
				RXD_3	UART Receive Input
				MTSR_4	Slave Receive Input
				T0_1	Timer 0 Input
				EXINT1_1	External Interrupt Input 1
				AN1	Analog Input 1 / Out of range comparator channel 1
P2.2	5/4		Hi-Z	CCPOS2_1	CCU6 Hall Input 2
				T12HR_3	CCU6 Timer 12 Hardware Run Input
				T13HR_3	CCU6 Timer 13 Hardware Run Input
				SCK_1	SSC Clock Input/Output
				T1_1	Timer 1 Input
				EXINT2	External Interrupt Input 2
				AN2	Analog Input 2 / Out of range comparator channel 2

Table 3 Pin Definitions and Functions for XC822/824

Symbol	Pin Number DSO20/ TSSOP16	Type	Reset State	Function	
P2.3	4/3		Hi-Z	CCPOS0_2	CCU6 Hall Input 0
				$\overline{\text{CTRAP}}$_2	CCU6 Trap Input
				T2_2	Timer 2 Input
				EXINT3	External Interrupt Input 3
				AN3	Analog Input 3 / Out of range comparator channel 3
V_{DDP}	12/9	–		I/O Port Supply (2.5 V - 5.5 V)	
V_{DDC}	14/11	–		Core Supply Output (2.5 V)	
V_{SSP}/ V_{SSC}	13/10	–		I/O Port Ground/ Core Supply Ground	

2.5 Memory Organization

The XC822/824 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM, Library ROM and User routines
- 256 bytes of internal RAM
- 256 bytes of XRAM
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 2/4 Kbytes of Flash

Figure 6 illustrates the memory address spaces of the 2 Kbyte Flash devices. There are two 1-Kbyte sectors in this device. **Figure 7** illustrates the memory address spaces of the 4 Kbyte Flash devices. This device has two 1-Kbyte sectors, two 512-byte sectors, two 256-byte sectors and four 128-byte sectors. **Figure 8** shows the Flash sectorization for 2 Kbyte and 4 Kbyte Flash devices.

3.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC822/824 can be subjected to without permanent damage.

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 8 Input/Output Characteristics of XC822/XC824 (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Pull-down current on port pins	I_{PDP}	CC	–	20	µA	$V_{IL,max}$ (5 V)
			150	–	µA	$V_{IH,min}$ (5 V)
			–	5	µA	$V_{IL,max}$ (3.3 V)
			100	–	µA	$V_{IH,min}$ (3.3 V)
Input leakage current on port pins[2)]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125$ °C
Overload current on any pin	I_{OVP}	SR	-5	5	mA	3)
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$	SR	–	25	mA	3)
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	4)
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M	SR	-15	25	mA	–
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	80	mA	3)
Maximum current out of V_{SS}	I_{MVSS}	SR	–	80	mA	3)

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.3 ADC Characteristics

The values in **Table 10** are given for an analog power supply of 5.0 V. The ADC can be used with an analog power supply down to 3 V. But in this case, analog parameters may show a reduced performances. In the reduced voltage mode (2.5 V < V_{DDP} < 3 V), the ADC is not recommended to be used.

Table 10 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5 V)

Parameter	Symbol		Limit Values			Unit	Test Conditions / Remarks
			Min.	Typ.	Max.		
Analog reference voltage	V_{AREF}		–	V_{DDP}	–	V	Connect internally to V_{DDP}
Analog reference ground	V_{AGND}		–	V_{SSP}	–	V	Connect internally to V_{SSP}
Alternate analog reference ground	$V_{AGNDALT}$	SR	V_{SSP} - 0.1	–	2.5[1]	V	Connect to AN0 in differential mode, See **Figure 10**.
Internal voltage reference	V_{INTREF}	SR	1.19	1.23	1.28	V	[3]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	–
ADC clock	f_{ADCI}		8	–	16	MHz	internal analog clock
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	–
Conversion time	t_C	CC	See **Section 3.2.3.1**			µs	–
Total unadjusted error	*TUE*[2]	CC	–	–	±1	LSB8	8-bit conversion with internal reference[3]
			–	–	+4/-1	LSB10	10-bit conversion with internal reference[3][4]
			–	–	+14/-2	LSB12	12-bit conversion using the Low Pass Filter [3]
Differential Nonlinearity	EA_{DNL}	CC	–	–	+1.5/ -1	LSB	10-bit conversion[3]

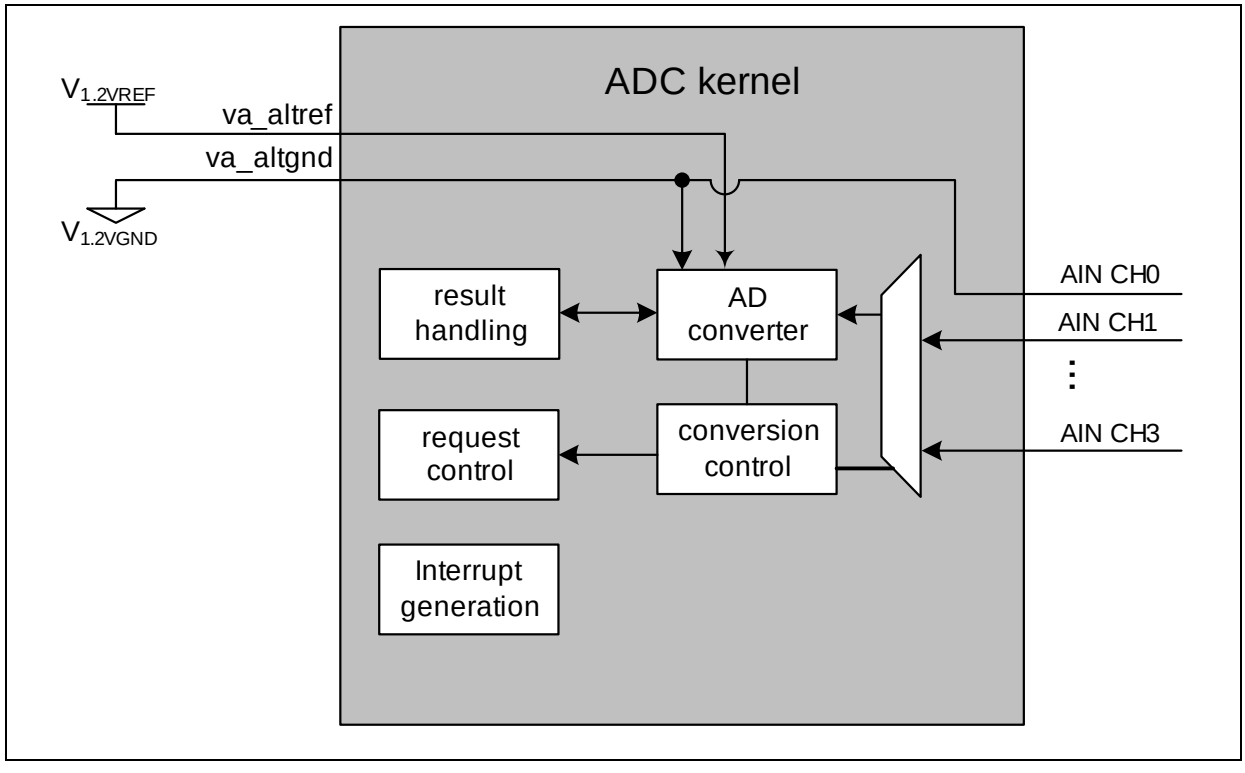


Figure 10 Differential like measurement with internal 1.2V voltage reference, and CH0 gnd.

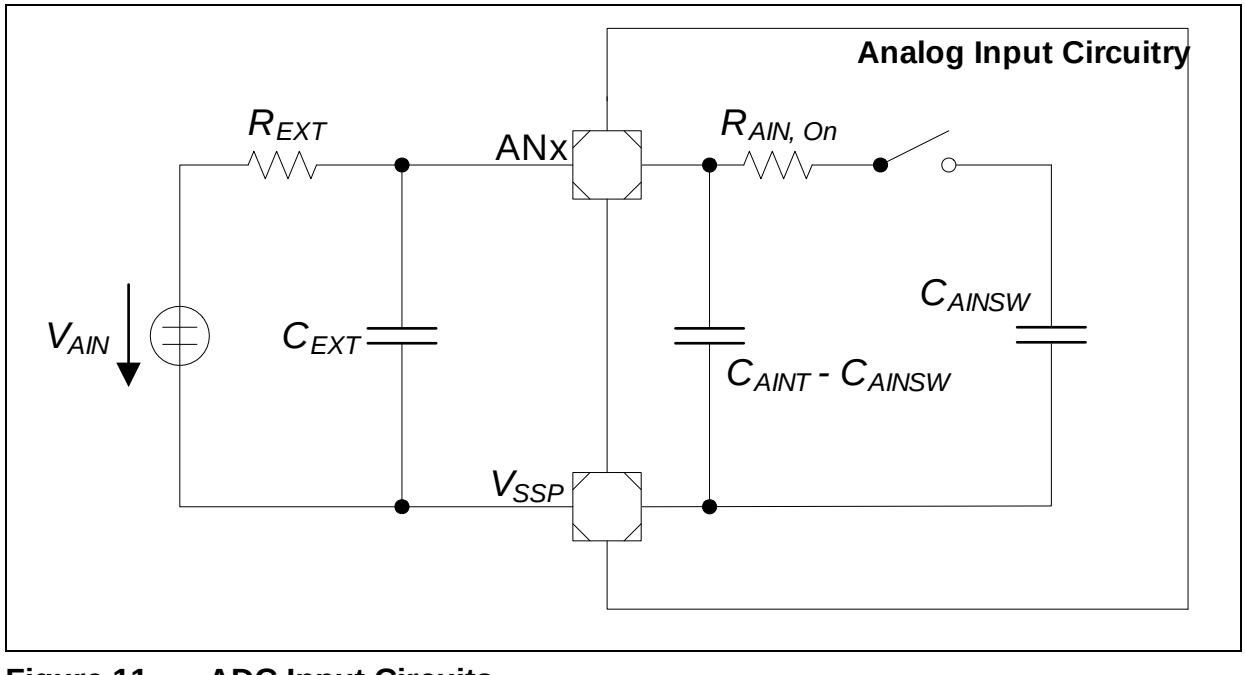


Figure 11 ADC Input Circuits

Table 14 Emulated Flash Data Retention and Endurance based on EEPROM Emulation ROM Library (Operating Conditions apply)[1)]

Retention	Endurance[2)]	Emulation Size	Remarks
2 years	1,600,000 cycles	31 bytes	
2 years	1,400,000 cycles	62 bytes	
2 years	1,200,000 cycles	93 bytes	
2 years	1,000,000 cycles	124 bytes	

1) EEPROM Emulation ROM Library can only be used in the 4 Kbyte Flash variant.

2) These values show the maximum endurance. Maximum endurance is the maximum possible unique data write if each data update is only 31 bytes. Minimum endurance cycle is the maximum possible unique data write if each data update is the same as the emulation size. The minimum endurance cycle can be calculated using the formulae [(max. endurance)*(31)/(emulation size)].

Table 16 shows the maximum active current within the device in the reduced voltage condition of 2.5 V < V_{DDP} < 3.0 V. The active current consumption needs to be below the specified values as according to the V_{DDP} voltage. If the conditions are not met, a brownout reset may be triggered.

Table 16 Active Current Consumption in Reduced Voltage Condition

V_{DDP}	2.5 V	2.6 V	2.7 V	2.8 V
Maximum active current	7 mA	13 mA	20 mA	25 mA

Table 17 provides the active current consumption of some modules operating at 8 MHz active mode, 3 V power supply at 25 °C. The typical values shown are used as a reference guide for device operating in reduced voltage conditions.

Table 17 Typical Active Current Consumption[1) 2)]

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current[3)]	I_{CPUDDC}	5850	µA	Modules including Core, memories, UART, T0, T1 and EVR. Disable ADC analog (GLOBCTR.ANON = 0).
ADC[4)]	I_{ADCDDC}	3390	µA	Set PMCON1.ADC_DIS to 0 and GLOBECTR. ANON to 1
SSC[5)]	I_{SSCDDC}	460	µA	Set PMCON1.SSC_DIS to 0
CCU6[6)]	$I_{CCU6DDC}$	3320	µA	Set PMCON1.CCU_DIS to 0
Timer 2[7)]	I_{T2DDC}	200	µA	Set PMCON1.T2_DIS to 0
MDU[8)]	I_{MDUDDC}	1260	µA	Set PMCON1.MDU_DIS to 0
LEDTSCU[9)]	I_{LEDDDC}	520	µA	Set PMCON1.LTS_DIS to 0
IIC[10)]	I_{IICDDC}	580	µA	Set PMCON1.IIC_DIS to 0

1) Modules that are controllable by programming the register PMCON1.

2) Not subject to production test, verified by design/characterisation.

3) Baseload current is measured when the device is running in user mode with an endless loop in the flash memory. All modules in register PMCON1 are disabled.

4) ADC active current is measured with: module enable, ADC analog clock at 8MHz, running in parallel conversion request in autoscan mode for 4 channels

5) SSC active curremt is measured with: module enabled, running in loop back mode at a baud rate of 1 MBaud

6) CCU6 active current is measured with: module enabled, all timers running in 8 MHz, 6 PWM outputs are generated.

7) Timer 2 active current is measured with: module enabled, timer running in 8 MHz

8) MDU active current is measured with: module enabled, division operation was performed.

3.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

3.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 12**, **Figure 13** and **Figure 14**.

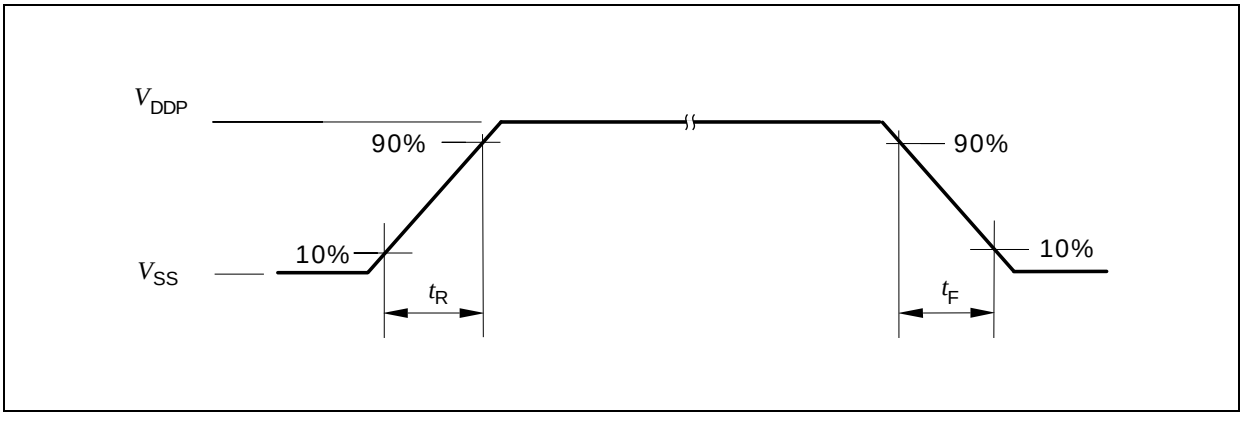


Figure 12 Rise/Fall Time Parameters

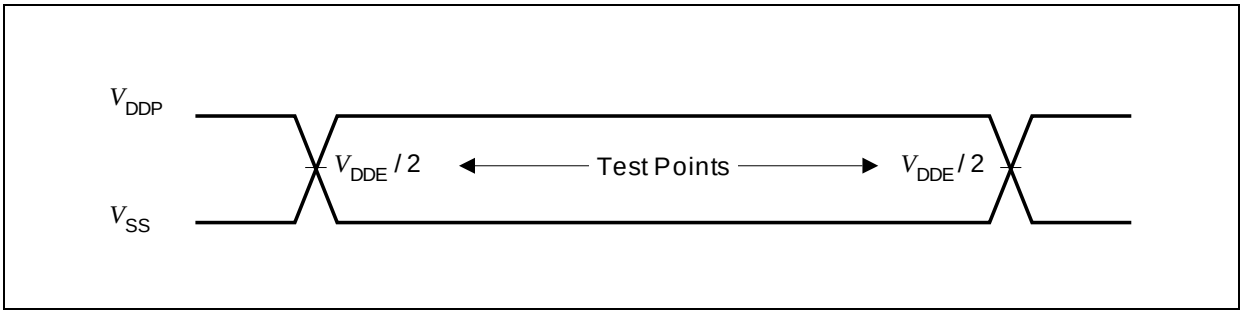


Figure 13 Testing Waveform, Output Delay

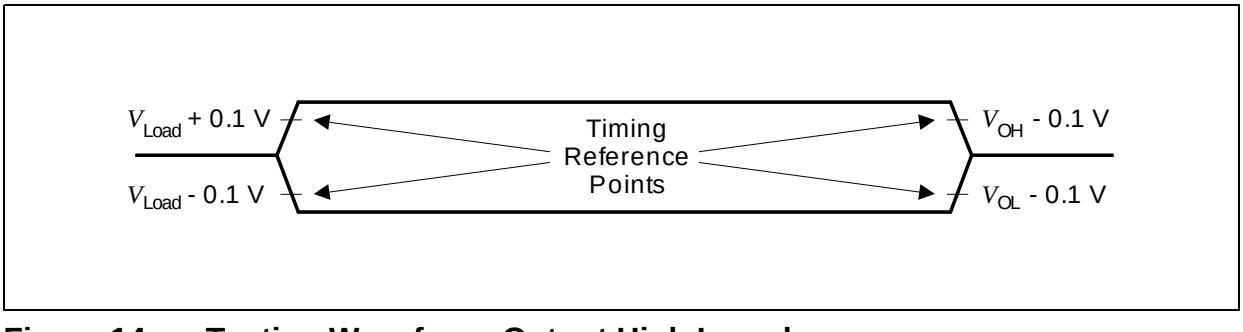


Figure 14 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 18 provides the characteristics of the output rise/fall times in the XC822/824.

Table 18 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	10	ns	20 pF[3)4)] (5 V & 3.3 V).

1) Rise/Fall time parameters are taken with 10% - 90% of supply.

2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

3) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF @ 0.125 ns/pF at 5 V supply voltage.

4) Additional rise/fall time valid for C_L = 20 pF - C_L = 100 pF.@ 0.225 ns/pF at 3.3 V supply voltage.

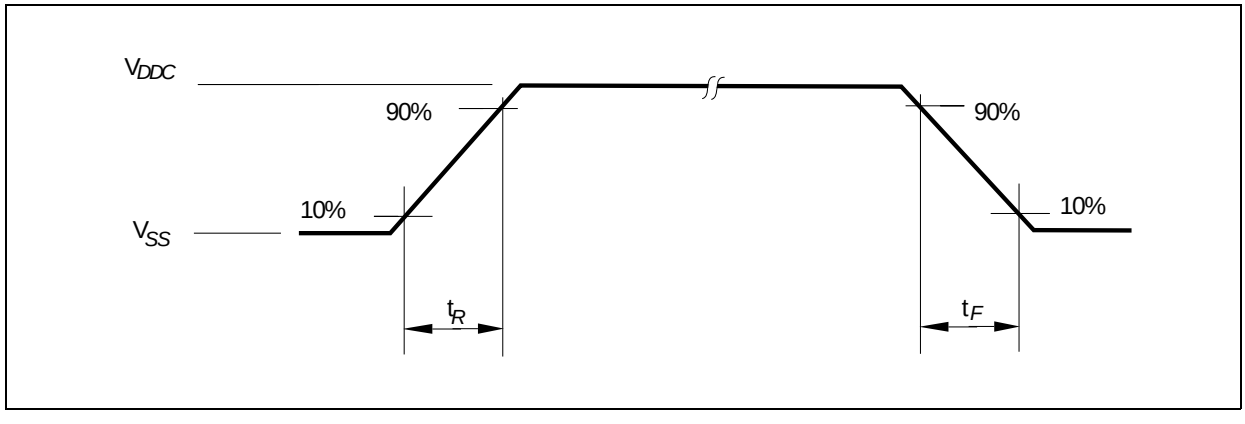


Figure 15 Rise/Fall Times Parameters

3.3.5.2 SSC Slave Mode Timing

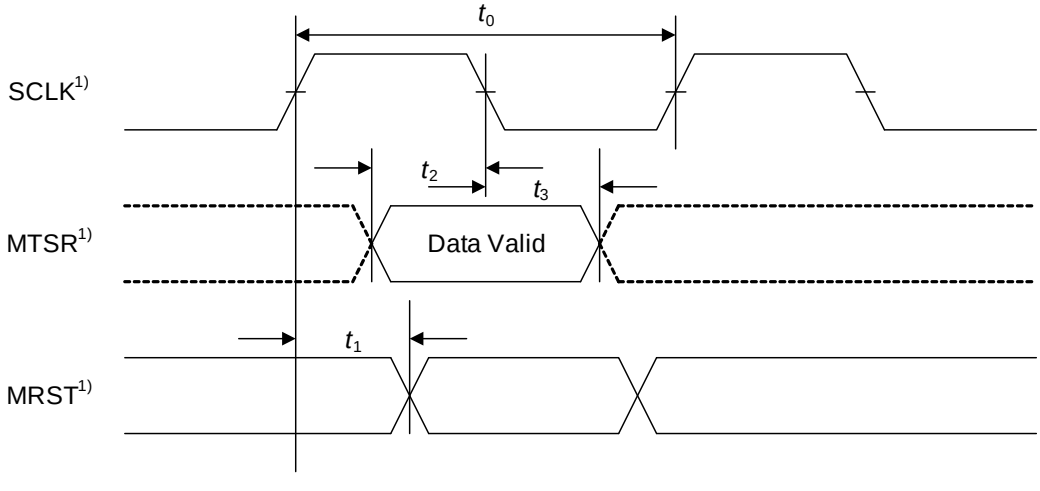
Table 23 provides the SSC slave mode timing in the XC822/824.

Table 23 SSC Slave Mode Timing[1] (Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
SCLK clock period	t_0	SR	4 * T_{SSC}[2]	–	ns
MRST delay from SCLK	t_1	CC	0	20	ns
MTSR setup to SCLK	t_2	SR	46	–	ns
MTSR hold from SCLK	t_3	SR	0	–	ns

1) Not subject to production test, verified by design/characterisation.

2) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When f_{CPU} = 24 MHz, t_0 = 166.7 ns. T_{CPU} is the CPU clock period.



1) This timing is based on the following setup : CON.PH = CON.PO = 0.

Figure 17 SSC Slave Mode Timing

4 Package and Quality Declaration

Chapter 4 provides the information of the XC822/824 package and reliability section.

4.1 Package Parameters

Table 24 provides the thermal characteristics of the packages used in XC822 and XC824 respectively.

Table 24 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Package Types
			Min.	Max.		
Thermal resistance junction case[1)]	R_{TJC}	CC	-	36.2	K/W	PG-TSSOP-16-1
			-	34.3	K/W	PG-DSO-20-45
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	356.6	K/W	PG-TSSOP-16-1
			-	36.2	K/W	PG-DSO-20-45

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.

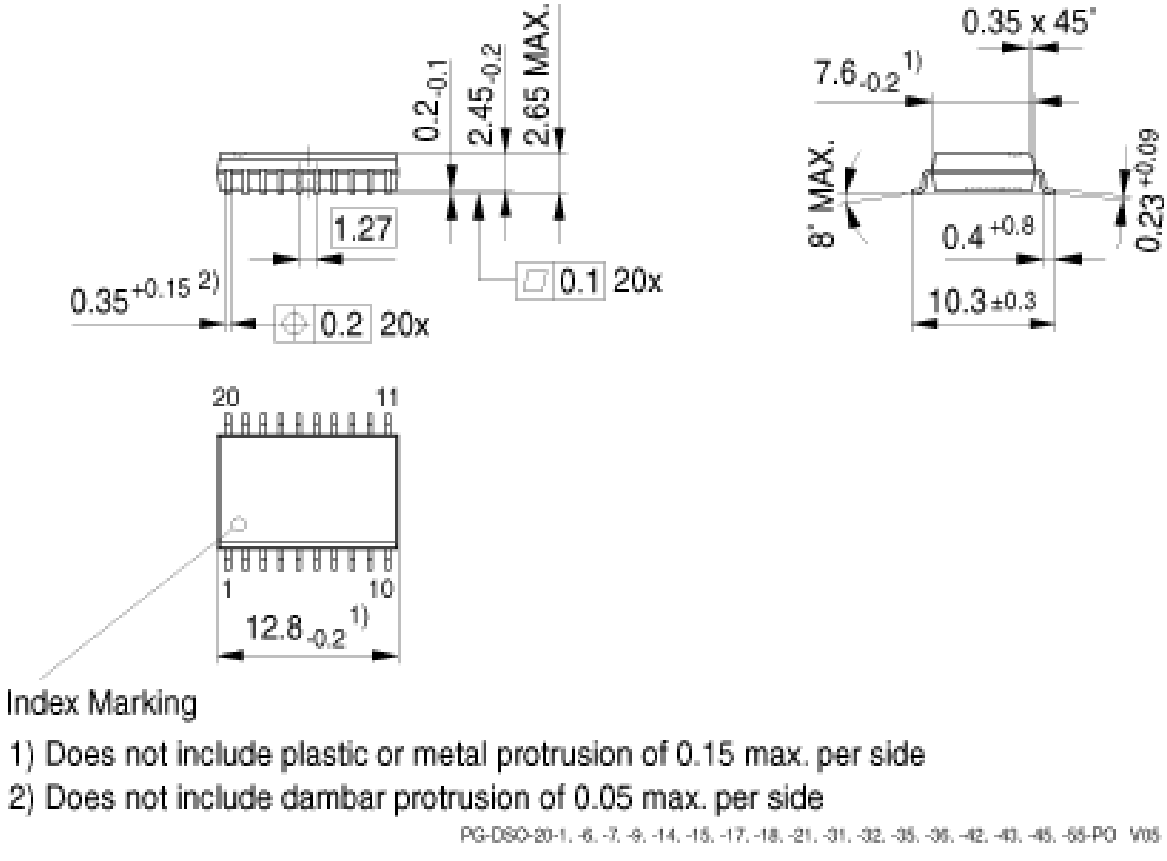


Figure 19 PG-DSO-20-45 Package Outline

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