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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kxpc8255cvvifbc

- Common on-chip processor (COP) test interface
- High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
 - G2 core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
 - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE Std 1149.1™ JTAG test access port
- Twelve-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
 - Byte write enables and selectable parity generation
 - 32-bit address decodes with programmable bank size
 - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
 - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
 - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)

- Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
- Interfaces to G2 core through on-chip 24-Kbyte dual-port RAM and DMA controller
- Serial DMA channels for receive and transmit on all serial channels
- Parallel I/O registers with open-drain and interrupt capability
- Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
- Three fast communications controllers (two on the MPC8255) supporting the following protocols:
 - 10/100-Mbit Ethernet/IEEE Std 802.3™ CDMA/CS interface through media independent interface (MII)
 - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
 - Transparent
 - HDLC—Up to T3 rates (clear channel)
- Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
 - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
- Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
 - Ethernet/IEEE 802.3 CDMA/CS
 - HDLC/SDLC and HDLC bus
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BISYNC) communications
 - Transparent
- Two serial management controllers (SMCs), identical to those of the MPC860
 - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
 - Transparent
 - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I²C) controller (identical to the MPC860 I²C controller)
 - Microwire compatible
 - Multiple-master, single-master, and slave modes

- Up to eight TDM interfaces (4 on the MPC8255)
 - Supports two groups of four TDM channels for a total of eight TDMs
 - 2,048 bytes of SI RAM
 - Bit or byte resolution
 - Independent transmit and receive routing, frame synchronization
 - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8260.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8260. [Table 1](#) shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings¹

Rating	Symbol	Value	Unit
Core supply voltage ²	VDD	-0.3 – 2.75	V
PLL supply voltage ²	VCCSYN	-0.3 – 2.75	V
I/O supply voltage ³	VDDH	-0.3 – 4.0	V
Input voltage ⁴	VIN	GND(-0.3) – 3.6	V
Junction temperature	T _j	120	°C
Storage temperature range	T _{STG}	(-55) – (+150)	°C

Note:

¹ Absolute maximum ratings are stress ratings only; functional operation (see [Table 2](#)) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

² **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

³ **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.0 V during normal operation.

⁴ **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions¹

Rating	Symbol	2.5-V Device ²	Unit
Core supply voltage	VDD	2.4–2.7	V
PLL supply voltage	VCCSYN	2.4–2.7	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (–0.3) – 3.465	V
Junction temperature (maximum)	T _j	105	°C

¹ **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

² Parts labeled with an “-HVA” suffix are 2.6-V devices.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

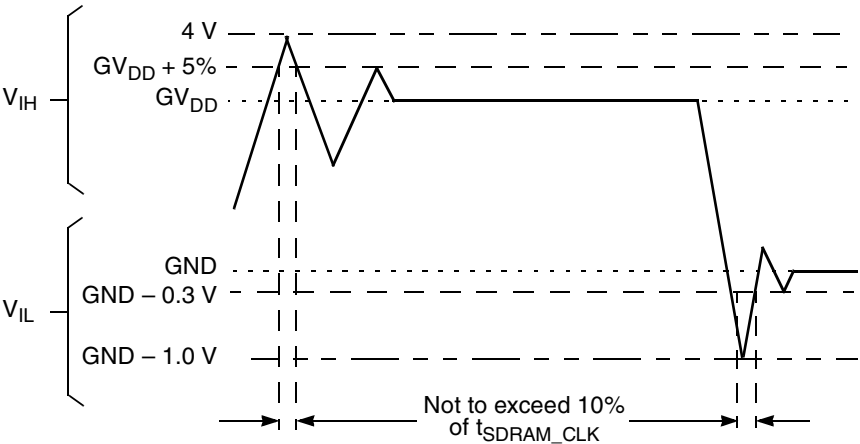


Figure 2. Overshoot/Undershoot Voltage

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 7.0\text{mA}$ \overline{BR} \overline{BG} $\overline{ABB}/\overline{IRQ2}$ \overline{TS} $A[0-31]$ $TT[0-4]$ \overline{TBST} $TSIZE[0-3]$ \overline{AACK} \overline{ARTRY} \overline{DBG} $\overline{DBB}/\overline{IRQ3}$ $D[0-63]$ $DP(0)/\overline{RSRV}/\overline{EXT_BR2}$ $DP(1)/\overline{IRQ1}/\overline{EXT_BG2}$ $DP(2)/\overline{TLBISYNC}/\overline{IRQ2}/\overline{EXT_DBG2}$ $DP(3)/\overline{IRQ3}/\overline{EXT_BR3}/\overline{CKSTP_OUT}$ $DP(4)/\overline{IRQ4}/\overline{EXT_BG3}/\overline{CORE_SREST}$ $DP(5)/\overline{TBEN}/\overline{IRQ5}/\overline{EXT_DBG3}$ $DP(6)/\overline{CSE(0)}/\overline{IRQ6}$ $DP(7)/\overline{CSE(1)}/\overline{IRQ7}$ \overline{PSDVAL} \overline{TA} \overline{TEA} $\overline{GBL}/\overline{IRQ1}$ $\overline{CI}/\overline{BADDR29}/\overline{IRQ2}$ $\overline{WT}/\overline{BADDR30}/\overline{IRQ3}$ $\overline{L2_HIT}/\overline{IRQ4}$ $\overline{CPU_BG}/\overline{BADDR31}/\overline{IRQ5}$ $\overline{CPU_DBG}$ $\overline{CPU_BR}$ $\overline{IRQ0}/\overline{NMI_OUT}$ $\overline{IRQ7}/\overline{INT_OUT}/\overline{APE}$ $\overline{PORESET}$ \overline{HRESET} \overline{SRESET} $\overline{RSTCONF}$ \overline{QREQ}	V_{OL}	—	0.4	V

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μ F by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8260 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above $P_D = 3W$ (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations¹

Bus (MHz)	CPM Multiplier	CPU Multiplier	CPM (MHz)	CPU (MHz)	$P_{INT} (W)^2$				
					Vddl				
					2.4	2.5	2.6	2.7	2.8 ³
33.3	4	4	133.3	133.3	2.04	2.14	2.26	2.38	2.50
50.0	2	3	100	150.0	2.21	2.30	2.45	2.59	2.69
66.7	2	2.5	133.3	166.7	2.47	2.62	2.74	2.88	3.02
66.7	2.5	2.5	166.7	166.7	2.57	2.69	2.83	2.98	3.12
66.7	2	3	133.3	200.0	2.81	2.95	3.12	3.29	3.43
66.7	2.5	3	166.7	200.0	2.88	3.05	3.22	3.38	3.55
50.0	3	4	150	200.0	2.83	3.00	3.14	3.31	3.48

Note:

¹ Test temperature = room temperature (25° C)

² $P_{INT} = I_{DD} \times V_{DD}$ Watts

³ 2.8 Vddl does not apply to HiP3 Rev C silicon.

Table 8. AC Characteristics for CPM Inputs¹

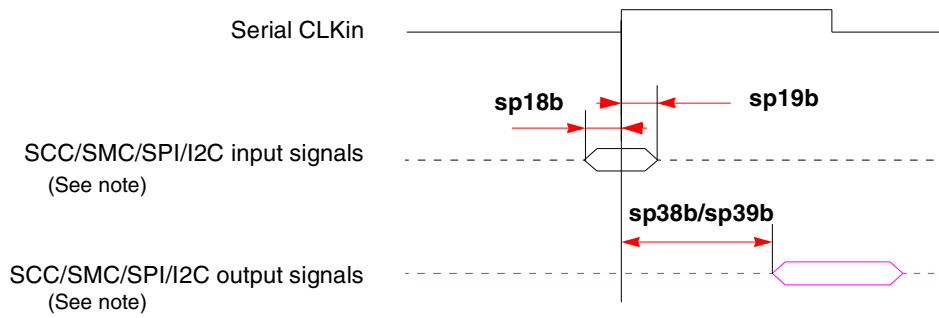
Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	3
sp20	sp21	TDM inputs/SI	15	12
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	5
sp22	sp23	PIO/TIMER/IDMA inputs	10	3

Note:

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 5 shows the SCC/SMC/SPI/I²C external clock.

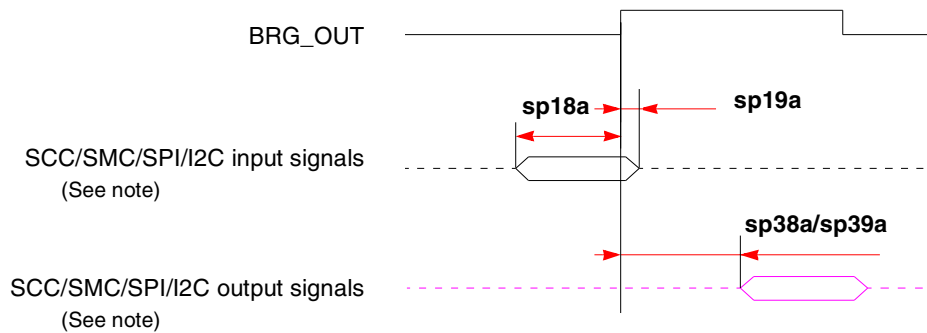


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I²C External Clock Diagram

Figure 6 shows the SCC/SMC/SPI/I²C internal clock.



Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs¹

Spec Number		Characteristic	Max Delay (ns)	Min Delay (ns)
Max	Min		66 MHz	66 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	10	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	0.5
sp33a	sp30	Data bus	8	0.5
sp33b	sp30	DP	12	0.5
sp34	sp30	memc signals/ALE	6	0.5
sp35	sp30	all other signals	7.5	0.5

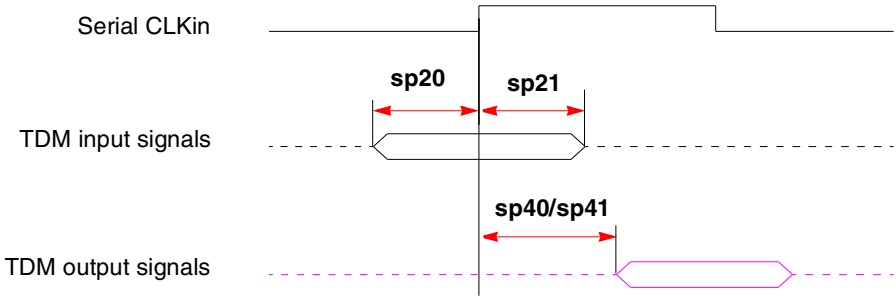
Note:

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 8 shows TDM input and output signals.



- Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
 2. Input sampled on the rising edge and output driven on the falling edge.
 3. Input sampled on the falling edge and output driven on the falling edge.
 4. Input sampled on the falling edge and output driven on the rising edge.

Figure 8. TDM Signal Diagram

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLK_{in}'s rising edge.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 12 shows the eight basic configuration modes. Another 49 modes are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 12 describes default clock modes for the MPC8260.

Table 12. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 13 describes all possible clock configurations when using the hard reset configuration sequence. Note also that basic modes are shown in boldface type.

Table 13. Clock Configuration Modes¹

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3,4}	CPM Multiplication Factor ^{2, 5}	CPM Frequency ²	Core Multiplication Factor ^{2, 6}	Core Frequency ²
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 13. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3,4}	CPM Multiplication Factor ^{2, 5}	CPM Frequency ²	Core Multiplication Factor ^{2, 6}	Core Frequency ²
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	33 MHz	4	133 MHz	4	133 MHz
0010_011	33 MHz	4	133 MHz	5	166 MHz
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

Table 13. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3,4}	CPM Multiplication Factor ^{2, 5}	CPM Frequency ²	Core Multiplication Factor ^{2, 6}	Core Frequency ²
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	66 MHz	2	133 MHz	2.5	166 MHz
0101_111	66 MHz	2	133 MHz	3	200 MHz
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	66 MHz	2.5	166 MHz	2.5	166 MHz
0110_101	66 MHz	2.5	166 MHz	3	200 MHz
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

Note:

- ¹ Because of speed dependencies, not all of the possible configurations in [Table 13](#) are applicable.
- ² The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU ranges between 133–200 and the CPM ranges between 50–166 MHz.
- ³ Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.
- ⁴ 60x and local bus frequency. Identical to CLKIN.
- ⁵ CPM multiplication factor = CPM clock/bus clock
- ⁶ CPU multiplication factor = Core PLL multiplication factor

4 Pinout

This section provides the pin assignments and pinout list for the MPC8260.

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

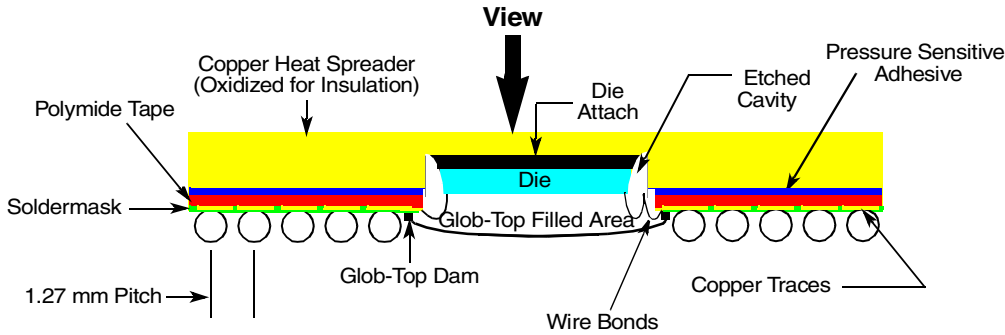


Figure 14. Side View of the TBGA Package

Table 14 shows the pinout list of the MPC8260. Table 15 defines conventions and acronyms used in Table 14.

Table 14. Pinout List

Pin Name	Ball
$\overline{\text{BR}}$	W5
$\overline{\text{BG}}$	F4
$\overline{\text{ABB/IRQ2}}$	E2
$\overline{\text{TS}}$	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1

Table 14. Pinout List (continued)

Pin Name	Ball
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
$\overline{\text{TBST}}$	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
$\overline{\text{AACK}}$	F3
$\overline{\text{ARTRY}}$	E1
$\overline{\text{DBG}}$	V1
$\overline{\text{DBB/IRQ3}}$	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6

Table 14. Pinout List (continued)

Pin Name	Ball
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17

Table 14. Pinout List (continued)

Pin Name	Ball
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/RSRV/EXT_BR2	B22
IRQ1/DP1/EXT_BG2	A22
IRQ2/DP2/TLBISYNC/EXT_DBG2	E21
IRQ3/DP3/CKSTP_OUT/EXT_BR3	D21
IRQ4/DP4/CORE_SRESET/EXT_BG3	C21
IRQ5/DP5/TBEN/EXT_DBG3	B21
IRQ6/DP6/CSE0	A21
IRQ7/DP7/CSE1	E20
PSDVAL	V3
TA	C22
TEA	V5
GBL/IRQ1	W1
CI/BADDR29/IRQ2	U2

Table 14. Pinout List (continued)

Pin Name	Ball
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/RESTART1/DREQ3/FCC2_UTM_TXADDR2	AC29 ²
PA1/REJECT1/FCC2_UTM_TXADDR1/DONE3	AC25 ²
PA2/CLK20/FCC2_UTM_TXADDR0/DACK3	AE28 ²
PA3/CLK19/FCC2_UTM_RXADDR0/DACK4/L1RXD1A2	AG29 ²
PA4/REJECT2/FCC2_UTM_RXADDR1/DONE4	AG28 ²
PA5/RESTART2/DREQ4/FCC2_UTM_RXADDR2	AG26 ²
PA6/L1RSYNCA1	AE24 ²
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25 ²
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23 ²
PA9/SMTXD2/L1TXD0A1	AH23 ²
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22 ²
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22 ²
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21 ²
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20 ²
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19 ²
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18 ²
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17 ²
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16 ²
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16 ²
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15 ²
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13 ²
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13 ²

Table 14. Pinout List (continued)

Pin Name	Ball
PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1	AE3 ²
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/FCC2_MII_TX_EN	AE2 ²
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5 ²
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4 ²
PC0/DREQ1/BRGO7/SMSYN2/L1CLKOA2	AB26 ²
PC1/DREQ2/BRGO6/L1RQA2	AD29 ²
PC2/FCC3_CD/FCC2_UT8_TXD3/DONE2	AE29 ²
PC3/FCC3_CTS/FCC2_UT8_TXD2/DACK2/CTS4	AE27 ²
PC4/FCC2_UTM_RXENB/FCC2_UTS_RXENB/SI2_L1ST4/FCC2_CD	AF27 ²
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/FCC2_CTS	AF24 ²
PC6/FCC1_CD/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR2/FCC1_UTM_RXCLAV1	AJ26 ²
PC7/FCC1_CTS/L1RQC1/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/FCC1_UTM_TXCLAV1	AJ25 ²
PC8/CD4/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/CTS3	AF22 ²
PC9/CTS4/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21 ²
PC10/CD3/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20 ²
PC11/CTS3/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19 ²
PC12/CD2/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18 ²
PC13/CTS2/CLSN2/L1RQD1/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18 ²
PC14/CD1/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17 ²
PC15/CTS1/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16 ²
PC16/CLK16/TIN4	AF15 ²
PC17/CLK15/TIN3/BRGO8	AJ15 ²
PC18/CLK14/TGATE2	AH14 ²
PC19/CLK13/BRGO7/SPICLK	AG13 ²
PC20/CLK12/TGATE1	AH12 ²
PC21/CLK11/BRGO6	AJ11 ²
PC22/CLK10/DONE1	AG10 ²
PC23/CLK9/BRGO5/DACK1	AE10 ²
PC24/FCC2_UT8_TXD3/CLK8/TOUT4	AF9 ²
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8 ²
PC26/CLK6/TOUT3/TMCLK	AJ6 ²
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2 ²
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	AF3 ²

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

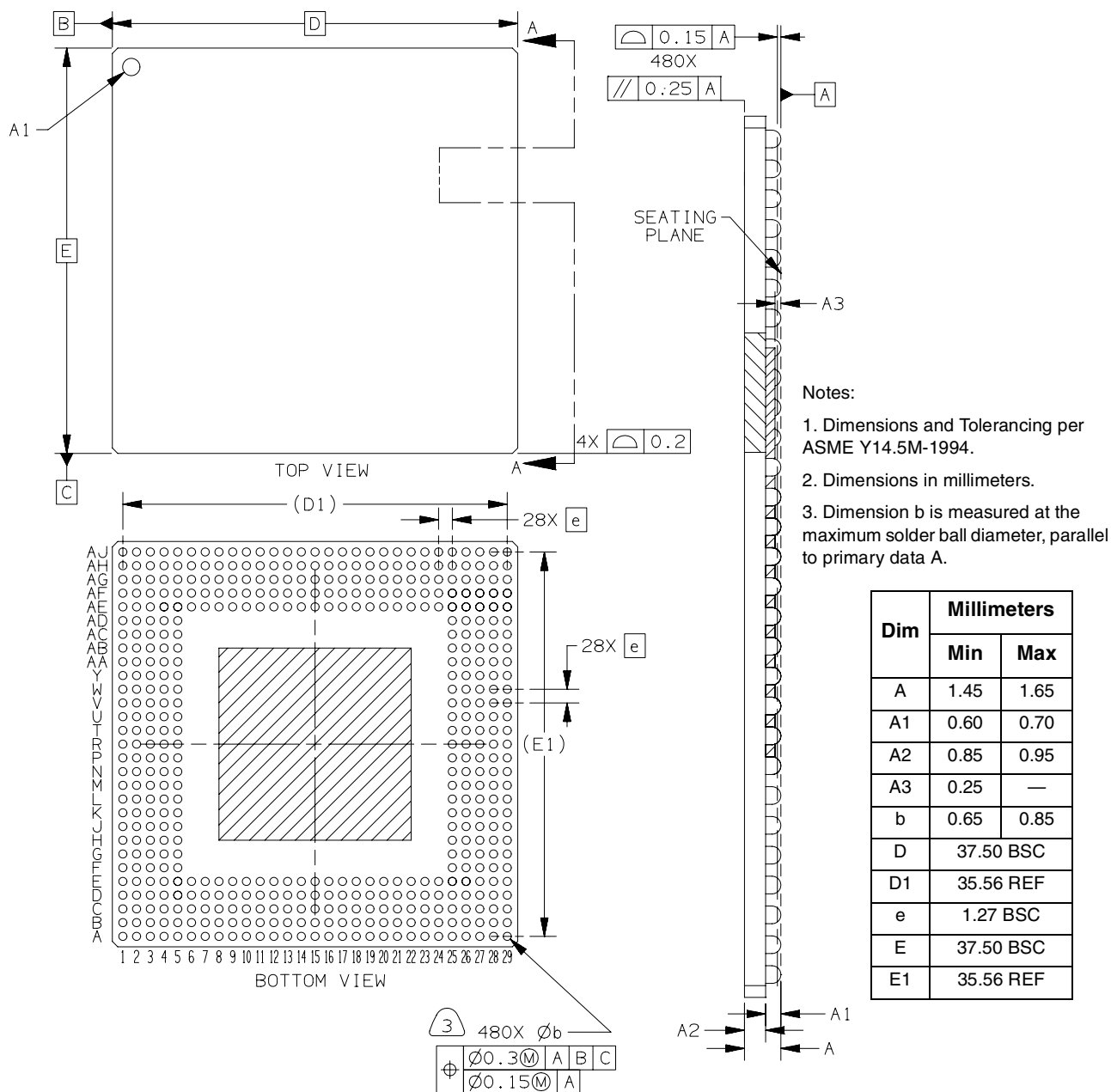


Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature