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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kxpc8255vvifbc

— Up to eight TDM interfaces (4 on the MPC8255)
  – Supports two groups of four TDM channels for a total of eight TDMs
  – 2,048 bytes of SI RAM
  – Bit or byte resolution
  – Independent transmit and receive routing, frame synchronization
  – Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
— Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
— Four independent 16-bit timers that can be interconnected as two 32-bit timers

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8260.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8260. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	-0.3 – 2.75	V
PLL supply voltage[2]	VCCSYN	-0.3 – 2.75	V
I/O supply voltage[3]	VDDH	-0.3 – 4.0	V
Input voltage[4]	VIN	GND(-0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(-55) – (+150)	°C

Note:

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.
3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.0 V during normal operation.
4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions[1]

Rating	Symbol	2.5-V Device[2]	Unit
Core supply voltage	VDD	2.4–2.7	V
PLL supply voltage	VCCSYN	2.4–2.7	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (-0.3) – 3.465	V
Junction temperature (maximum)	T_j	105	°C

1 **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

2 Parts labeled with an “-HVA” suffix are 2.6-V devices.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

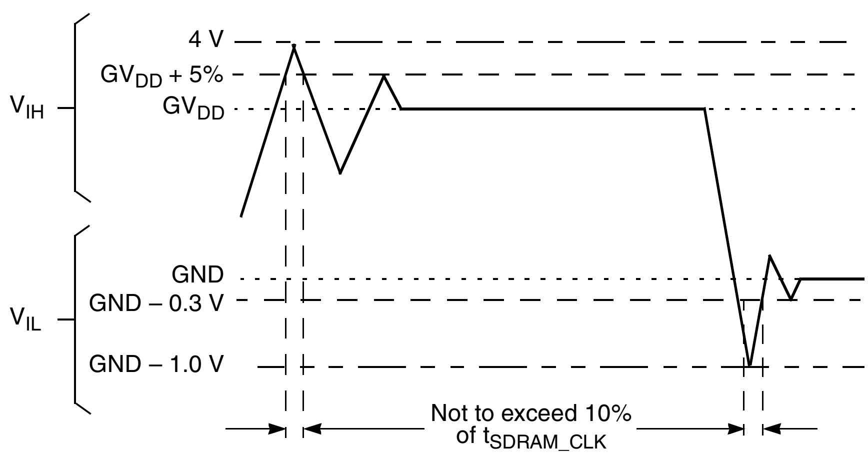


Figure 2. Overshoot/Undershoot Voltage

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA $\overline{\text{CS}}$[0-9] $\overline{\text{CS}}$(10)/$\overline{\text{BCTL1}}$ $\overline{\text{CS}}$(11)/AP(0) BADDR[27–28] ALE $\overline{\text{BCTL0}}$ $\overline{\text{PWE}}$(0:7)/$\overline{\text{PSDDQM}}$(0:7)/$\overline{\text{PBS}}$(0:7) PSDA10/PGPL0 $\overline{\text{PSDWE}}$/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0:3]/LBS[0–3] LSDA10/LGPL0 LSDWE/LGPL1 LOE/LSDRAS/LGPL2 LSDCAS/LGPL3 LGTA/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$ LSDAMUX[3]/LGPL5 $\overline{\text{LWR}}$ MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2) I_{OL} = 3.2mA L_A14 L_A15/$\overline{\text{SMI}}$ L_A16 L_A17/CKSTP_OUT L_A18 L_A19 L_A20 L_A21 L_A22 L_A23 L_A24 L_A25 L_A26 L_A27 L_A28/$\overline{\text{CORE\_SRESET}}$ L_A29 L_A30 L_A31 LCL_D(0-31) LCL_DP(0-3) PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO	V_{OL}	—	0.4	V

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 The leakage current is measured for nominal VDD, VCCSYN, and VDD.

3 Rev C.2 silicon only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics

Characteristics	Symbol	Value	Unit	Air Flow
Thermal resistance for TBGA	θ_{JA}	13.07[1]	°C/W	NC[2]
	θ_{JA}	9.55[1]	°C/W	1 m/s
	θ_{JA}	10.48[3]	°C/W	NC
	θ_{JA}	7.78[3]	°C/W	1 m/s

Note:

1 Assumes a single layer board with no thermal vias
2 Natural convection
3 Assumes a four layer board

2.3 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K/(T_J + 273° C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° C) + \theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8260 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT} (W)[2]				
					Vddl				
					2.4	2.5	2.6	2.7	2.8[3]
33.3	4	4	133.3	133.3	2.04	2.14	2.26	2.38	2.50
50.0	2	3	100	150.0	2.21	2.30	2.45	2.59	2.69
66.7	2	2.5	133.3	166.7	2.47	2.62	2.74	2.88	3.02
66.7	2.5	2.5	166.7	166.7	2.57	2.69	2.83	2.98	3.12
66.7	2	3	133.3	200.0	2.81	2.95	3.12	3.29	3.43
66.7	2.5	3	166.7	200.0	2.88	3.05	3.22	3.38	3.55
50.0	3	4	150	200.0	2.83	3.00	3.14	3.31	3.48

Note:

1 Test temperature = room temperature (25° C)
2 $P_{INT} = I_{DD} \times V_{DD}$ Watts
3 2.8 Vddl does not apply to HiP3 Rev C silicon.

Table 8. AC Characteristics for CPM Inputs[1]

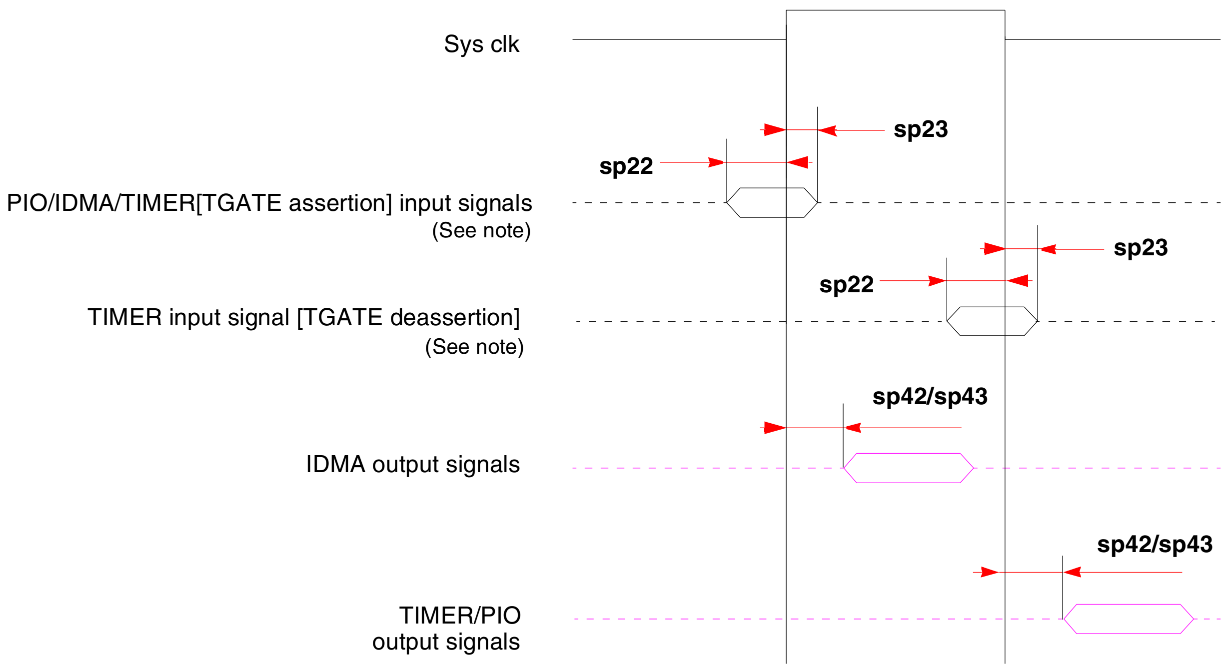
Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	3
sp20	sp21	TDM inputs/SI	15	12
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	5
sp22	sp23	PIO/TIMER/IDMA inputs	10	3

Note:

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 7 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 7. PIO, Timer, and DMA Signal Diagram

Table 9 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp11	sp10	$\overline{AACK}$/$\overline{ARTRY}$/$\overline{TA}$/$\overline{TS}$/$\overline{TEA}$/$\overline{DBG}$/$\overline{BG}$/$\overline{BR}$	6	1
sp12	sp10	Data bus in normal mode	5	1
sp13	sp10	Data bus in ECC and PARITY modes	8	1
sp14	sp10	DP pins	8	1
sp14	sp10	All other pins	5	1

Note:

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Figure 9 shows the interaction of several bus signals.

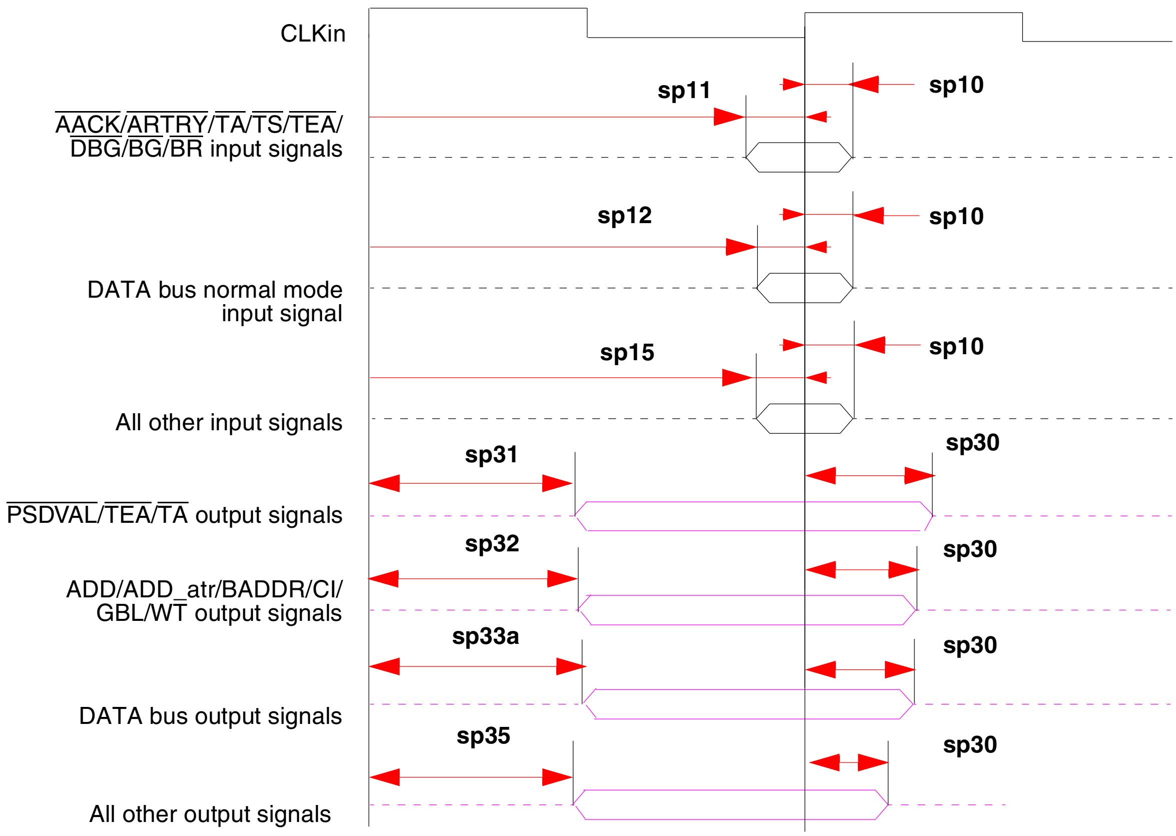


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

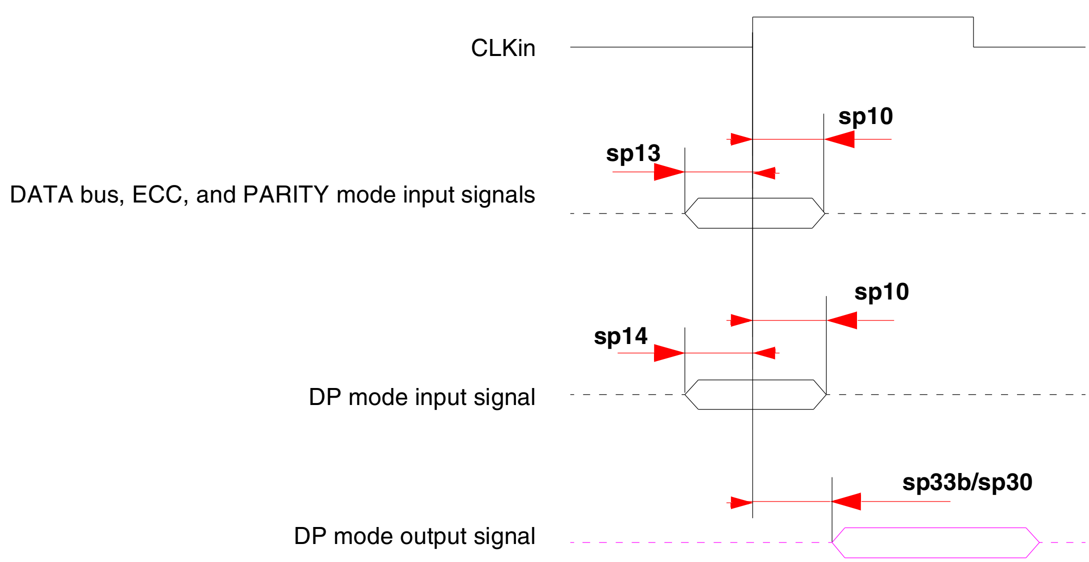


Figure 10. Parity Mode Diagram

[1] Because of speed dependencies, not all of the possible configurations in Table 13 are applicable.
[2] The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU ranges between 133–200 and the CPM ranges between 50–166 MHz.
[3] Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.
[4] 60x and local bus frequency. Identical to CLKIN.
[5] CPM multiplication factor = CPM clock/bus clock
[6] CPU multiplication factor = Core PLL multiplication factor

4 Pinout

This section provides the pin assignments and pinout list for the MPC8260.

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC8260 480 TBGA package as viewed from the top surface.

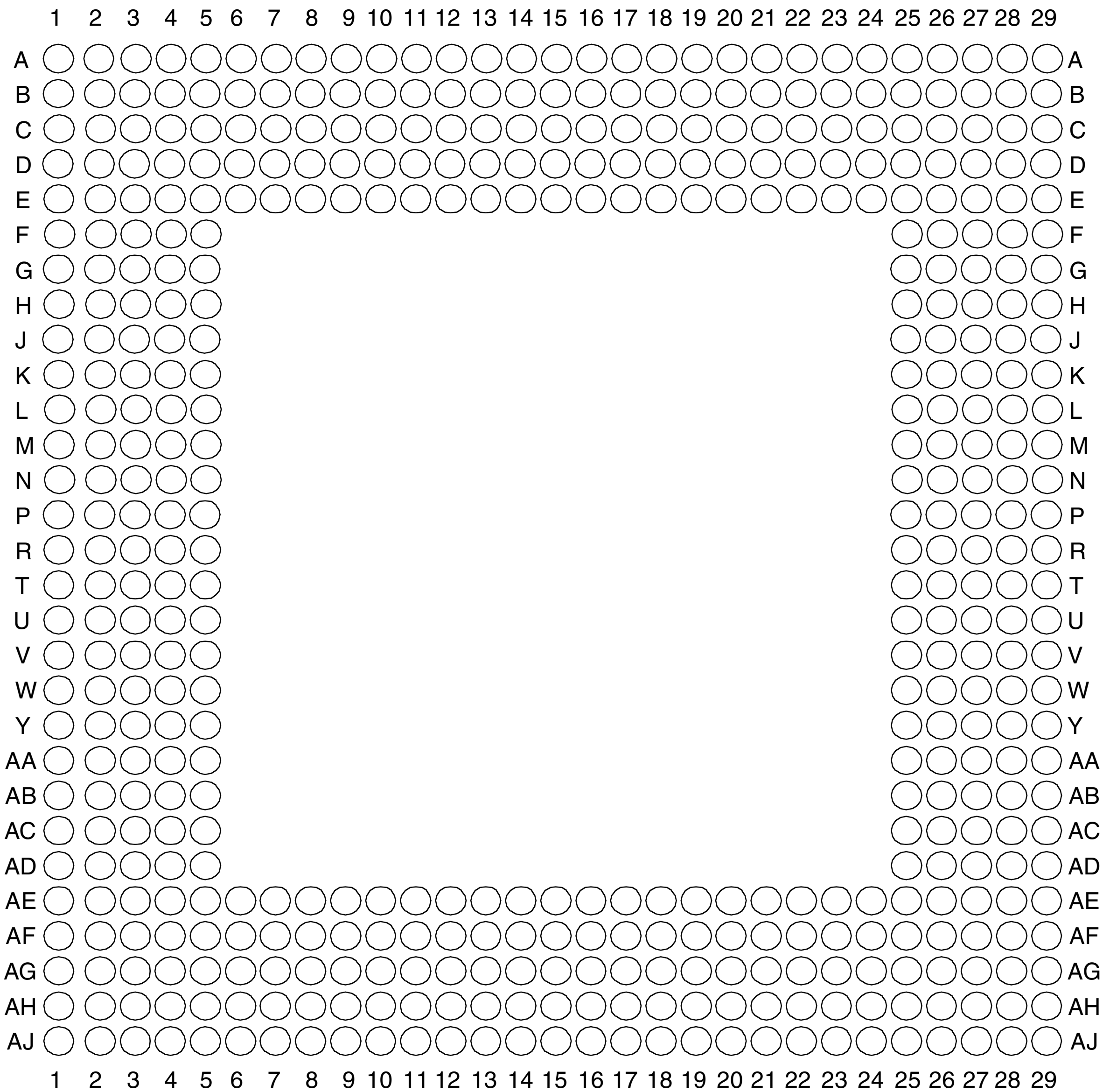


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Table 14. Pinout List (continued)

Pin Name	Ball
WT/BADDR30/IRQ3	U3
L2_HIT/IRQ4	Y4
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22

Table 14. Pinout List (continued)

Pin Name	Ball
LCL_D6	K25
LCL_D7	L29
LCL_D8	L27
LCL_D9	L26
LCL_D10	L25
LCL_D11	M29
LCL_D12	M28
LCL_D13	M27
LCL_D14	M26
LCL_D15	N29
LCL_D16	T25
LCL_D17	U27
LCL_D18	U26
LCL_D19	U25
LCL_D20	V29
LCL_D21	V28
LCL_D22	V27
LCL_D23	V26
LCL_D24	W27
LCL_D25	W26
LCL_D26	W25
LCL_D27	Y29
LCL_D28	Y28
LCL_D29	Y25
LCL_D30	AA29
LCL_D31	AA28
LCL_DP0	L28
LCL_DP1	N28
LCL_DP2	T28
LCL_DP3	W28
$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$	T1
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$	D1
$\overline{\text{TRST}}$	AH3
TCK	AG5
TMS	AJ3

Table 14. Pinout List (continued)

Pin Name	Ball
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12[2]
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11[2]
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9[2]
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8[2]
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7[2]
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7[2]
PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN	AD5[2]
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1[2]
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/FCC1_RTS	AD3[2]
PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL	AB5[2]
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS	AD28[2]
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26[2]
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25[2]
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26[2]
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27[2]
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24[2]
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24[2]
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22[2]
PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21[2]
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19[2]
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18[2]
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17[2]
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14[2]
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13[2]
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12[2]
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11[2]
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2	AH16[2]
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2	AE15[2]
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9[2]
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2	AJ7[2]
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6[2]

Table 14. Pinout List (continued)

Pin Name	Ball
PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1	AE3[2]
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/ FCC2_MII_TX_EN	AE2[2]
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5[2]
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4[2]
PC0/DREQ1/BRGO7/SMSYN2/L1CLKOA2	AB26[2]
PC1/DREQ2/BRGO6/L1RQA2	AD29[2]
PC2/FCC3_CD/FCC2_UT8_TXD3/DONE2	AE29[2]
PC3/FCC3_CTS/FCC2_UT8_TXD2/DACK2/CTS4	AE27[2]
PC4/FCC2_UTM_RXENB/FCC2_UTS_RXENB/SI2_L1ST4/FCC2_CD	AF27[2]
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/FCC2_CTS	AF24[2]
PC6/FCC1_CD/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26[2]
PC7/FCC1_CTS/L1RQC1/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AJ25[2]
PC8/CD4/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/CTS3	AF22[2]
PC9/CTS4/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[2]
PC10/CD3/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20[2]
PC11/CTS3/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19[2]
PC12/CD2/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18[2]
PC13/CTS2/CLSN2/L1RQD1/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18[2]
PC14/CD1/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17[2]
PC15/CTS1/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16[2]
PC16/CLK16/TIN4	AF15[2]
PC17/CLK15/TIN3/BRGO8	AJ15[2]
PC18/CLK14/TGATE2	AH14[2]
PC19/CLK13/BRGO7/SPICLK	AG13[2]
PC20/CLK12/TGATE1	AH12[2]
PC21/CLK11/BRGO6	AJ11[2]
PC22/CLK10/DONE1	AG10[2]
PC23/CLK9/BRGO5/DACK1	AE10[2]
PC24/FCC2_UT8_TXD3/CLK8/TOUT4	AF9[2]
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8[2]
PC26/CLK6/TOUT3/TMCLK	AJ6[2]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[2]
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	AF3[2]

Table 14. Pinout List (continued)

Pin Name	Ball
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	AF2[2]
PC30/FCC2_UT8_TXD3/CLK2/TOUT1	AE1[2]
PC31/CLK1/BRGO1	AD1[2]
PD4/BRGO8/L1TSYNCD1/L1GNTD1/FCC3_RTS/SMRXD2	AC28[2]
PD5/FCC1_UT16_TXD3/DONE1	AD27[2]
PD6/FCC1_UT16_TXD4/DACK1	AF29[2]
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC1_UTM_TXADDR4/FCC1_TXCLAV2	AF28[2]
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25[2]
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26[2]
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27[2]
PD11/L1RQB2/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23[2]
PD12/SI1_L1ST2/L1RXDB1	AG23[2]
PD13/SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20[2]
PD15/FCC1_UT16_RXD1/L1RQC2/I2CSDA	AJ20[2]
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18[2]
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17[2]
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3/ SPICLK/FCC2_UTM_RXADDR3/FCC2_UTS_RXADDR0	AF16[2]
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/FCC1_UTM_TXCLAV3/ SPISEL/BRGO1/FCC2_UTM_TXADDR3/FCC2_UTS_TXADDR0	AH15[2]
PD20/RTS4/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14[2]
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13[2]
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12[2]
PD23/RTS3/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/RTS2/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/RTS1/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4/FCC2_UTS_RXADDR1	AG1[2]
PD30/FCC2_UTM_TXENB/FCC2_UTS_TXENB/TXD1	AD4[2]
PD31/RXD1	AD2[2]
VCCSYN	AB3

Table 15. Symbol Legend (continued)

Symbol	Meaning
UTS	Indicates that a signal is part of the UTOPIA slave interface
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface
MII	Indicates that a signal is part of the media independent interface

5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC8260.

5.1 Package Parameters

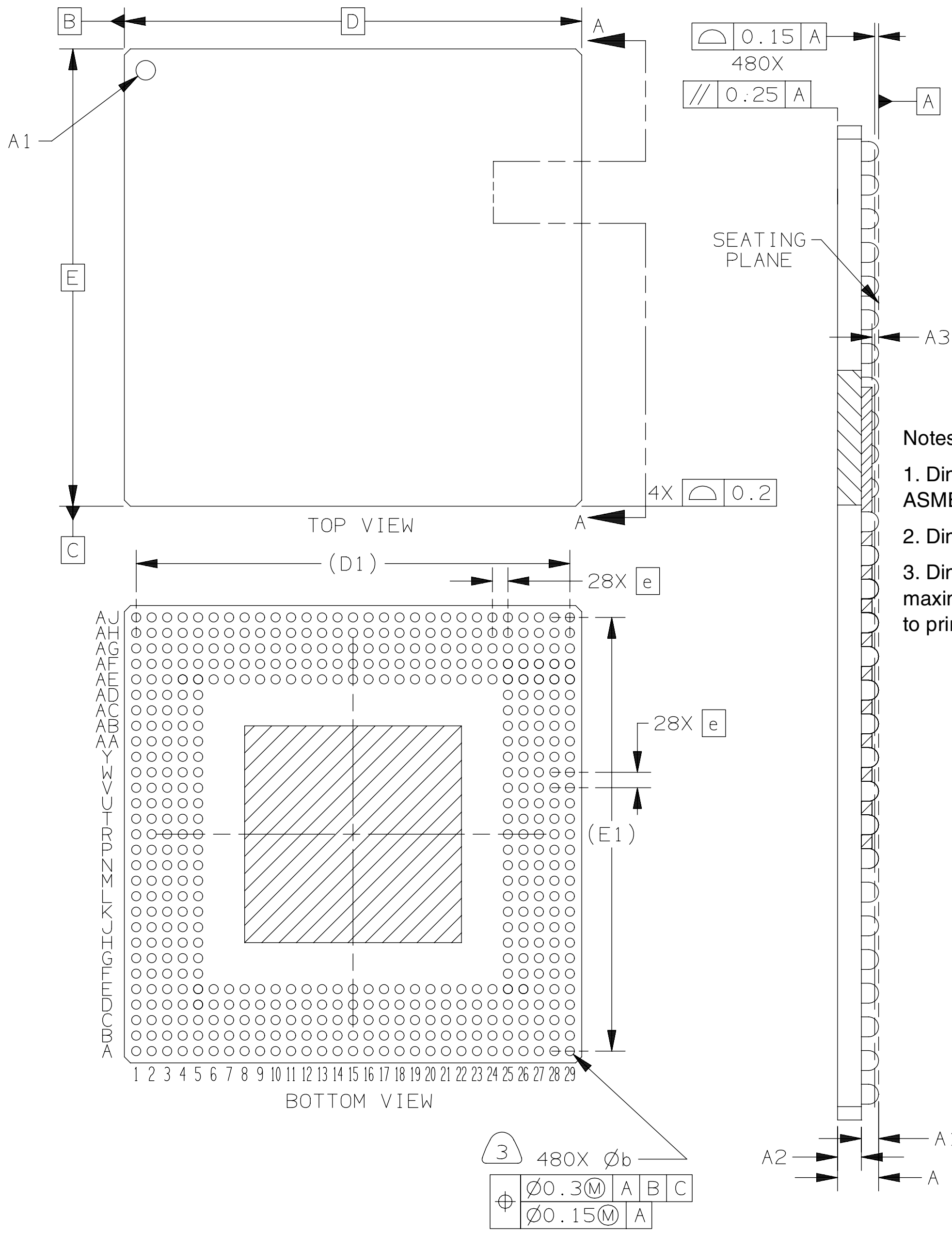
Package parameters are provided in Table 16. The package type is a 37.5 × 37.5 mm, 480-lead TBGA.

Table 16. Package Parameters

Parameter	Value
Package Outline	37.5 x 37.5 mm
Interconnects	480 (29 x 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC8260. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

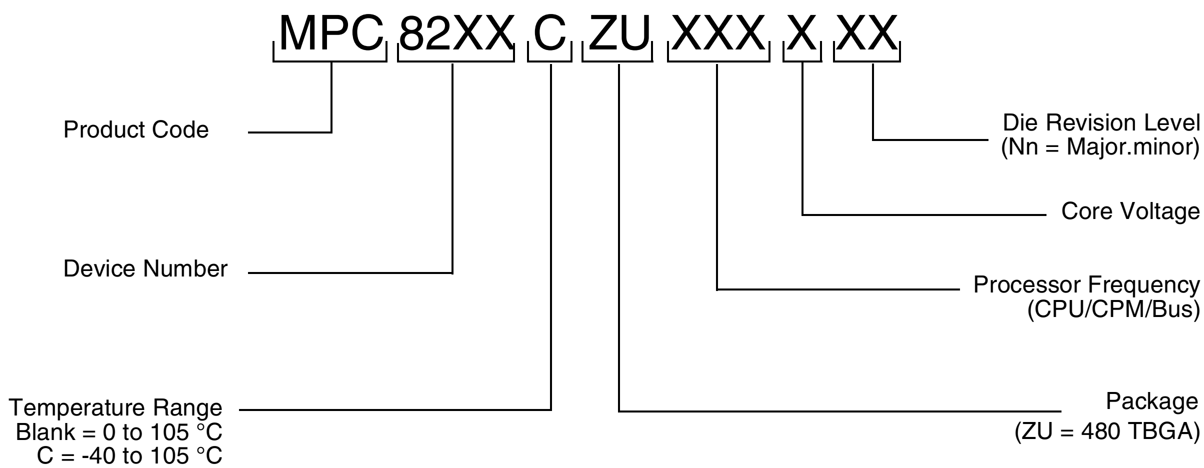


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 17 lists significant changes in each revision of this document.

Table 17. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	05/2010	Added a note about rise/fall time on CPM input pins above Table 8, “AC Characteristics for CPM Inputs.”
1.3	9/2005	• Document template update.
1.2	8/2003	• Note: In revision 0.7, sp30 (Table 10) was changed. This change was not previously recorded in this “Document Revision History” Table. • Addition of MPC8255 description to Section 1, “Features” • Addition of Figure 2 • Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2 • Addition of note 1 to Table 3 • Addition of notes or modifications to Figure 3 through Figure 8 • Addition of reference notes 4, 5, and 6 to Table 13 • Addition of note 2 to Table 14 • Addition of SPICLK to PC19 in Table 14. It is documented correctly in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 14.
1.1	5/2002	• Section 1, “Features”: updated minimum supported core frequency to 133 MHz • Addition of “Note” at bottom of page 5. • Table 13: Note 3.

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