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NXP USA Inc. - KXPC8255ZUIFBC Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kxpc8255zuifbc

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 1 shows the block diagram for the MPC8260.



Figure 1. MPC8260 Block Diagram

1 Features

The major features of the MPC8260 are as follows:

- Dual-issue integer core
 - A core version of the EC603e microprocessor
 - System core microprocessor supporting frequencies of 133–200 MHz (150–200 MHz for the MPC8255)
 - Separate 16-Kbyte data and instruction caches:
 - Four-way set associative
 - Physically addressed
 - LRU replacement algorithm
 - PowerPC architecture-compliant memory management unit (MMU)

Table 2 lists recommended operational voltage conditions.

Rating	Symbol	2.5-V Device ²	Unit
Core supply voltage	VDD	2.4–2.7	V
PLL supply voltage	VCCSYN	2.4–2.7	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (-0.3) – 3.465	V
Junction temperature (maximum)	Тj	105	°C

Table 2. Recommended Operating Conditions¹

¹ **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

² Parts labeled with an "-HVA" suffix are 2.6-V devices.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.



Figure 2. Overshoot/Undershoot Voltage



Table 3 shows DC electrical characteristics.

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V _{IH}	2.0	3.465	V
Input low voltage	V _{IL}	GND	0.8	V
CLKIN input high voltage	V _{IHC}	2.4	3.465	V
CLKIN input low voltage	V _{ILC}	GND	0.4	V
Input leakage current, V _{IN} = VDDH ²	I _{IN}		10	μA
Hi-Z (off state) leakage current, V _{IN} = VDDH ²	Ι _{ΟΖ}	_	10	μA
Signal low input current, V _{IL} = 0.8 V	١L	—	1	μA
Signal high input current, V _{IH} = 2.0 V	Ι _Η	_	1	μA
Output high voltage, $I_{OH} = -2 \text{ mA}$ except XFC, UTOPIA mode, and open drain pins	V _{OH}	2.4		V
In UTOPIA mode: I _{OH} = -8.0mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]				
In UTOPIA mode: I _{OL} = 8.0mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V _{OL}	_	0.5	V

Table 3. DC Electrical Characteristics¹



Characteristic	Symbol	Min	Max	Unit
$\begin{tabular}{lllllllllllllllllllllllllllllllllll$	Symbol V _{OL}	Min —	<u>Мах</u> 0.4	V
CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ				

Table 3. DC Electrical Characteristics¹ (continued)



Characteristic	Symbol	Min	Мах	Unit
I _{OL} = 5.3mA	V _{OL}	—	0.4	V
<u>CS</u> [0-9]				
<u>CS(10)/BCTL1</u>				
CS(11)/AP(0)				
BADDR[27–28]				
ALE				
BCTLO				
PWE(0:7)/PSDDQM(0:7)/PBS(0:7)				
PSDA10/PGPL0				
PSDWE/PGPL1				
L SDW/E/L GPL 1				
LOF/LSDBAS/LGPL2				
LSDCAS/LGPL3				
LGTA/LUPMWAIT/LGPL4/LPBS				
LSDAMUX ³ /LGPL5				
LWR				
MODCK1/AP(1)/TC(0)/BNKSEL(0)				
MODCK2/AP(2)/TC(1)/BNKSEL(1)				
MODCK3/AP(3)/TC(2)/BNKSEL(2)				
I _{OL} = 3.2mA				
L_A14				
L_A15/SMI				
L_/20				
L A22				
L_A23				
L_A24				
L_A25				
L_A26				
L_A28/CORE_SRESET				
LCL D(0-31)				
LCL DP(0-3)				
PA[0-31]				
PB[4-31]				
PC[0-31]				
PD[4–31]				
TDO				

Table 3. DC Electrical Characteristics¹ (continued)

¹ The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

² The leakage current is measured for nominal VDD, VCCSYN, and VDD.



2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8260 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above $P_D = 3W$ (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

			P _{INT} (W) ²						
Bus (MHz)	CPM Multiplier	CPU Multiplier	CPM (MHz)	CPU (MHz)	Vddl				
					2.4	2.5	2.6	2.7	2.8 ³
33.3	4	4	133.3	133.3	2.04	2.14	2.26	2.38	2.50
50.0	2	3	100	150.0	2.21	2.30	2.45	2.59	2.69
66.7	2	2.5	133.3	166.7	2.47	2.62	2.74	2.88	3.02
66.7	2.5	2.5	166.7	166.7	2.57	2.69	2.83	2.98	3.12
66.7	2	3	133.3	200.0	2.81	2.95	3.12	3.29	3.43
66.7	2.5	3	166.7	200.0	2.88	3.05	3.22	3.38	3.55
50.0	3	4	150	200.0	2.83	3.00	3.14	3.31	3.48

Table 5. Estimated Power Dissipation for Various Configurations¹

Note:

¹ Test temperature = room temperature (25° C)

² $P_{INT} = I_{DD} \times V_{DD}$ Watts

³ 2.8 Vddl does not apply to HiP3 Rev C silicon.



2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8260 device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in Table 6.

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46

Table 6.	Output	Buffer	Impedances ¹
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Note:

¹ These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7.	AC	Characteristics	for	СРМ	Outputs ¹
		•		•••••	

Spec Number		Characteristic	Max Delay (ns)	Min Delay (ns)
Max	Min	Characteristic	66 MHz	66 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	2
sp40	sp41	TDM outputs/SI	25	5
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	1
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	2
sp42	sp43	PIO/TIMER/IDMA outputs	14	1

Note:

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.



Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	3
sp20	sp21	TDM inputs/SI	15	12
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	5
sp22	sp23	PIO/TIMER/IDMA inputs	10	3

Table 8. AC Characteristics for CPM Inputs¹

Note:

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.



Figure 3 shows the FCC external clock.



Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.



Figure 4. FCC Internal Clock Diagram



Figure 5 shows the SCC/SMC/SPI/I²C external clock.



Note: There are four possible timing conditions for SCC and SPI:

- 1. Input sampled on the rising edge and output driven on the rising edge (shown).
- 2. Input sampled on the rising edge and output driven on the falling edge.
- 3. Input sampled on the falling edge and output driven on the falling edge.
- 4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I²C External Clock Diagram

Figure 6 shows the SCC/SMC/SPI/I²C internal clock.



Note: There are four possible timing conditions for SCC and SPI:

- 1. Input sampled on the rising edge and output driven on the rising edge (shown).
- 2. Input sampled on the rising edge and output driven on the falling edge.
- 3. Input sampled on the falling edge and output driven on the falling edge.
- 4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram



Figure 9 shows the interaction of several bus signals.



Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).





MODCK_H-MODCK[1-3]	Input Clock Frequency ^{2,3,4}	CPM Multiplication Factor ^{2, 5}	CPM Frequency ²	Core Multiplication Factor ^{2, 6}	Core Frequency ²
			·		
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
	•		4		•
0010_010	33 MHz	4	133 MHz	4	133 MHz
0010_011	33 MHz	4	133 MHz	5	166 MHz
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
	I.		4		ļ
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
	ł		4		ł
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001			Reserved		
0100_010					
0100_011	1				
0100_100	1				
0100_101	1				
0100_110	1				

Table 13. Clock Configuration Modes¹ (continued)



- ¹ Because of speed dependencies, not all of the possible configurations in Table 13 are applicable.
- ² The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU ranges between 133–200 and the CPM ranges between 50–166 MHz.
- ³ Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.
- ⁴ 60x and local bus frequency. Identical to CLKIN.
- ⁵ CPM multiplication factor = CPM clock/bus clock
- ⁶ CPU multiplication factor = Core PLL multiplication factor

4 Pinout

This section provides the pin assignments and pinout list for the MPC8260.



Pinout

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC8260 480 TBGA package as viewed from the top surface.



Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface



Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.



Table 14 shows the pinout list of the MPC8260. Table 15 defines conventions and acronyms used in Table 14.

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	К4
A10	КЗ
A11	К2
A12	К1
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1

Table	14.	Pinout	List
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Table 14. Pinout List (continued)

Pin Name	Ball
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17



Table 14. Pinout List (continued)

Pin Name	Ball
WT/BADDR30/IRQ3	U3
L2_HIT/IRQ4	Y4
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CSO	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTLO	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22



Table 14. Pinout List (continued)

Pin Name	Ball
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	AF2 ²
PC30/FCC2_UT8_TXD3/CLK2/TOUT1	AE1 ²
PC31/CLK1/BRGO1	AD1 ²
PD4/BRGO8/L1TSYNCD1/L1GNTD1/FCC3_RTS/SMRXD2	AC28 ²
PD5/FCC1_UT16_TXD3/DONE1	AD27 ²
PD6/FCC1_UT16_TXD4/DACK1	AF29 ²
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC1_UTM_TXADDR4/FCC1_TXCLAV2	AF28 ²
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25 ²
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26 ²
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27 ²
PD11/L1RQB2/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23 ²
PD12/SI1_L1ST2/L1RXDB1	AG23 ²
PD13/SI1_L1ST1/L1TXDB1	AJ22 ²
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20 ²
PD15/FCC1_UT16_RXD1/L1RQC2/I2CSDA	AJ20 ²
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18 ²
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17 ²
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3/ SPICLK/FCC2_UTM_RXADDR3/FCC2_UTS_RXADDR0	AF16 ²
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/FCC1_UTM_TXCLAV3/ SPISEL/BRG01/FCC2_UTM_TXADDR3/FCC2_UTS_TXADDR0	AH15 ²
PD20/RTS4/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14 ²
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13 ²
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12 ²
PD23/RTS3/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12 ²
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10 ²
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9 ²
PD26/RTS2/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8 ²
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7 ²
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4 ²
PD29/RTS1/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4/FCC2_UTS_RXADDR1	AG1 ²
PD30/FCC2_UTM_TXENB/FCC2_UTS_TXENB/TXD1	AD4 ²
PD31/RXD1	AD2 ²
VCCSYN	AB3



Pinout

Table 14. Pinout List (continued)

Pin Name	Ball
VCCSYN1	В9
GNDSYN	AB1
SPARE1 ³	AE11
SPARE4 ³	U5
SPARE5 ⁴	AF25
SPARE6 ³	V4
THERMAL0 ⁵	AA1
THERMAL1 ⁵	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

Note:

¹ Only on Rev C.2 silicon.

² The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

³ Must be pulled down or left floating.

⁴ Must be pulled down or left floating. However, if compatibility with HiP4 silicon is required, this pin must be pulled up or left floating.

⁵ For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

Symbols used in Table 14 are described in Table 15.

Table 15. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as \overline{TA} , are active low
UTM	Indicates that a signal is part of the UTOPIA master interface



Package Description

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature