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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kxpc8260vvihbc

  - Common on-chip processor (COP) test interface
  - High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)
  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE Std 1149.1™ JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)

— Up to eight TDM interfaces (4 on the MPC8255)
  – Supports two groups of four TDM channels for a total of eight TDMs
  – 2,048 bytes of SI RAM
  – Bit or byte resolution
  – Independent transmit and receive routing, frame synchronization
  – Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
— Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
— Four independent 16-bit timers that can be interconnected as two 32-bit timers

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8260.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8260. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	-0.3 – 2.75	V
PLL supply voltage[2]	VCCSYN	-0.3 – 2.75	V
I/O supply voltage[3]	VDDH	-0.3 – 4.0	V
Input voltage[4]	VIN	GND(-0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(-55) – (+150)	°C

Note:

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.
3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.0 V during normal operation.
4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions[1]

Rating	Symbol	2.5-V Device[2]	Unit
Core supply voltage	VDD	2.4–2.7	V
PLL supply voltage	VCCSYN	2.4–2.7	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (-0.3) – 3.465	V
Junction temperature (maximum)	T_j	105	°C

1 **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

2 Parts labeled with an "-HVA" suffix are 2.6-V devices.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

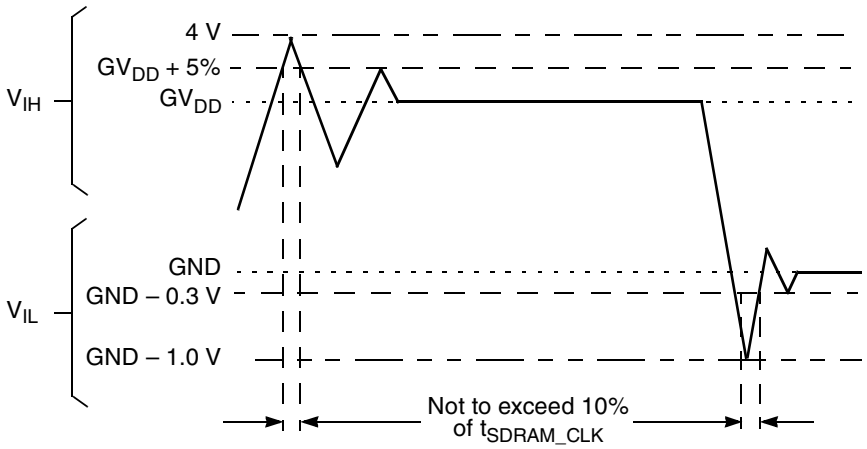


Figure 2. Overshoot/Undershoot Voltage

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8260 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT} (W)[2]				
					Vddl				
					2.4	2.5	2.6	2.7	2.8[3]
33.3	4	4	133.3	133.3	2.04	2.14	2.26	2.38	2.50
50.0	2	3	100	150.0	2.21	2.30	2.45	2.59	2.69
66.7	2	2.5	133.3	166.7	2.47	2.62	2.74	2.88	3.02
66.7	2.5	2.5	166.7	166.7	2.57	2.69	2.83	2.98	3.12
66.7	2	3	133.3	200.0	2.81	2.95	3.12	3.29	3.43
66.7	2.5	3	166.7	200.0	2.88	3.05	3.22	3.38	3.55
50.0	3	4	150	200.0	2.83	3.00	3.14	3.31	3.48

Note:

1 Test temperature = room temperature (25° C)
2 $P_{INT} = I_{DD} \times V_{DD}$ Watts
3 2.8 Vddl does not apply to HiP3 Rev C silicon.

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8260 device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46

Note:

1 These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs[1]

Spec Number		Characteristic	Max Delay (ns)	Min Delay (ns)
Max	Min		66 MHz	66 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	2
sp40	sp41	TDM outputs/SI	25	5
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	1
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	2
sp42	sp43	PIO/TIMER/IDMA outputs	14	1

Note:

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 8. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	3
sp20	sp21	TDM inputs/SI	15	12
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	5
sp22	sp23	PIO/TIMER/IDMA inputs	10	3

Note:

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

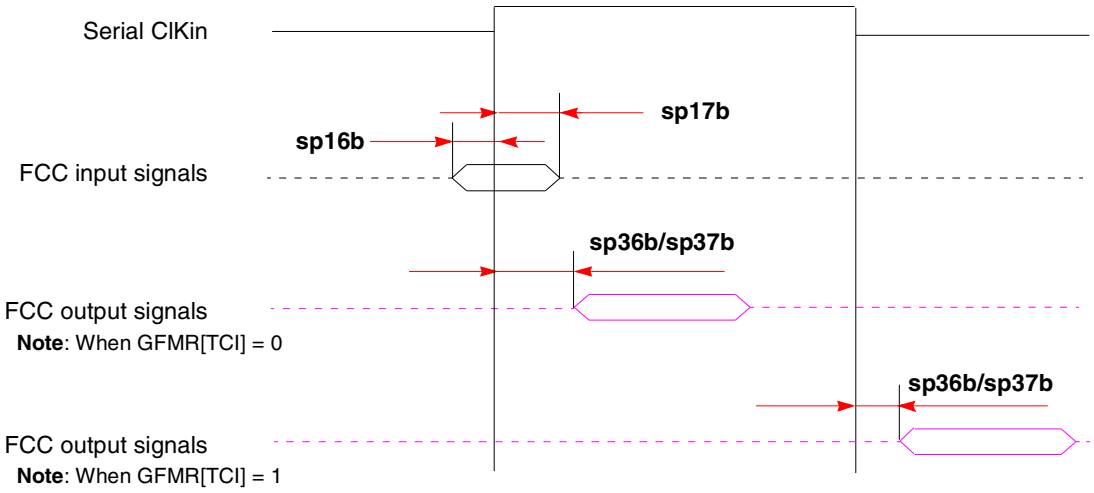


Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.

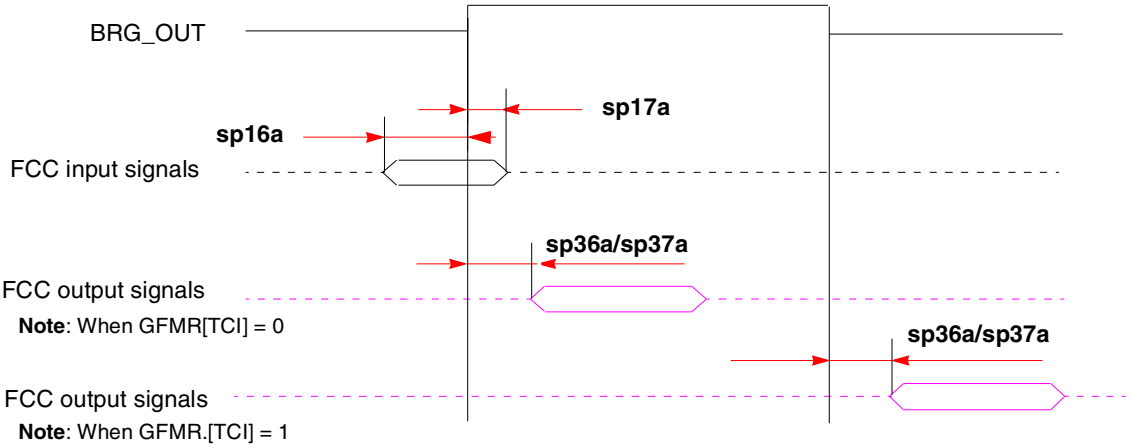
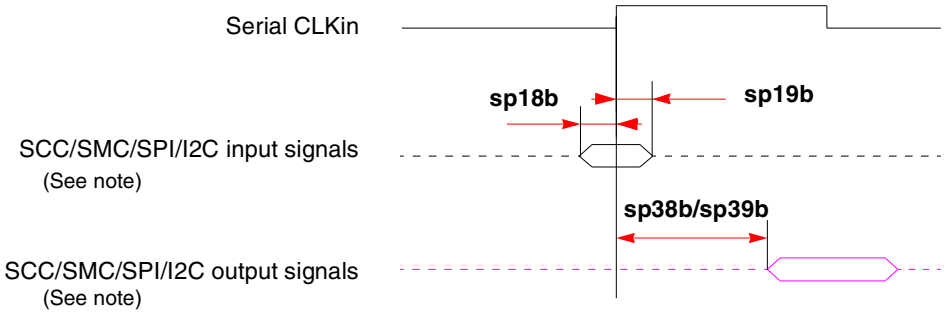


Figure 4. FCC Internal Clock Diagram

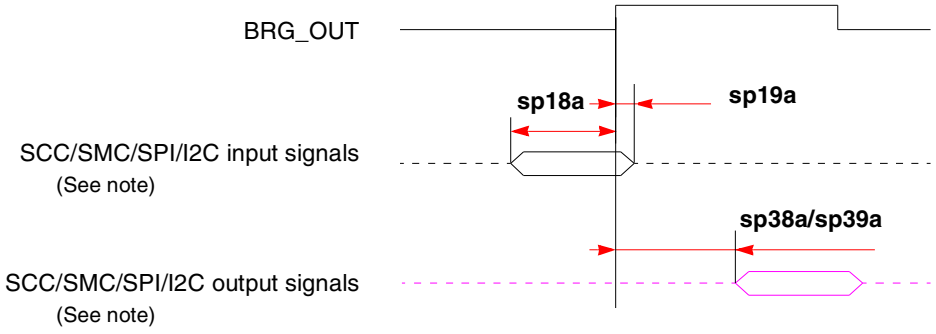
Figure 5 shows the SCC/SMC/SPI/I^{2}C external clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^{2}C External Clock Diagram

Figure 6 shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Max Delay (ns)	Min Delay (ns)
Max	Min		66 MHz	66 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	10	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	0.5
sp33a	sp30	Data bus	8	0.5
sp33b	sp30	DP	12	0.5
sp34	sp30	memc signals/ALE	6	0.5
sp35	sp30	all other signals	7.5	0.5

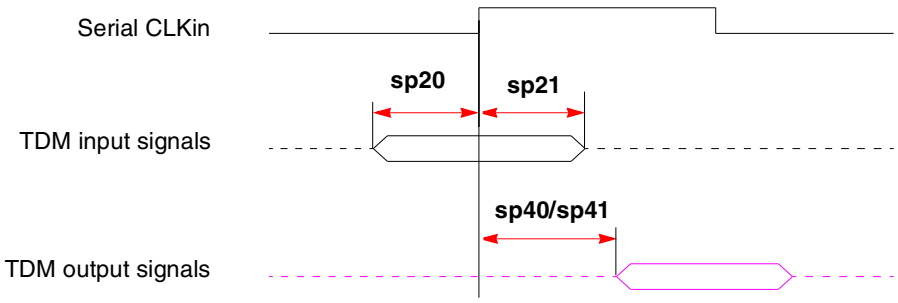
Note:

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 8 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 8. TDM Signal Diagram

Table 13. Clock Configuration Modes[1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3,4]	CPM Multiplication Factor[2, 5]	CPM Frequency[2]	Core Multiplication Factor[2, 6]	Core Frequency[2]
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

Note:

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC8260 480 TBGA package as viewed from the top surface.

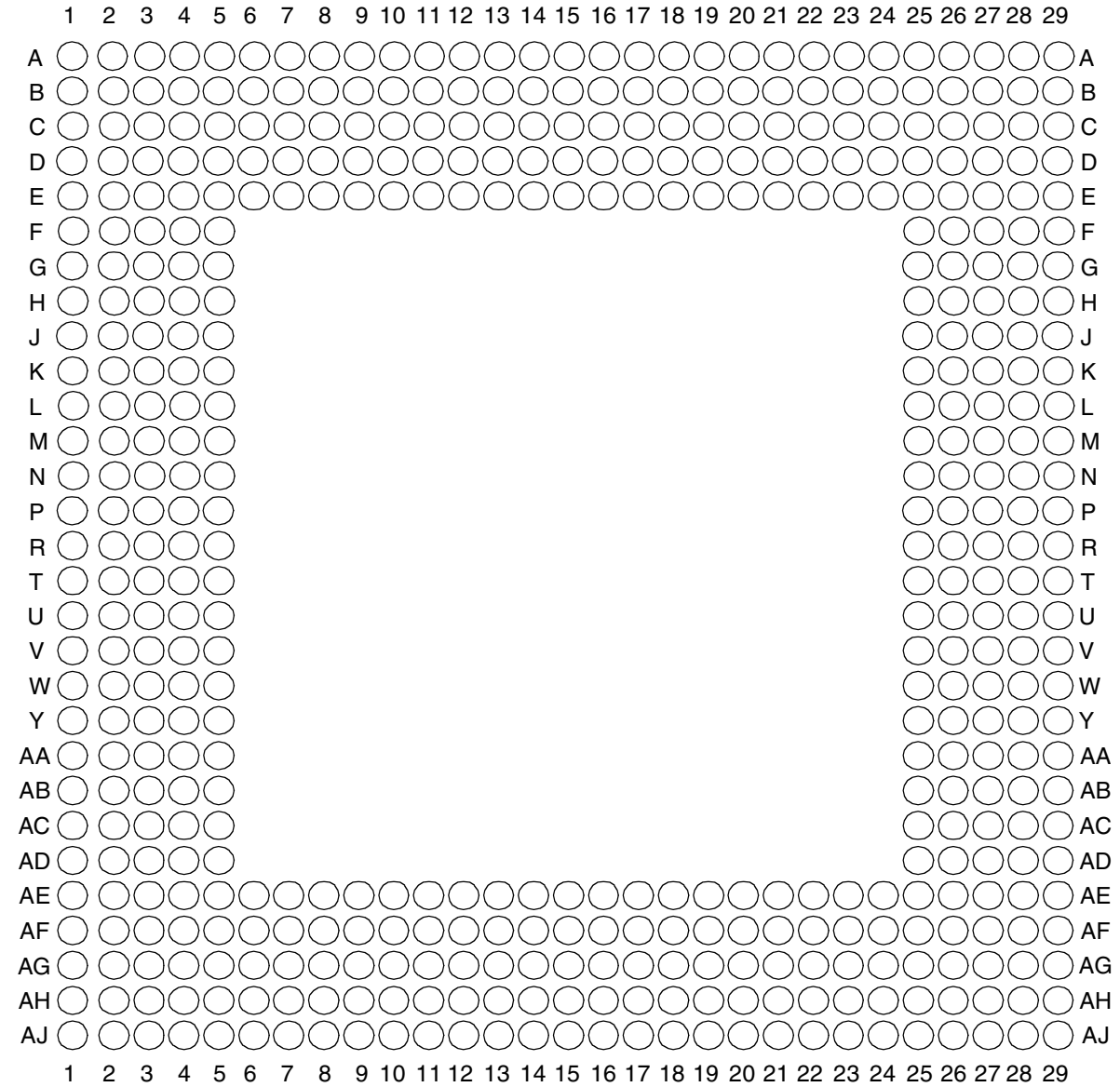


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Table 14. Pinout List (continued)

Pin Name	Ball
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
$\overline{\text{TBST}}$	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
$\overline{\text{AACK}}$	F3
$\overline{\text{ARTRY}}$	E1
$\overline{\text{DBG}}$	V1
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6

Table 14. Pinout List (continued)

Pin Name	Ball
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17

Table 14. Pinout List (continued)

Pin Name	Ball
WT/BADDR30/IRQ3	U3
L2_HIT/IRQ4	Y4
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22

Table 14. Pinout List (continued)

Pin Name	Ball
LWE0/LSDDQM0/LBS0	H28
LWE1/LSDDQM1/LBS1	H27
LWE2/LSDDQM2/LBS2	H26
LWE3/LSDDQM3/LBS3	G29
LSDA10/LGPL0	D27
LSDWE/LGPL1	C28
LOE/LSDRAS/LGPL2	E26
LSDCAS/LGPL3	D25
LGTA/LUPMWAIT/LGPL4/LPBS	C26
LGPL5/LSDAMUX[1]	B27
LWR	D28
L_A14	N27
L_A15/SMI	T29
L_A16	R27
L_A17/CKSTP_OUT	R26
L_A18	R29
L_A19	R28
L_A20	W29
L_A21	P28
L_A22	N26
L_A23	AA27
L_A24	P29
L_A25	AA26
L_A26	N25
L_A27	AA25
L_A28/CORE_SRESET	AB29
L_A29	AB28
L_A30	P25
L_A31	AB27
LCL_D0	H29
LCL_D1	J29
LCL_D2	J28
LCL_D3	J27
LCL_D4	J26
LCL_D5	J25

Table 14. Pinout List (continued)

Pin Name	Ball
LCL_D6	K25
LCL_D7	L29
LCL_D8	L27
LCL_D9	L26
LCL_D10	L25
LCL_D11	M29
LCL_D12	M28
LCL_D13	M27
LCL_D14	M26
LCL_D15	N29
LCL_D16	T25
LCL_D17	U27
LCL_D18	U26
LCL_D19	U25
LCL_D20	V29
LCL_D21	V28
LCL_D22	V27
LCL_D23	V26
LCL_D24	W27
LCL_D25	W26
LCL_D26	W25
LCL_D27	Y29
LCL_D28	Y28
LCL_D29	Y25
LCL_D30	AA29
LCL_D31	AA28
LCL_DP0	L28
LCL_DP1	N28
LCL_DP2	T28
LCL_DP3	W28
$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$	T1
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$	D1
$\overline{\text{TRST}}$	AH3
TCK	AG5
TMS	AJ3

Table 14. Pinout List (continued)

Pin Name	Ball
VCCSYN1	B9
GNDSYN	AB1
SPARE1[3]	AE11
SPARE4[3]	U5
SPARE5[4]	AF25
SPARE6[3]	V4
THERMAL0[5]	AA1
THERMAL1[5]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

Note:

1 Only on Rev C.2 silicon.

2 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

3 Must be pulled down or left floating.

4 Must be pulled down or left floating. However, if compatibility with HiP4 silicon is required, this pin must be pulled up or left floating.

5 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

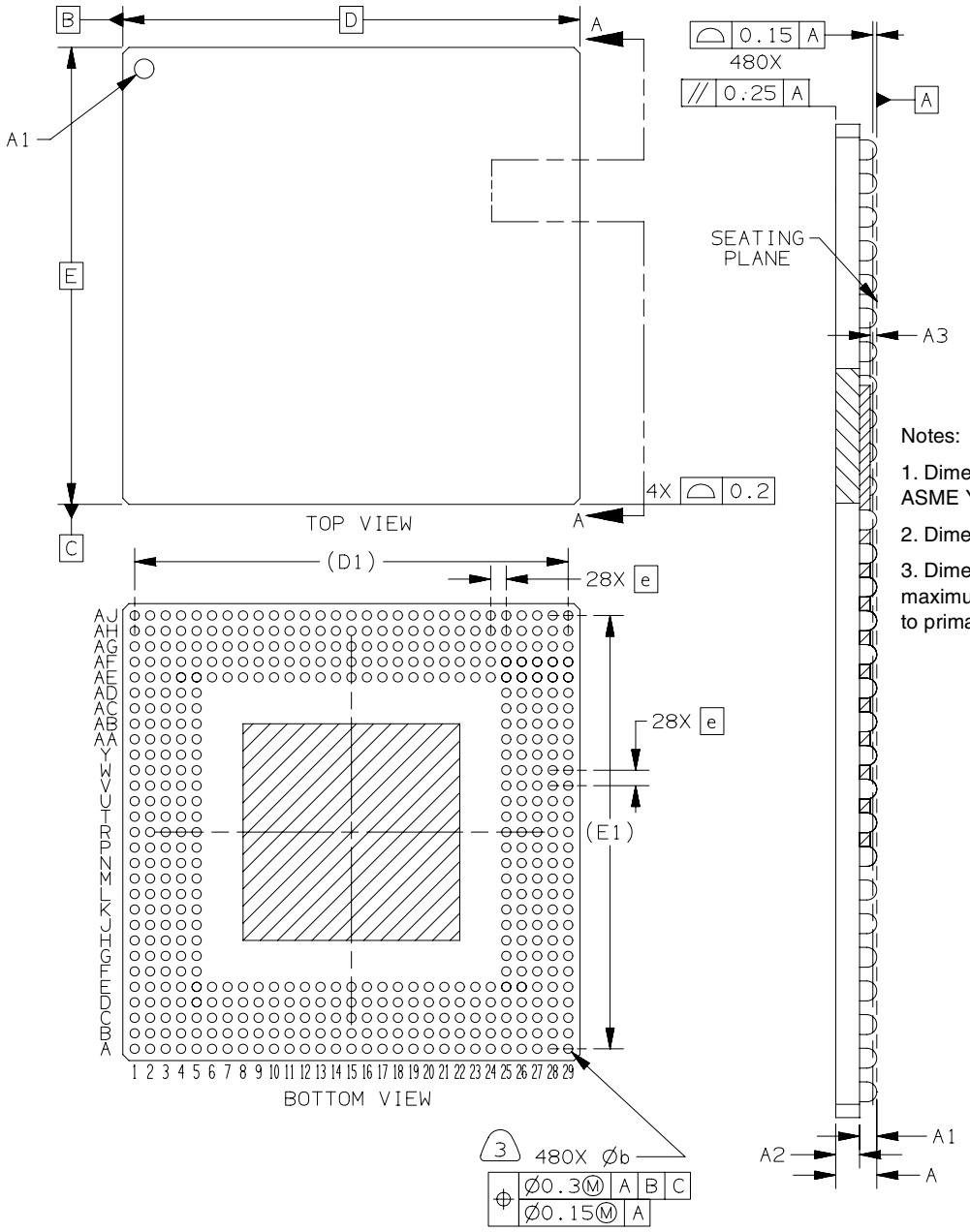
Symbols used in Table 14 are described in Table 15.

Table 15. Symbol Legend

Symbol	Meaning
$\overline{\text{OVERBAR}}$	Signals with overbars, such as $\overline{\text{TA}}$, are active low
UTM	Indicates that a signal is part of the UTOPIA master interface

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC8260. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

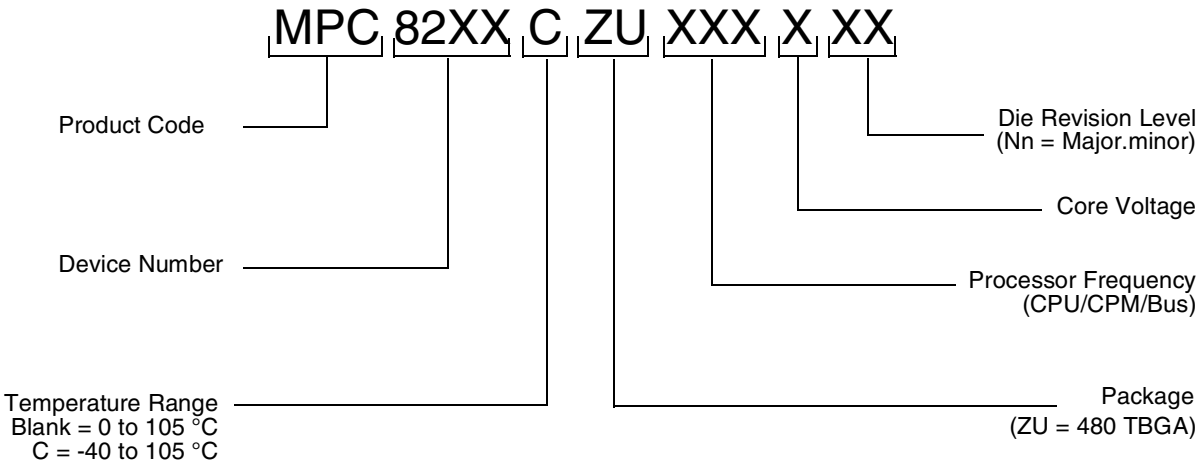


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 17 lists significant changes in each revision of this document.

Table 17. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	05/2010	Added a note about rise/fall time on CPM input pins above Table 8, “AC Characteristics for CPM Inputs.”
1.3	9/2005	• Document template update.
1.2	8/2003	• Note: In revision 0.7, sp30 (Table 10) was changed. This change was not previously recorded in this “Document Revision History” Table. • Addition of MPC8255 description to Section 1, “Features” • Addition of Figure 2 • Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2 • Addition of note 1 to Table 3 • Addition of notes or modifications to Figure 3 through Figure 8 • Addition of reference notes 4, 5, and 6 to Table 13 • Addition of note 2 to Table 14 • Addition of SPICLK to PC19 in Table 14. It is documented correctly in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 14.
1.1	5/2002	• Section 1, “Features”: updated minimum supported core frequency to 133 MHz • Addition of “Note” at bottom of page 5. • Table 13: Note 3.