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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc8260cvvhfbc

Figure 1 shows the block diagram for the MPC8260.

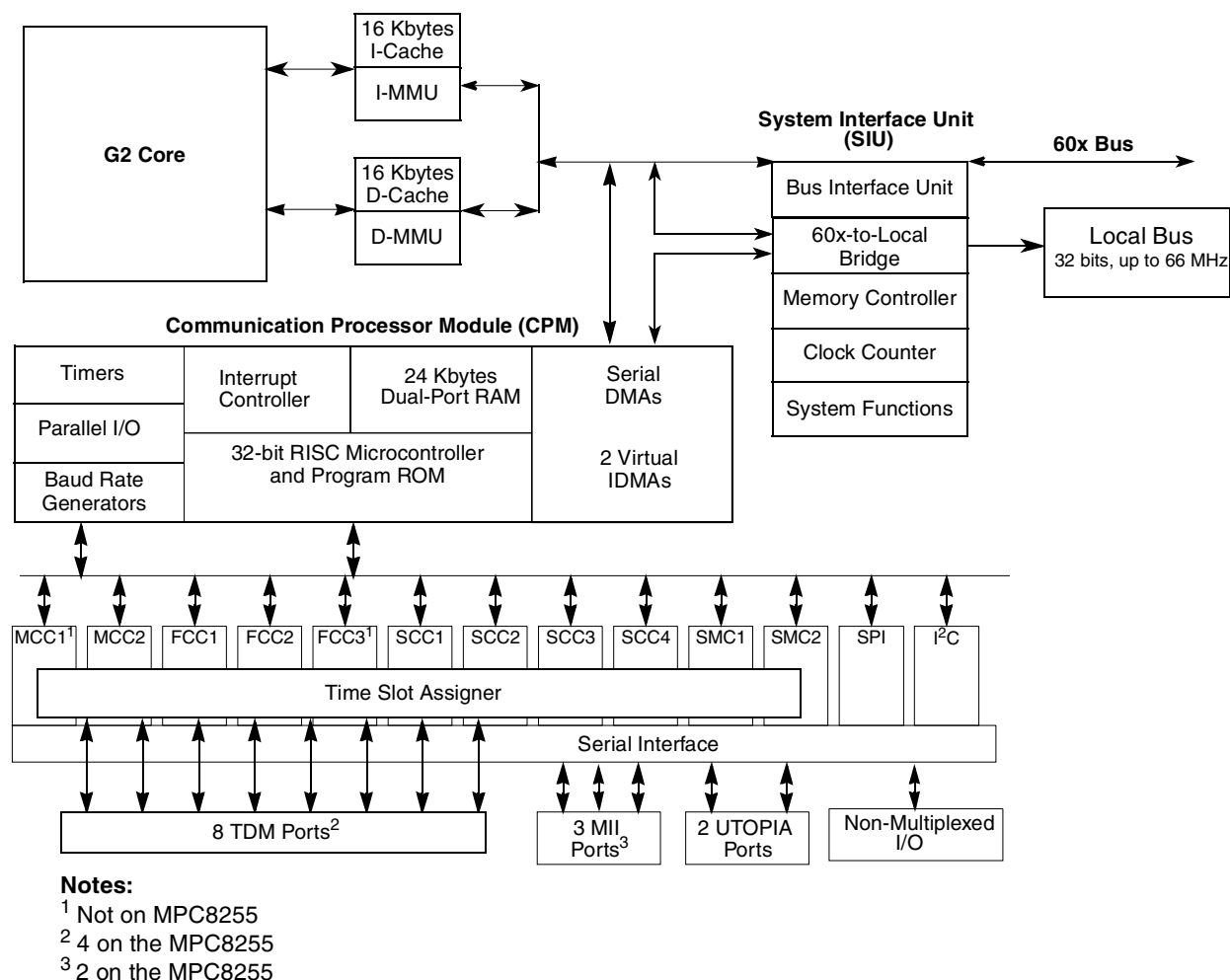


Figure 1. MPC8260 Block Diagram

1 Features

The major features of the MPC8260 are as follows:

- Dual-issue integer core
 - A core version of the EC603e microprocessor
 - System core microprocessor supporting frequencies of 133–200 MHz (150–200 MHz for the MPC8255)
 - Separate 16-Kbyte data and instruction caches:
 - Four-way set associative
 - Physically addressed
 - LRU replacement algorithm
 - PowerPC architecture-compliant memory management unit (MMU)

- Common on-chip processor (COP) test interface
- High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
 - G2 core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
 - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE Std 1149.1™ JTAG test access port
- Twelve-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
 - Byte write enables and selectable parity generation
 - 32-bit address decodes with programmable bank size
 - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
 - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
 - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)

- Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
- Interfaces to G2 core through on-chip 24-Kbyte dual-port RAM and DMA controller
- Serial DMA channels for receive and transmit on all serial channels
- Parallel I/O registers with open-drain and interrupt capability
- Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
- Three fast communications controllers (two on the MPC8255) supporting the following protocols:
 - 10/100-Mbit Ethernet/IEEE Std 802.3™ CDMA/CS interface through media independent interface (MII)
 - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
 - Transparent
 - HDLC—Up to T3 rates (clear channel)
- Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
 - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
- Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
 - Ethernet/IEEE 802.3 CDMA/CS
 - HDLC/SDLC and HDLC bus
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BISYNC) communications
 - Transparent
- Two serial management controllers (SMCs), identical to those of the MPC860
 - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
 - Transparent
 - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I²C) controller (identical to the MPC860 I²C controller)
 - Microwire compatible
 - Multiple-master, single-master, and slave modes

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics¹

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}^2$	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}^2$	I_{OZ}	—	10	μA
Signal low input current, $V_{IL} = 0.8 V$	I_L	—	1	μA
Signal high input current, $V_{IH} = 2.0 V$	I_H	—	1	μA
Output high voltage, $I_{OH} = -2 mA$ except XFC, UTOPIA mode, and open drain pins In UTOPIA mode: $I_{OH} = -8.0mA$ PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	—	V
In UTOPIA mode: $I_{OL} = 8.0mA$ PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	—	0.5	V

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 7.0\text{mA}$ \overline{BR} \overline{BG} $\overline{ABB}/\overline{IRQ2}$ \overline{TS} $A[0-31]$ $TT[0-4]$ \overline{TBST} $TSIZE[0-3]$ \overline{AACK} \overline{ARTRY} \overline{DBG} $\overline{DBB}/\overline{IRQ3}$ $D[0-63]$ $DP(0)/\overline{RSRV}/\overline{EXT_BR2}$ $DP(1)/\overline{IRQ1}/\overline{EXT_BG2}$ $DP(2)/\overline{TLBISYNC}/\overline{IRQ2}/\overline{EXT_DBG2}$ $DP(3)/\overline{IRQ3}/\overline{EXT_BR3}/\overline{CKSTP_OUT}$ $DP(4)/\overline{IRQ4}/\overline{EXT_BG3}/\overline{CORE_SREST}$ $DP(5)/\overline{TBEN}/\overline{IRQ5}/\overline{EXT_DBG3}$ $DP(6)/\overline{CSE(0)}/\overline{IRQ6}$ $DP(7)/\overline{CSE(1)}/\overline{IRQ7}$ \overline{PSDVAL} \overline{TA} \overline{TEA} $\overline{GBL}/\overline{IRQ1}$ $\overline{CI}/\overline{BADDR29}/\overline{IRQ2}$ $\overline{WT}/\overline{BADDR30}/\overline{IRQ3}$ $\overline{L2_HIT}/\overline{IRQ4}$ $\overline{CPU_BG}/\overline{BADDR31}/\overline{IRQ5}$ $\overline{CPU_DBG}$ $\overline{CPU_BR}$ $\overline{IRQ0}/\overline{NMI_OUT}$ $\overline{IRQ7}/\overline{INT_OUT}/\overline{APE}$ $\overline{PORESET}$ \overline{HRESET} \overline{SRESET} $\overline{RSTCONF}$ \overline{QREQ}	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ \overline{ALE} $\overline{BCTL0}$ $\overline{PWE}(0:7)/\overline{PSDDQM}(0:7)/\overline{PBS}(0:7)$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0:3]/\overline{LBS}[0-3]$ $\overline{LSDA10}/\overline{LGPL0}$ $\overline{LSDWE}/\overline{LGPL1}$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}$ $\overline{LSDCAS}/\overline{LGPL3}$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}^3/\overline{LGPL5}$ \overline{LWR} $\overline{MODCK1}/\overline{AP}(1)/\overline{TC}(0)/\overline{BNKSEL}(0)$ $\overline{MODCK2}/\overline{AP}(2)/\overline{TC}(1)/\overline{BNKSEL}(1)$ $\overline{MODCK3}/\overline{AP}(3)/\overline{TC}(2)/\overline{BNKSEL}(2)$ $I_{OL} = 3.2\text{mA}$ $\overline{L_A14}$ $\overline{L_A15}/\overline{SMI}$ $\overline{L_A16}$ $\overline{L_A17}/\overline{CKSTP_OUT}$ $\overline{L_A18}$ $\overline{L_A19}$ $\overline{L_A20}$ $\overline{L_A21}$ $\overline{L_A22}$ $\overline{L_A23}$ $\overline{L_A24}$ $\overline{L_A25}$ $\overline{L_A26}$ $\overline{L_A27}$ $\overline{L_A28}/\overline{CORE_SRESET}$ $\overline{L_A29}$ $\overline{L_A30}$ $\overline{L_A31}$ $\overline{LCL_D}(0-31)$ $\overline{LCL_DP}(0-3)$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ \overline{TDO}	V_{OL}	—	0.4	V

¹ The default configuration of the CPM pins ($\overline{PA}[0-31]$, $\overline{PB}[4-31]$, $\overline{PC}[0-31]$, $\overline{PD}[4-31]$) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

² The leakage current is measured for nominal VDD, VCCSYN, and VDD.

³ Rev C.2 silicon only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics

Characteristics	Symbol	Value	Unit	Air Flow
Thermal resistance for TBGA	θ_{JA}	13.07 ¹	°C/W	NC ²
	θ_{JA}	9.55 ¹	°C/W	1 m/s
	θ_{JA}	10.48 ³	°C/W	NC
	θ_{JA}	7.78 ³	°C/W	1 m/s

Note:

¹ Assumes a single layer board with no thermal vias

² Natural convection

³ Assumes a four layer board

2.3 Power Considerations

The average chip-junction temperature, T_J , in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K / (T_J + 273^\circ \text{C}) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273^\circ \text{C}) + \theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μ F by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8260 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above $P_D = 3W$ (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations¹

Bus (MHz)	CPM Multiplier	CPU Multiplier	CPM (MHz)	CPU (MHz)	$P_{INT} (W)^2$				
					Vddl				
					2.4	2.5	2.6	2.7	2.8 ³
33.3	4	4	133.3	133.3	2.04	2.14	2.26	2.38	2.50
50.0	2	3	100	150.0	2.21	2.30	2.45	2.59	2.69
66.7	2	2.5	133.3	166.7	2.47	2.62	2.74	2.88	3.02
66.7	2.5	2.5	166.7	166.7	2.57	2.69	2.83	2.98	3.12
66.7	2	3	133.3	200.0	2.81	2.95	3.12	3.29	3.43
66.7	2.5	3	166.7	200.0	2.88	3.05	3.22	3.38	3.55
50.0	3	4	150	200.0	2.83	3.00	3.14	3.31	3.48

Note:

¹ Test temperature = room temperature (25° C)

² $P_{INT} = I_{DD} \times V_{DD}$ Watts

³ 2.8 Vddl does not apply to HiP3 Rev C silicon.

Figure 3 shows the FCC external clock.

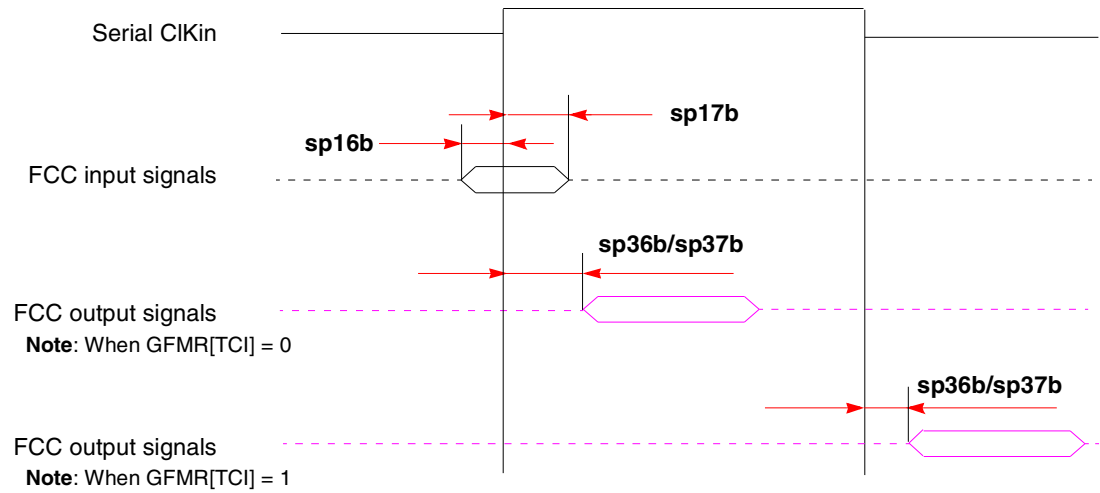


Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.

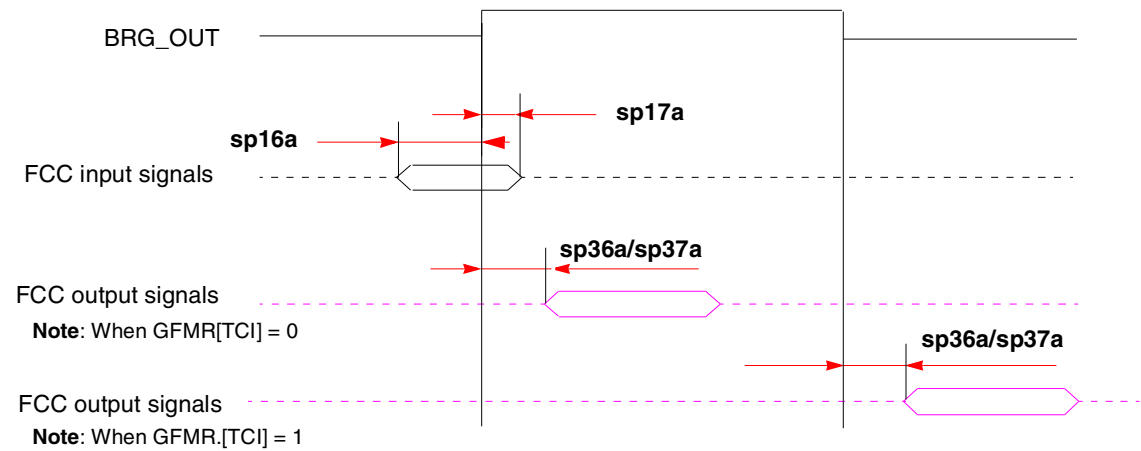


Figure 4. FCC Internal Clock Diagram

Figure 9 shows the interaction of several bus signals.

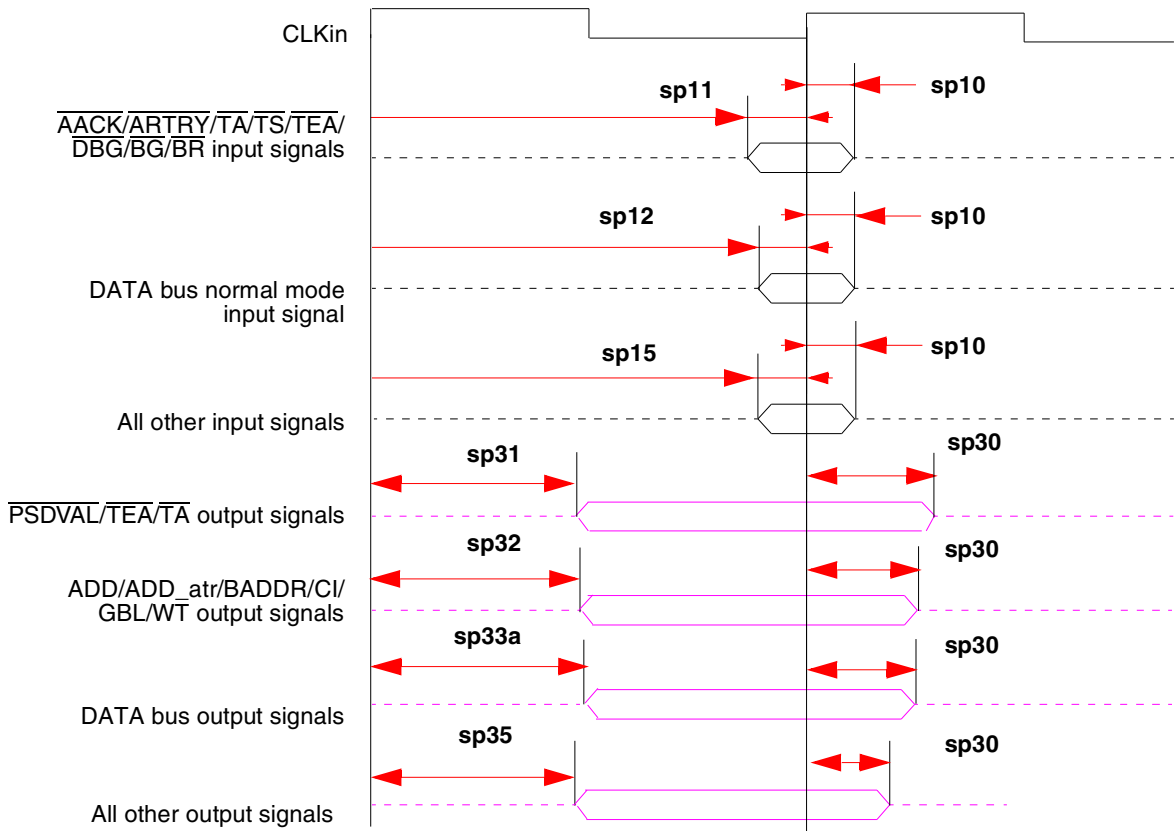


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

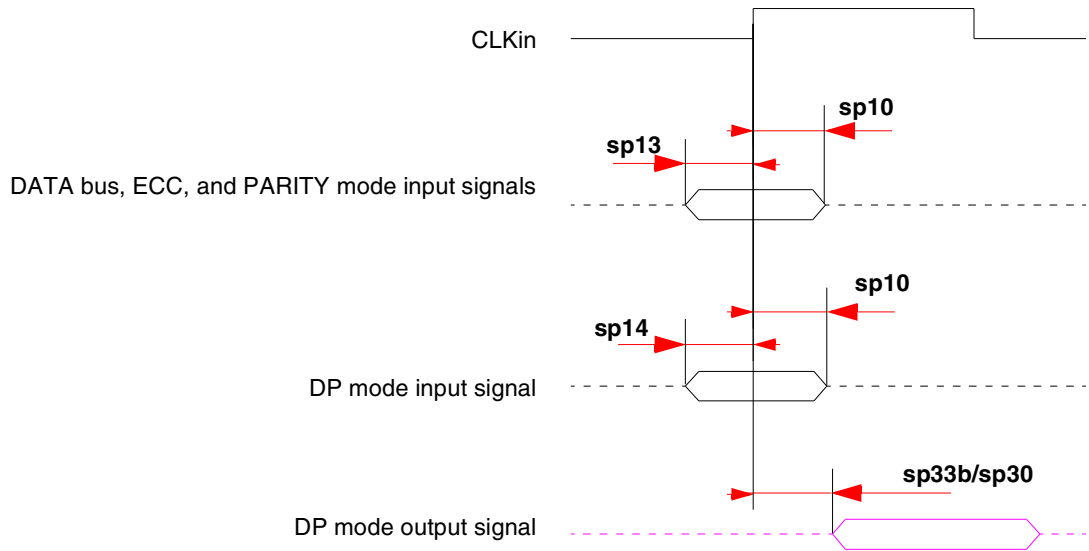


Figure 10. Parity Mode Diagram

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLK_{in}'s rising edge.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 12 shows the eight basic configuration modes. Another 49 modes are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 12 describes default clock modes for the MPC8260.

Table 12. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 13 describes all possible clock configurations when using the hard reset configuration sequence. Note also that basic modes are shown in boldface type.

Table 13. Clock Configuration Modes¹

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3,4}	CPM Multiplication Factor ^{2, 5}	CPM Frequency ²	Core Multiplication Factor ^{2, 6}	Core Frequency ²
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 13. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3,4}	CPM Multiplication Factor ^{2, 5}	CPM Frequency ²	Core Multiplication Factor ^{2, 6}	Core Frequency ²
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	66 MHz	2	133 MHz	2.5	166 MHz
0101_111	66 MHz	2	133 MHz	3	200 MHz
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	66 MHz	2.5	166 MHz	2.5	166 MHz
0110_101	66 MHz	2.5	166 MHz	3	200 MHz
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

Note:

Table 14. Pinout List (continued)

Pin Name	Ball
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
TBST	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
AACK	F3
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6

Table 14. Pinout List (continued)

Pin Name	Ball
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/RSRV/EXT_BR2	B22
IRQ1/DP1/EXT_BG2	A22
IRQ2/DP2/TLBISYNC/EXT_DBG2	E21
IRQ3/DP3/CKSTP_OUT/EXT_BR3	D21
IRQ4/DP4/CORE_SRESET/EXT_BG3	C21
IRQ5/DP5/TBEN/EXT_DBG3	B21
IRQ6/DP6/CSE0	A21
IRQ7/DP7/CSE1	E20
PSDVAL	V3
TA	C22
TEA	V5
GBL/IRQ1	W1
CI/BADDR29/IRQ2	U2

Table 14. Pinout List (continued)

Pin Name	Ball
$\overline{\text{LWE0}}/\text{LSDDQM0}/\text{LBS0}$	H28
$\overline{\text{LWE1}}/\text{LSDDQM1}/\text{LBS1}$	H27
$\overline{\text{LWE2}}/\text{LSDDQM2}/\text{LBS2}$	H26
$\overline{\text{LWE3}}/\text{LSDDQM3}/\text{LBS3}$	G29
$\text{LSDA10}/\text{LGPL0}$	D27
$\overline{\text{LSDWE}}/\text{LGPL1}$	C28
$\overline{\text{LOE}}/\text{LSDRAS}/\text{LGPL2}$	E26
$\overline{\text{LSDCAS}}/\text{LGPL3}$	D25
$\overline{\text{LGTA}}/\text{LUPMWAIT}/\text{LGPL4}/\text{LPBS}$	C26
$\text{LGPL5}/\text{LSDAMUX}^1$	B27
$\overline{\text{LWR}}$	D28
L_A14	N27
L_A15/ $\overline{\text{SMI}}$	T29
L_A16	R27
L_A17/ $\overline{\text{CKSTP_OUT}}$	R26
L_A18	R29
L_A19	R28
L_A20	W29
L_A21	P28
L_A22	N26
L_A23	AA27
L_A24	P29
L_A25	AA26
L_A26	N25
L_A27	AA25
L_A28/ $\overline{\text{CORE_SRESET}}$	AB29
L_A29	AB28
L_A30	P25
L_A31	AB27
LCL_D0	H29
LCL_D1	J29
LCL_D2	J28
LCL_D3	J27
LCL_D4	J26
LCL_D5	J25

Table 14. Pinout List (continued)

Pin Name	Ball
LCL_D6	K25
LCL_D7	L29
LCL_D8	L27
LCL_D9	L26
LCL_D10	L25
LCL_D11	M29
LCL_D12	M28
LCL_D13	M27
LCL_D14	M26
LCL_D15	N29
LCL_D16	T25
LCL_D17	U27
LCL_D18	U26
LCL_D19	U25
LCL_D20	V29
LCL_D21	V28
LCL_D22	V27
LCL_D23	V26
LCL_D24	W27
LCL_D25	W26
LCL_D26	W25
LCL_D27	Y29
LCL_D28	Y28
LCL_D29	Y25
LCL_D30	AA29
LCL_D31	AA28
LCL_DP0	L28
LCL_DP1	N28
LCL_DP2	T28
LCL_DP3	W28
$\overline{\text{IRQ0/NMI_OUT}}$	T1
$\overline{\text{IRQ7/INT_OUT/APE}}$	D1
$\overline{\text{TRST}}$	AH3
TCK	AG5
TMS	AJ3

Table 14. Pinout List (continued)

Pin Name	Ball
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	AF2 ²
PC30/FCC2_UT8_TXD3/CLK2/TOUT1	AE1 ²
PC31/CLK1/BRGO1	AD1 ²
PD4/BRGO8/L1TSYNCD1/L1GN1D1/FCC3_RTS/SMRXD2	AC28 ²
PD5/FCC1_UT16_TXD3/DONE1	AD27 ²
PD6/FCC1_UT16_TXD4/DACK1	AF29 ²
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC1_UTM_TXADDR4/FCC1_TXCLAV2	AF28 ²
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25 ²
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26 ²
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27 ²
PD11/L1RQB2/FCC2_UT8_RXD0/L1TSYNCB1/L1GN1B1	AJ23 ²
PD12/SI1_L1ST2/L1RXDB1	AG23 ²
PD13/SI1_L1ST1/L1TXDB1	AJ22 ²
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20 ²
PD15/FCC1_UT16_RXD1/L1RQC2/I2CSDA	AJ20 ²
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GN1C1/SPIMISO	AG18 ²
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17 ²
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3/ SPICLK/FCC2_UTM_RXADDR3/FCC2_UTS_RXADDR0	AF16 ²
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/FCC1_UTM_TXCLAV3/ SPISEL/BRGO1/FCC2_UTM_TXADDR3/FCC2_UTS_TXADDR0	AH15 ²
PD20/RTS4/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14 ²
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13 ²
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12 ²
PD23/RTS3/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12 ²
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10 ²
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9 ²
PD26/RTS2/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8 ²
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7 ²
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4 ²
PD29/RTS1/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4/FCC2_UTS_RXADDR1	AG1 ²
PD30/FCC2_UTM_TXENB/FCC2_UTS_TXENB/TXD1	AD4 ²
PD31/RXD1	AD2 ²
VCCSYN	AB3

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

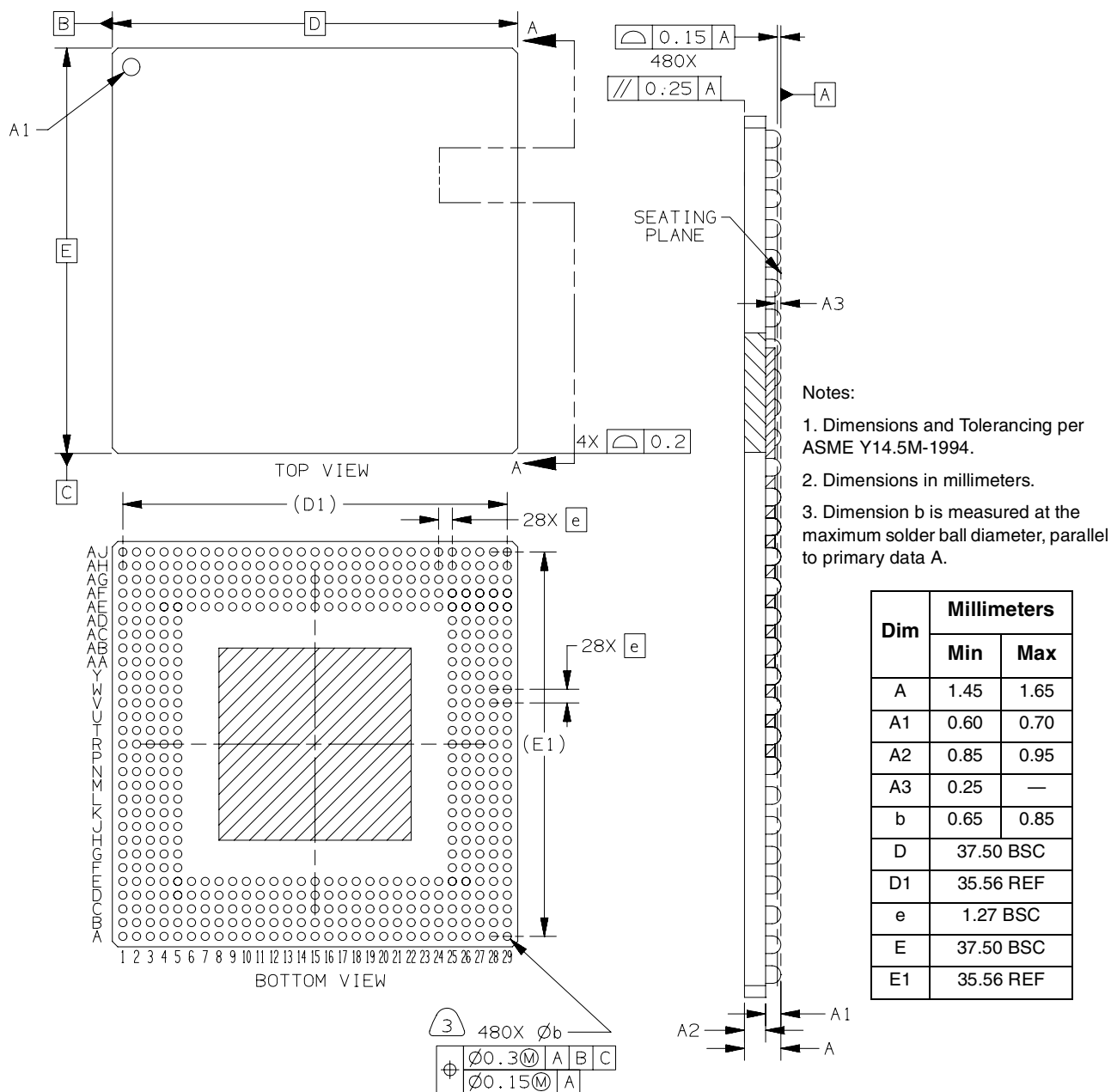


Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature

Table 17. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1.0	3/2002	<ul style="list-style-type: none"> • Table 14: modified notes to pins AE11 and AF25. • Table 14: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.9	2/2002	<ul style="list-style-type: none"> • Table 14: additional note added to AE11
0.8	2/2002	<ul style="list-style-type: none"> • Table 7, Table 8, Table 9, and Table 10: revision 0.7 of this document incorrectly included values for 83 MHz. 83 MHz is not supported on the MPC8260. • Table 14: notes added to pins at AE11, AF25, U5, and V4.
0.7	11/2001	<ul style="list-style-type: none"> • Revision of Table 5, "Power Dissipation" • Modifications to Figure 9, Table 2, Table 10, Table 11 • Additional revisions to text and figures throughout
0.6	5/2001	Corrected the thermal values in Table 3, "Thermal Characteristics."
0.2–0.5	—	Temporary revisions
0.1	1/2000	—
0	—	Initial version

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