Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc8260vvihbc

  - Common on-chip processor (COP) test interface
  - High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)
  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE Std 1149.1™ JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)

— Up to eight TDM interfaces (4 on the MPC8255)
  – Supports two groups of four TDM channels for a total of eight TDMs
  – 2,048 bytes of SI RAM
  – Bit or byte resolution
  – Independent transmit and receive routing, frame synchronization
  – Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
— Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
— Four independent 16-bit timers that can be interconnected as two 32-bit timers

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8260.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8260. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	-0.3 – 2.75	V
PLL supply voltage[2]	VCCSYN	-0.3 – 2.75	V
I/O supply voltage[3]	VDDH	-0.3 – 4.0	V
Input voltage[4]	VIN	GND(-0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(-55) – (+150)	°C

Note:

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.
3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.0 V during normal operation.
4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA $\overline{CS}$[0-9] $\overline{CS}$(10)/$\overline{BCTL1}$ $\overline{CS}$(11)/AP(0) BADDR[27–28] ALE $\overline{BCTL0}$ $\overline{PWE}$(0:7)/$\overline{PSDDQM}$(0:7)/$\overline{PBS}$(0:7) PSDA10/PGPL0 $\overline{PSDWE}$/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0:3]/LBS[0–3] LSDA10/LGPL0 LSDWE/LGPL1 LOE/LSDRAS/LGPL2 LSDCAS/LGPL3 LGTA/LUPMWAIT/LGPL4/$\overline{LPBS}$ LSDAMUX[3]/LGPL5 $\overline{LWR}$ MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14 L_A15/$\overline{SMI}$ L_A16 L_A17/CKSTP_OUT L_A18 L_A19 L_A20 L_A21 L_A22 L_A23 L_A24 L_A25 L_A26 L_A27 L_A28/$\overline{CORE\_SRESET}$ L_A29 L_A30 L_A31 LCL_D(0-31) LCL_DP(0-3) PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 The leakage current is measured for nominal VDD, VCCSYN, and VDD.

Table 8. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	3
sp20	sp21	TDM inputs/SI	15	12
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	5
sp22	sp23	PIO/TIMER/IDMA inputs	10	3

Note:

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 11 shows signal behavior in MEMC mode.

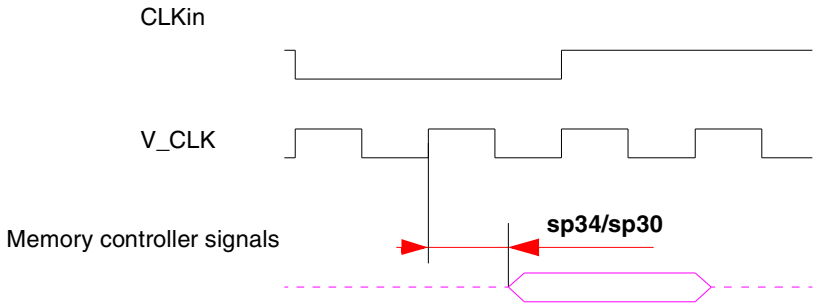


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC8260 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 12 is a graphical representation of Table 11.

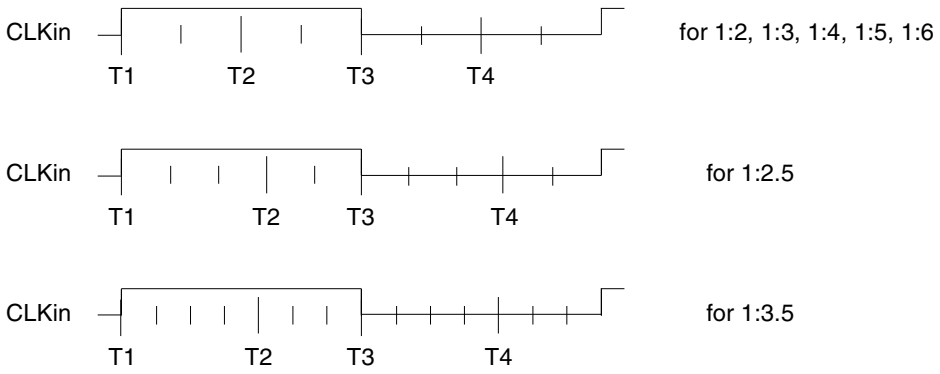


Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 12 shows the eight basic configuration modes. Another 49 modes are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 12 describes default clock modes for the MPC8260.

Table 12. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 13 describes all possible clock configurations when using the hard reset configuration sequence. Note also that basic modes are shown in boldface type.

Table 13. Clock Configuration Modes[1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3,4]	CPM Multiplication Factor[2, 5]	CPM Frequency[2]	Core Multiplication Factor[2, 6]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

1 Because of speed dependencies, not all of the possible configurations in Table 13 are applicable.
2 The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU ranges between 133–200 and the CPM ranges between 50–166 MHz.
3 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.
4 60x and local bus frequency. Identical to CLKIN.
5 CPM multiplication factor = CPM clock/bus clock
6 CPU multiplication factor = Core PLL multiplication factor

4 Pinout

This section provides the pin assignments and pinout list for the MPC8260.

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC8260 480 TBGA package as viewed from the top surface.

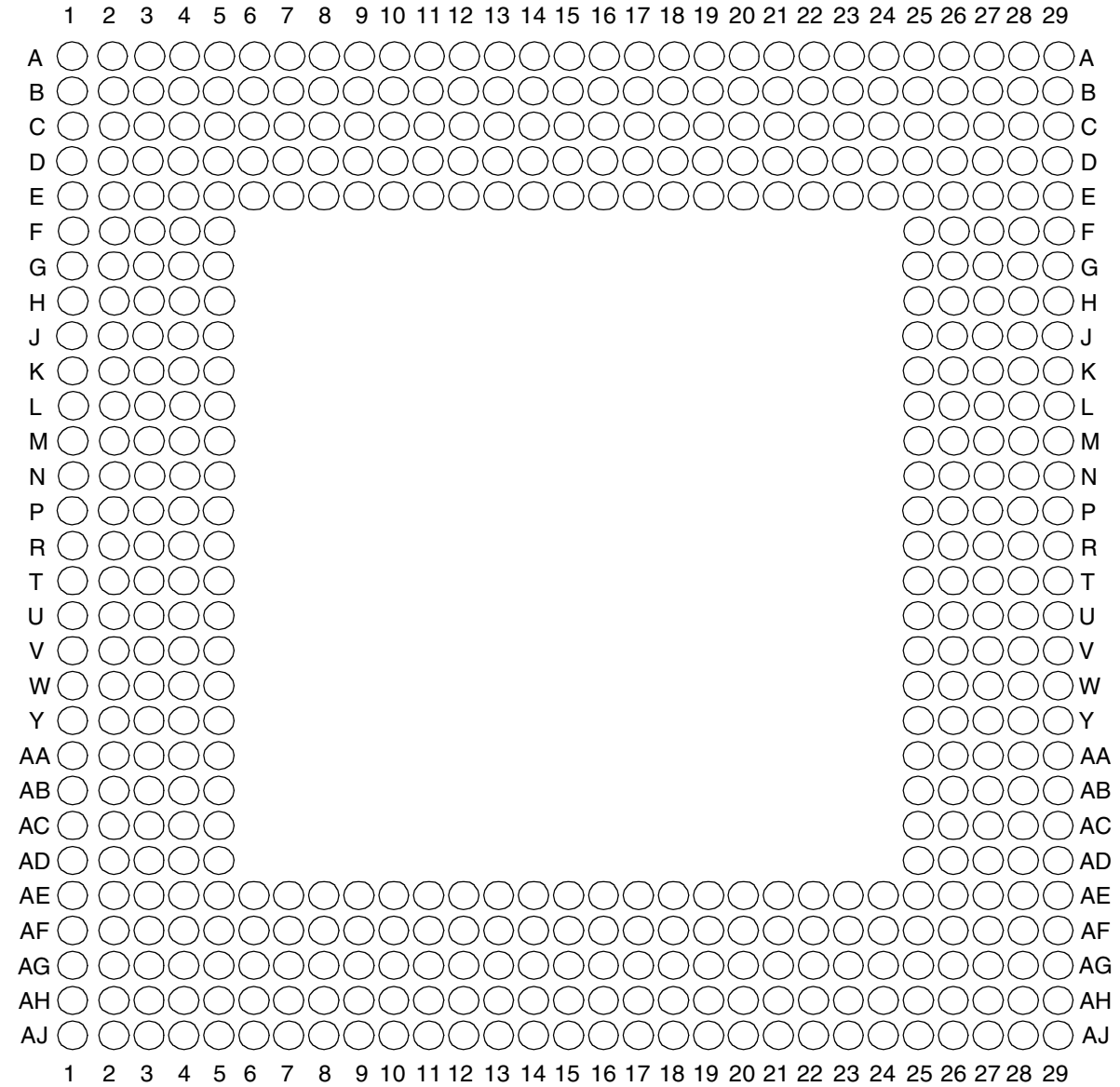


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Table 14. Pinout List (continued)

Pin Name	Ball
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
$\overline{\text{TBST}}$	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
$\overline{\text{AACK}}$	F3
$\overline{\text{ARTRY}}$	E1
$\overline{\text{DBG}}$	V1
$\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6

Table 14. Pinout List (continued)

Pin Name	Ball
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17

Table 14. Pinout List (continued)

Pin Name	Ball
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20
$\overline{\text{PSDVAL}}$	V3
$\overline{\text{TA}}$	C22
$\overline{\text{TEA}}$	V5
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$	W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	U2

Table 14. Pinout List (continued)

Pin Name	Ball
WT/BADDR30/IRQ3	U3
L2_HIT/IRQ4	Y4
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22

Table 14. Pinout List (continued)

Pin Name	Ball
LCL_D6	K25
LCL_D7	L29
LCL_D8	L27
LCL_D9	L26
LCL_D10	L25
LCL_D11	M29
LCL_D12	M28
LCL_D13	M27
LCL_D14	M26
LCL_D15	N29
LCL_D16	T25
LCL_D17	U27
LCL_D18	U26
LCL_D19	U25
LCL_D20	V29
LCL_D21	V28
LCL_D22	V27
LCL_D23	V26
LCL_D24	W27
LCL_D25	W26
LCL_D26	W25
LCL_D27	Y29
LCL_D28	Y28
LCL_D29	Y25
LCL_D30	AA29
LCL_D31	AA28
LCL_DP0	L28
LCL_DP1	N28
LCL_DP2	T28
LCL_DP3	W28
$\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$	T1
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$	D1
$\overline{\text{TRST}}$	AH3
TCK	AG5
TMS	AJ3

Table 14. Pinout List (continued)

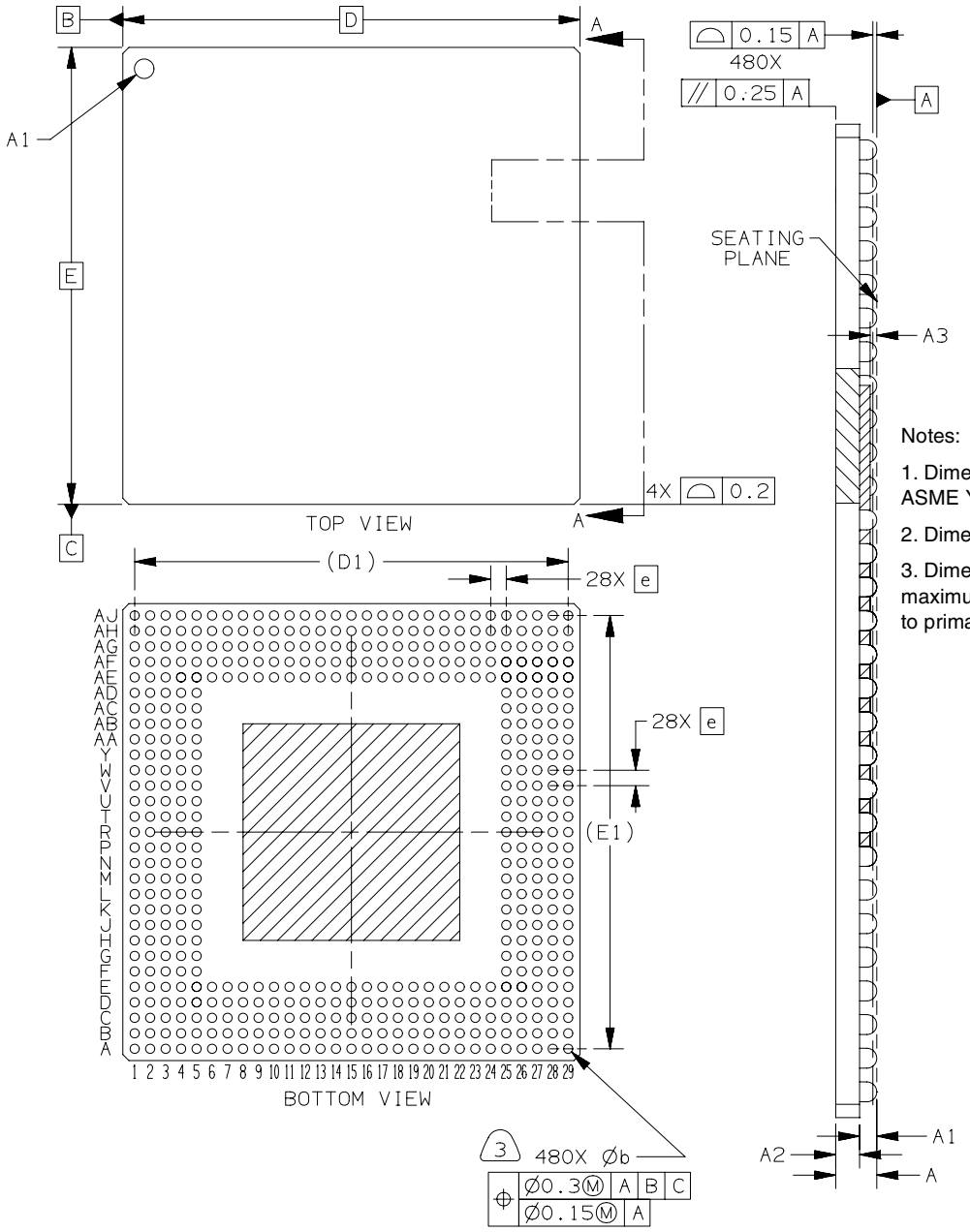
Pin Name	Ball
TDI	AE6
TDO	AF5
$\overline{\text{TRIS}}$	AB4
$\overline{\text{PORESET}}$	AG6
$\overline{\text{HRESET}}$	AH5
$\overline{\text{SRESET}}$	AF6
$\overline{\text{QREQ}}$	AA3
$\overline{\text{RSTCONF}}$	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3/FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25[2]
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28[2]
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/L1RXD1A2	AG29[2]
PA4/$\overline{\text{REJECT2}}$/FCC2_UTM_RXADDR1/$\overline{\text{DONE4}}$	AG28[2]
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26[2]
PA6/L1RSYNCA1	AE24[2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2/L1TXD0A1	AH23[2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22[2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22[2]
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21[2]
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20[2]
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19[2]
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18[2]
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17[2]
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16[2]
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16[2]
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15[2]
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13[2]
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13[2]

Table 14. Pinout List (continued)

Pin Name	Ball
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[2]
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1[2]
PC31/CLK1/BRGO1	AD1[2]
PD4/BRGO8/L1TSYNCD1/L1GNTD1/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[2]
PD5/FCC1_UT16_TXD3/$\overline{\text{DONE1}}$	AD27[2]
PD6/FCC1_UT16_TXD4/$\overline{\text{DACK1}}$	AF29[2]
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC1_UTM_TXADDR4/FCC1_TXCLAV2	AF28[2]
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25[2]
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26[2]
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27[2]
PD11/$\overline{\text{L1RQB2}}$/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23[2]
PD12/SI1_L1ST2/L1RXDB1	AG23[2]
PD13/SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20[2]
PD15/FCC1_UT16_RXD1/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[2]
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18[2]
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17[2]
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3/ SPICLK/FCC2_UTM_RXADDR3/FCC2_UTS_RXADDR0	AF16[2]
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/FCC1_UTM_TXCLAV3/ SPISEL/BRGO1/FCC2_UTM_TXADDR3/FCC2_UTS_TXADDR0	AH15[2]
PD20/$\overline{\text{RTS4}}$/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14[2]
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13[2]
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12[2]
PD23/$\overline{\text{RTS3}}$/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/$\overline{\text{RTS2}}$/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/$\overline{\text{RTS1}}$/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4/FCC2_UTS_RXADDR1	AG1[2]
PD30/$\overline{\text{FCC2\_UTM\_TXENB}}$/$\overline{\text{FCC2\_UTS\_TXENB}}$/TXD1	AD4[2]
PD31/RXD1	AD2[2]
VCCSYN	AB3

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC8260. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

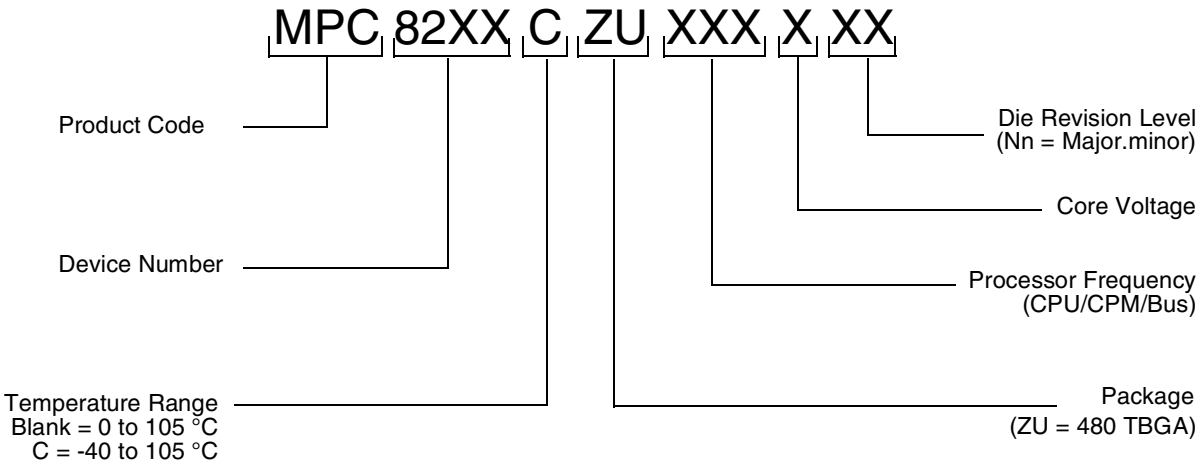


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 17 lists significant changes in each revision of this document.

Table 17. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	05/2010	Added a note about rise/fall time on CPM input pins above Table 8, “AC Characteristics for CPM Inputs.”
1.3	9/2005	• Document template update.
1.2	8/2003	• Note: In revision 0.7, sp30 (Table 10) was changed. This change was not previously recorded in this “Document Revision History” Table. • Addition of MPC8255 description to Section 1, “Features” • Addition of Figure 2 • Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2 • Addition of note 1 to Table 3 • Addition of notes or modifications to Figure 3 through Figure 8 • Addition of reference notes 4, 5, and 6 to Table 13 • Addition of note 2 to Table 14 • Addition of SPICLK to PC19 in Table 14. It is documented correctly in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 14.
1.1	5/2002	• Section 1, “Features”: updated minimum supported core frequency to 133 MHz • Addition of “Note” at bottom of page 5. • Table 13: Note 3.

Table 17. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1.0	3/2002	• Table 14: modified notes to pins AE11 and AF25. • Table 14: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.9	2/2002	• Table 14: additional note added to AE11
0.8	2/2002	• Table 7, Table 8, Table 9, and Table 10: revision 0.7 of this document incorrectly included values for 83 MHz. 83 MHz is not supported on the MPC8260. • Table 14: notes added to pins at AE11, AF25, U5, and V4.
0.7	11/2001	• Revision of Table 5, “Power Dissipation” • Modifications to Figure 9, Table 2,Table 10, Table 11 • Additional revisions to text and figures throughout
0.6	5/2001	Corrected the thermal values in Table 3, “Thermal Characteristics.”
0.2–0.5	—	Temporary revisions
0.1	1/2000	—
0	—	Initial version

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC8260EC
Rev. 2
05/2010