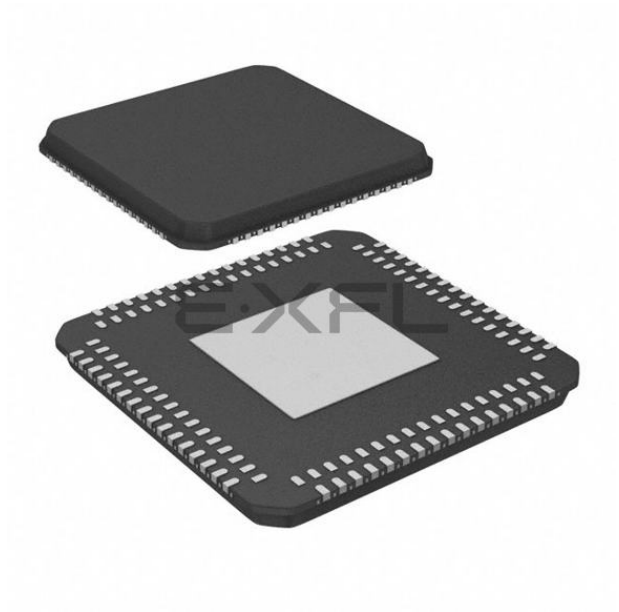

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Product Status	Active
Applications	Keyboard and Embedded Controller
Core Processor	ARM® Cortex®-M4
Program Memory Type	-
Controller Series	-
RAM Size	128KB
Interface	ACPI, BC-Link, I²C/SMBus, LPC, PECI, PS/2, SPI, UART
Number of I/O	116
Voltage - Supply	3.135V ~ 3.465V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	132-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	132-DQFN (11x11)
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2.0 BLOCK OVERVIEW

This Chapter provides an overview of the blocks in the MEC1322.

The block diagram of the MEC1322 is shown in Figure 2-1.

FIGURE 2-1: BLOCK DIAGRAM

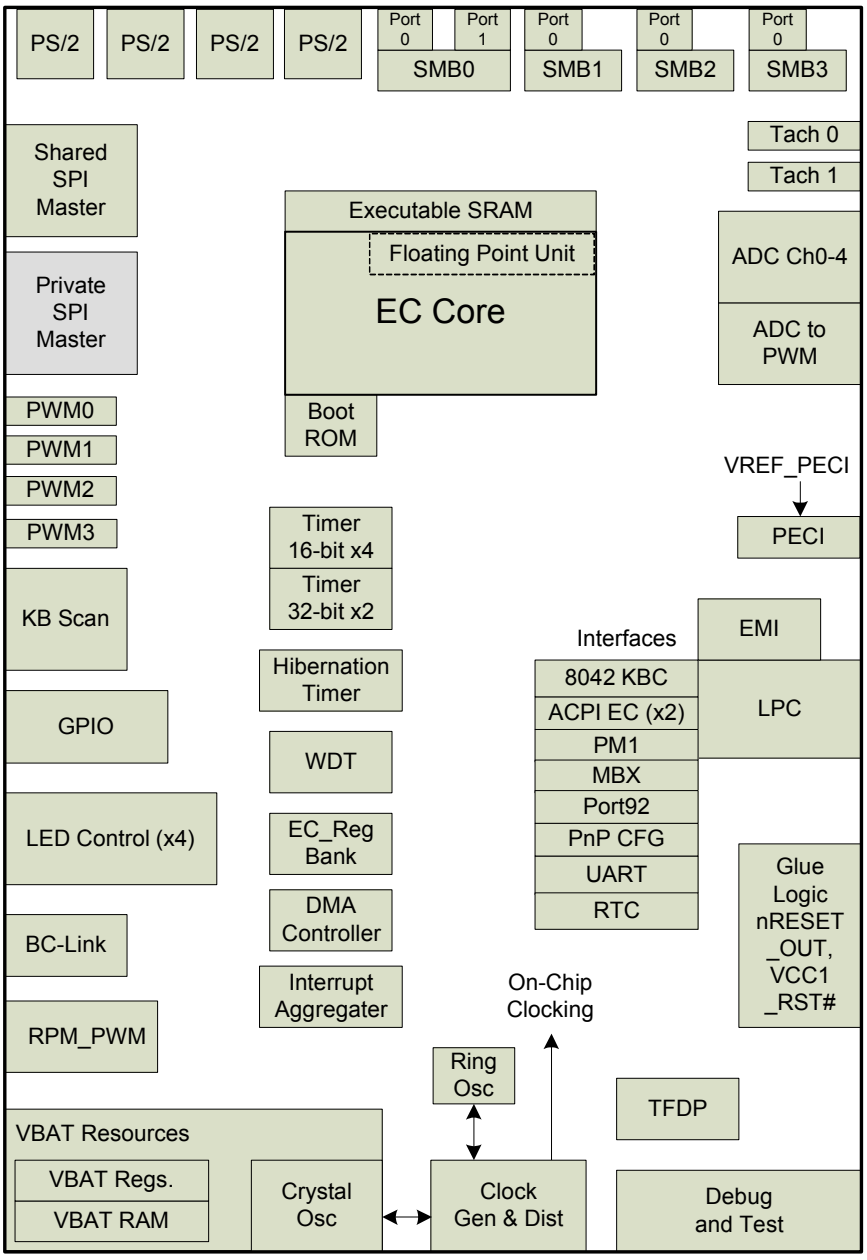

Table 2-1 on page 46 lists Address Ranges for each of the blocks.

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
8	PROCESSOR Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET
7	TFDP Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET
6	DMA Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET
5	PMC Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET
4	PWM0 Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET
3	RESERVED	RES		
2	TACH0 Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET
1	PECI Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET
0	INT Sleep Enable 0: block is free to use clocks as necessary. 1: block is commanded to sleep at next available moment.	R/W	0h	VCC1_RESET

Note 3-11 The basic timers in this device have an auto-reload mode. When this mode is selected, the block's clk_req equation is always asserted, which will prevent the device from gating its clock tree and going to sleep. When the firmware intends to put the device to sleep, none of the timers should be in auto-reload mode. Alternatively, use the timer's HALT function inside the control register to stop the timer in auto-reload mode so it can go to sleep.

3.9.4 EC CLOCK REQUIRED STATUS REGISTERS (EC_CLK_REQ_STS)

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	TIMER16_1 Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	VCC1_RESET
30	TIMER16_0 Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	VCC1_RESET
29	EC_REG_BANK Clock Required 0: block does NOT need clocks. 1: block requires clocks.	R	0h	VCC1_RESET
28:23	RESERVED	RES		

5.0 LPC INTERFACE

5.1 Introduction

The Intel® Low Pin Count (LPC) Interface is the LPC Interface used by the system host to configure the chip and communicate with the logical devices implemented in the design through a series of read/write registers. Register access is accomplished through the LPC transfer cycles defined in Table 5-8, "LPC Cycle Types Supported".

The Logical Devices implemented in the design are identified in Table 5-16, “I/O Base Address Registers,” on page 92. The Base Address Registers allow any logical device’s runtime registers to be relocated in LPC I/O space. All chip configuration registers for the device are accessed indirectly through the LPC I/O Configuration Port (see Section 5.8.3, "Configuration Port," on page 83).

LPC memory cycles may also be used to access the Base Address Registers of certain devices.

5.2 References

- Intel® Low Pin Count (LPC) Interface Specification, v1.1
- PCI Local Bus Specification, Rev. 2.2
- Serial IRQ Specification for PCI Systems Version 6.0.
- PCI Mobile Design Guide Rev 1.0

5.3 Terminology

This table defines specialized terms localized to this feature.

TABLE 5-1: TERMINOLOGY

Term	Definition
System Host	Refers to the external CPU that communicates with this device via the LPC Interface.
Logical Devices	Logical Devices are LPC accessible features that are allocated a Base Address and range in LPC I/O address space
Runtime Register	Runtime Registers are register that are directly I/O accessible by the System Host via the LPC interface. These registers are defined in Section 5.10, "Runtime Registers," on page 93.
Configuration Registers	Registers that are only accessible in CONFIG_MODE. These registers are defined in Section 5.9, "LPC Configuration Registers," on page 88.
EC_Only Registers	Registers that are not accessible by the System Host. They are only accessible by an internal embedded controller. These registers are defined in Section 5.11, "EC-Only Registers," on page 94.

TABLE 5-19: RUNTIME REGISTER SUMMARY

Offset	Register Name
00h	INDEX Register
01h	DATA Register

Note: The LPC Runtime Register space has been used to implement the INDEX and DATA registers in the Configuration Port. In CONFIG_MODE, the Configuration Port is used to access the Configuration Registers.

5.10.1 INDEX REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	INDEX The INDEX register, which is part of the Configuration Port, is used as a pointer to a Configuration Register Address. **Note:** For a description of accessing the Configuration Port see Section 5.8.3, "Configuration Port," on page 83.	R/W	0h	VCC1_RESET

5.10.2 DATA REGISTER

Offset	01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	DATA The DATA register, which is part of the Configuration Port, is used to read or write data to the register currently being selected by the INDEX Register. **Note:** For a description of accessing the Configuration Port see Section 5.8.3, "Configuration Port," on page 83	R/W	0h	VCC1_RESET

5.11 EC-Only Registers

Note: EC-Only registers are not accessible by the LPC interface.

The registers listed in Table 5-21, "EC-Only Register Summary" are for a single instance of the LPC Interface. Their addresses are defined as a relative offset to the host base address defined in Table 5-20.

The following table defines the fixed host base address for each LPC Interface instance.

TABLE 5-20: EC-ONLY REGISTER ADDRESS RANGE TABLE

INSTANCE NAME	INSTANCE NUMBER	HOST	ADDRESS SPACE	BEGIN ADDRESS
LPC Interface	0	EC	32-bit internal address space	400F_3100h

The Begin Address indicates where the first register can be accessed in a particular address space for a block instance.

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1:0	Clock_Control This field controls when the host interface will permit the internal ring oscillator to be shut down. The choices are as follows: **0h:** Reserved **1h:** The host interface will permit the internal clocks to be shut down if the CLKRUN# signals “CLOCK STOP” and there are no pending serial interrupt request or DMA requests from devices associated with the device. The CLKRUN# signals “CLOCK STOP” by CLKRUN# being high for 5 LPCCLK’s after the raising edge of CLKRUN# **2h:** The host interface will permit the ring oscillator to be shut down after the completion of every LPC transaction. This mode may cause an increase in the time to respond to LPC transactions if the ring oscillator is off when the LPC transaction is detected. **3h:** The ring oscillator is not permitted to shut down as long as the host interface is active. When the ACTIVATE bit in the LPC Activate Register is 0, the Host Interface will permit the ring oscillator to be shut down and the Clock_Control Field is ignored. The Clock_Control Field only effects the Host Interface when the ACTIVATE bit in the LPC Activate Register is 1. Although the Host Interface can permit the internal oscillator to shut down, it cannot turn the oscillator on in response to an LPC transaction that occurs while the oscillator is off. In order to restart the oscillator in order to complete an LPC transaction, EC firmware must enable a wake interrupt on the LPC LFRAME# input. See the Application Note in Section 15.8.1, "WAKE Generation" for details.	R/W	0h	VCC1_RESET

5.11.5 MCHP TEST REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	RESERVED	RES	-	-
7:0	MCHP Reserved	R	0h	VCC1_RESET

5.11.6 MCHP TEST REGISTER

Offset	18h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:2	RESERVED	RES	-	-
1	MCHP Reserved	R/W	0h	VCC1_RESET
0	MCHP Reserved	R/W	0h	VCC1_RESET

Offset	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
1	SAEN Software-assist enable. 1=This bit allows control of the GATEA20 signal via firmware 0=GATEA20 corresponds to either the last Host-initiated control of GATEA20 or the firmware write to the Keyboard Control Register or the EC AUX Data Register.	R/W	0h	VCC1_RESET
0	UD3 User-defined data. Readable and writable by the EC when written by the EC at its EC-only alias.	R/W	0h	VCC1_RESET

11.15.5 EC AUX DATA REGISTER

Offset	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	EC_AUX_DATA This 8-bit register is write-only. When written, the C/D in the Keyboard Status Read Register is cleared to ‘0’, signifying data, and the IBF in the same register is set to ‘1’. When the Runtime Register at offset 0h is read by the Host, it functions as the EC_HOST Data / AUX Data Register.	W	0h	VCC1_RESET

11.15.6 PCOBF REGISTER

Offset	14h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	-	-
0	PCOBF For a description of this bit, see Section 11.10.1, "PCOBF Description".	R/W	0h	VCC1_RESET

13.12.1 EC_PM_STS REGISTER

Offset	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	UD	R/W	00h	VCC1_RESET
0	EC_SCI_STS If the EC_SCI_STS bit is “1”, an interrupt is generated on the EC_SCI# pin.	R/W	00h	VCC1_RESET

Note: This register is only accessed by the EC. There is no host access to this register.

TABLE 15-20: BIT DEFINITIONS FOR GIRQ17 SOURCE, ENABLE, AND RESULT REGISTERS

Bit	Block Instance Name	Source Name	Wake	Source Description
13	MCHP Reserved	MCHP Reserved	N	MCHP Reserved
14	PS2_0	PS2 ACT	N	PS2_0 Activity Interrupt from PS/2 Block
15	PS2_1	PS2 ACT	N	PS2_1 Activity Interrupt from PS/2 Block
16	PS2_2	PS2 ACT	N	PS2_2 Activity Interrupt from PS/2 Block
17	PS2_3	PS2 ACT	N	PS2_3 Activity Interrupt from PS/2 Block
18	RTC	RTC	Y	RTC Interrupt
19	RTC ALARM	RTC ALARM	Y	RTC Alarm Interrupt
20	HTIMER	HTIMER	Y	Signal indicating that the hibernation timer is enabled and has expired.
21	KEYSCAN	KSC_INT	N	Keyboard Scan Interface runtime interrupt
22	KEYSCAN wake	KSC_INT_WAKE	Y	Keyboard Scan Interface wake interrupt
23	RPM_INT Stall	Fan Stall Status Interrupt	N	RPM-PWM Interface DRIVE_FAIL & FAN_SPIN indication
24	RPM_INT Spin	Fan Fail/Spin Status Interrupt	N	RPM-PWM Interface SPIN indication
25	PFR_Status	PFR_Status	N	Power-Fail and Reset Status Register events (VBAT POR and WDT).
26	PWM_WDT[0]	PWM_WDT	N	PWM watchdog time out interrupt from Blinking/Breathing PWM block
27	PWM_WDT[1]	PWM_WDT	N	PWM watchdog time out interrupt from Blinking/Breathing PWM block
28	PWM_WDT[2]	PWM_WDT	N	PWM watchdog time out interrupt from Blinking/Breathing PWM block
29	BCM_ERR	BCM_INT Err	N	BC_LINK Master Error Flag Interrupt
30	BCM_BUSY_CLR	BCM_INT Busy	N	BC_LINK Master Busy Clear Flag Interrupt
31	n/a	n/a	N	See Table 15-7, "GIRQx Source Register", Table 15-8, "GIRQx Enable Set Register", Table 15-10, "GIRQx Enable Clear Register", and Table 15-9, "GIRQx Result Register" for a definition of this bit for the Source, Enable, and Result registers.

15.9.11 GIRQ18

TABLE 15-21: BIT DEFINITIONS FOR GIRQ18 SOURCE, ENABLE, AND RESULT REGISTERS

Bit	Block Instance Name	Source Name	Wake	Source Description
0	SPI0 TX	TXBE_STS	N	SPI controller 0 Interrupt output to EC driven by TXBE status bit
1	SPI0 RX	RXBF_STS	N	SPI controller 0 Interrupt output to EC driven by RXBE status bit
2	SPI1 TX	TXBE_STS	N	SPI controller 1 Interrupt output to EC driven by TXBE status bit
3	SPI1 RX	RXBF_STS	N	SPI controller 1 Interrupt output to EC driven by RXBE status bit
4	PWM_WDT[3]	PWM_WDT	N	PWM watchdog time out interrupt from Blinking/Breathing PWM block
5	MCHP Reserved	MCHP Reserved	N	MCHP Reserved

TABLE 15-21: BIT DEFINITIONS FOR GIRQ18 SOURCE, ENABLE, AND RESULT REGISTERS

Bit	Block Instance Name	Source Name	Wake	Source Description
6	MCHP Reserved	MCHP Reserved	N	MCHP Reserved
7	MCHP Reserved	MCHP Reserved	N	MCHP Reserved
8	MCHP Reserved	MCHP Reserved	N	MCHP Reserved
9	MCHP Reserved	MCHP Reserved	N	MCHP Reserved
[30:10]	Reserved	Reserved	N	Reserved
31	n/a	n/a	N	See Table 15-7, "GIRQx Source Register", Table 15-8, "GIRQx Enable Set Register", Table 15-10, "GIRQx Enable Clear Register", and Table 15-9, "GIRQx Result Register" for a definition of this bit for the Source, Enable, and Result registers.

15.9.12 GIRQ19

TABLE 15-22: BIT DEFINITIONS FOR GIRQ19 SOURCE, ENABLE, AND RESULT REGISTERS

Bit	Block Instance Name	Source Name	Wake	Source Description
0	VCC_PWRGD	VCC_PWRGD	Y	VCC_PWRGD interrupt from pin (see Note 15-2 on page 215).
1	LRESET#	LRESET#	Y	LRESET# interrupt from pin (see Note 15-2 on page 215).
[30:2]	Reserved	Reserved	N	Reserved
31	n/a	n/a	N	See Table 15-7, "GIRQx Source Register", Table 15-8, "GIRQx Enable Set Register", Table 15-10, "GIRQx Enable Clear Register", and Table 15-9, "GIRQx Result Register" for a definition of this bit for the Source, Enable, and Result registers.

15.9.13 GIRQ20

TABLE 15-23: BIT DEFINITIONS FOR GIRQ20 SOURCE, ENABLE, AND RESULT REGISTERS

Bit	Block Instance Name	Source Name	Wake	Source Description
[4:0]	GPIO[204:200]	GPIO_Event	Y	Bits[0:4] are controlled by the GPIO_Events generated by GPIO200 through GPIO204, respectively. The GPIO Interface can generate an interrupt source event on a high level, low level, rising edge and falling edge, as configured by the Interrupt Detection (int_det) bits in the Pin Control Register associated with the GPIO signal function.
5	Reserved	Reserved	N	Reserved
6	GPIO206	GPIO_Event	Y	Bit 6 is controlled by the GPIO_Events generated by GPIO206. The GPIO Interface can generate an interrupt source event on a high level, low level, rising edge and falling edge, as configured by the Interrupt Detection (int_det) bits in the Pin Control Register associated with the GPIO signal function.
7	Reserved	Reserved	N	Reserved

segments fields in each of the following registers (see Table 28-11): the LED Update Stepsize Register register and the LED Update Interval Register register. In Asymmetric mode the rising ramp rate uses 4 of the 8 segments fields and the falling ramp rate uses the remaining 4 of the 8 segments fields (see Table 28-11).

The parameters MIN, MAX, HD, LD and the 8 fields in LED_STEP and LED_INT determine the brightness range of the LED and the rate at which its brightness changes. See the descriptions of the fields in Section 28.10, "EC-Only Registers", as well as the examples in Section 28.9.3, "Breathing Examples" for information on how to set these fields.

TABLE 28-11: SYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 28-3, "Clipping Example"	Duty Cycle	Segment Index	Symmetric Mode Register Fields Utilized	
X	000xxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
X	001xxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
X	010xxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]
X	011xxxxxb	011b	STEP[3]/INT[3]	Bits[15:12]
X	100xxxxxb	100b	STEP[4]/INT[4]	Bits[19:16]
X	101xxxxxb	101b	STEP[5]/INT[5]	Bits[23:20]
X	110xxxxxb	110b	STEP[6]/INT[6]	Bits[27:24]
X	111xxxxxb	111b	STEP[7]/INT[7]	Bits[31:28]
Note: In Symmetric Mode the Segment_Index[2:0] = Duty Cycle Bits[7:5]				

TABLE 28-12: ASYMMETRIC BREATHING MODE REGISTER USAGE

Rising/ Falling Ramp Times in Figure 28-3, "Clipping Example"	Duty Cycle	Segment Index	Asymmetric Mode Register Fields Utilized	
Rising	00xxxxxxb	000b	STEP[0]/INT[0]	Bits[3:0]
Rising	01xxxxxxb	001b	STEP[1]/INT[1]	Bits[7:4]
Rising	10xxxxxxb	010b	STEP[2]/INT[2]	Bits[11:8]
Rising	11xxxxxxb	011b	STEP[3]/INT[3]	Bits[15:12]
falling	00xxxxxxb	100b	STEP[4]/INT[4]	Bits[19:16]
falling	01xxxxxxb	101b	STEP[5]/INT[5]	Bits[23:20]
falling	10xxxxxxb	110b	STEP[6]/INT[6]	Bits[27:24]
falling	11xxxxxxb	111b	STEP[7]/INT[7]	Bits[31:28]
Note: In Asymmetric Mode the Segment_Index[2:0] is the bit concatenation of following: Segment_Index[2] = (FALLING RAMP TIME in Figure 28-3, "Clipping Example") and Segment_Index[1:0] = Duty Cycle Bits[7:6].				

28.9.2 BLINKING CONFIGURATION

The Delay counter and the PWM counter are the same as in the breathing configuration, except in this configuration they are connected differently. The Delay counter is clocked on either the 32.768 KHz clock or the 48 MHz clock, rather than the output of the PWM. The PWM counter is clocked by the zero output of the Delay counter, which functions as a prescalar for the input clocks to the PWM. The Delay counter is reloaded from the LD field of the LED_DELAY register. When the LD field is 0 the input clock is passed directly to the PWM counter without prescaling. In Blinking/PWM mode the PWM counter is always 8-bit, and the PSIZE parameter has no effect.

The frequency of the PWM pulse waveform is determined by the formula:

$$f_{PWM} = \frac{f_{clock}}{(256 \times (LD + 1))}$$

where f_{PWM} is the frequency of the PWM, f_{clock} is the frequency of the input clock (32.768 KHz clock or 48 MHz clock) and LD is the contents of the LD field.

31.11.1 BC-LINK STATUS REGISTER

Offset	00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:4	Reserved	R	-	-
7	RESET When this bit is ‘1’the BC_Link Master Interface will be placed in reset and be held in reset until this bit is cleared to ‘0’. Setting RESET to ‘1’ causes the BUSY bit to be set to ‘1’. The BUSY remains set to ‘1’ until the reset operation of the BC Interface is completed, which takes approximately 48 BC clocks. The de-assertion of the BUSY bit on reset will not generate an interrupt, even if the BC_BUSY_CLR_INT_EN bit is ‘1’. The BUSY bit must be polled in order to determine when the reset operation has completed.	R/W	1h	VCC1_RESET
6	BC_ERR This bit indicates that a BC Bus Error has occurred. If an error occurs this bit is set by hardware when the BUSY bit is cleared. This bit is cleared when written with a ’1’. An interrupt is generated If this bit is ‘1’ and BC_ERR_INT_EN bit is ‘1’. Errors that cause this interrupt are: • Bad Data received by the BASE (CRC Error) • Time-out caused by the COMPANION not responding. All COMPANION errors cause the COMPANION to abort the operation and the BASE to time-out.	R/WC	0h	VCC1_RESET
5	BC_ERR_INT_EN This bit is an enable for generating an interrupt when the BC_ERR bit is set by hardware. When this bit is ‘1’, the interrupt signal is enabled. When this bit is ‘0’, the interrupt is disabled.	R/W	0b	VCC1_RESET
4	BC_BUSY_CLR_INT_EN This bit is an enable for generating an interrupt when the BUSY bit in this register is cleared by hardware. When this bit is set to ‘1’, the interrupt signal is enabled. When the this bit is cleared to ‘0’, the interrupt is disabled. When enabled, the interrupt occurs after a BC Bus read or write.	R/W	0h	VCC1_RESET
3:1	Reserved	R	-	-
0	BUSY This bit is asserted to ‘1’ when the BC interface is transferring data and on reset. Otherwise it is cleared to ‘0’. When this bit is cleared by hardware, an interrupt is generated if the BC_BUSY_CLR_INT_EN bit is set to ‘1’.	R	1h	VCC1_RESET

31.11.2 BC-LINK ADDRESS REGISTER

Offset	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	-	-
7:0	ADDRESS Address in the Companion for the BC-Link transaction.	R/W	0h	VCC1_RESET

Address (Hex)	HW Block Instance Name	HW Block Instance No.	Reg. Bank Name	Reg. Instance Name
4000A003	RPM Fan Control	0	RPM_FAN	Fan Configuration 2
4000A004	RPM Fan Control	0	RPM_FAN	MCHP Reserved
4000A005	RPM Fan Control	0	RPM_FAN	Gain
4000A006	RPM Fan Control	0	RPM_FAN	Fan Spin Up Configuration
4000A007	RPM Fan Control	0	RPM_FAN	Fan Step
4000A008	RPM Fan Control	0	RPM_FAN	Fan Minimum Drive
4000A009	RPM Fan Control	0	RPM_FAN	Valid Tach Count
4000A00A	RPM Fan Control	0	RPM_FAN	Fan Drive Fail Band Low Byte
4000A00B	RPM Fan Control	0	RPM_FAN	Fan Drive Fail Band High Byte
4000A00C	RPM Fan Control	0	RPM_FAN	Tach Target Low Byte
4000A00D	RPM Fan Control	0	RPM_FAN	Tach Target High Byte
4000A00E	RPM Fan Control	0	RPM_FAN	Tach Reading Low Byte
4000A00F	RPM Fan Control	0	RPM_FAN	Tach Reading High Byte
4000A010	RPM Fan Control	0	RPM_FAN	PWM Driver Base Frequency
4000A011	RPM Fan Control	0	RPM_FAN	Fan Status
4000A012	RPM Fan Control	0	RPM_FAN	Reserved
4000A014	RPM Fan Control	0	RPM_FAN	RPM Fan Test
4000A015	RPM Fan Control	0	RPM_FAN	RPM Fan Test1
4000A016	RPM Fan Control	0	RPM_FAN	RPM Fan Test2
4000A017	RPM Fan Control	0	RPM_FAN	RPM Fan Test3
4000A400	VBAT Registers	0	VBAT_EC_REG_BANK	Power-Fail and Reset Status Register
4000A404	VBAT Registers	0	VBAT_EC_REG_BANK	Control
4000A800	VBAT Powered RAM	0	Registers	VBAT Backed Memory
4000AC00	SMB Device Interface	1	SMB_EC_Only	Control Register
4000AC00	SMB Device Interface	1	SMB_EC_Only	Status Register
4000AC01	SMB Device Interface	1	SMB_EC_Only	Reserved
4000AC04	SMB Device Interface	1	SMB_EC_Only	Own Address Register
4000AC06	SMB Device Interface	1	SMB_EC_Only	Reserved
4000AC08	SMB Device Interface	1	SMB_EC_Only	Data
4000AC09	SMB Device Interface	1	SMB_EC_Only	Reserved
4000AC0C	SMB Device Interface	1	SMB_EC_Only	SMBus Master Command Register
4000AC10	SMB Device Interface	1	SMB_EC_Only	SMBus Slave Command Register
4000AC14	SMB Device Interface	1	SMB_EC_Only	PEC Register
4000AC15	SMB Device Interface	1	SMB_EC_Only	Reserved
4000AC18	SMB Device Interface	1	SMB_EC_Only	DATA_TIMING2
4000AC19	SMB Device Interface	1	SMB_EC_Only	Reserved
4000AC20	SMB Device Interface	1	SMB_EC_Only	Completion Register
4000AC24	SMB Device Interface	1	SMB_EC_Only	Idle Scaling Register