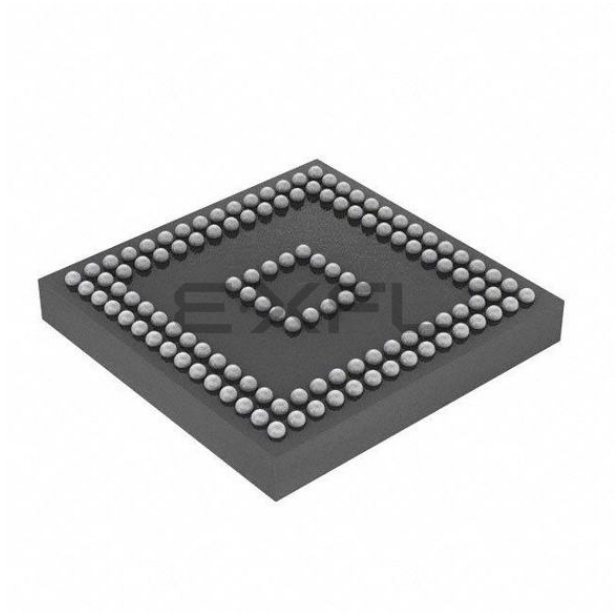

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	DMA, I²S, LCD, POR, WDT
Number of I/O	66
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 12x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LFBGA, CSPBGA
Supplier Device Package	120-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm350bbcz-rl

GENERAL DESCRIPTION

The ADuCM350 is a complete, coin cell powered, high precision, meter-on-chip for portable device applications for applications such as point-of-care diagnostics and body-worn devices for monitoring vital signs. The ADuCM350 is designed for high precision amperometric, voltametric, and impedometric measurement capabilities.

The ADuCM350 analog front end (AFE) features a 16-bit, precision, 160 kSPS analog-to-digital converter (ADC); 0.17% precision voltage reference; 12-bit, no missing codes digital-to-analog converter (DAC); and a reconfigurable ultralow leakage switch matrix. The ADuCM350 also includes an ARM® Cortex-M3-based processor, memory, and all I/O connectivity to support portable meters with display, USB communication, and active sensors. The ADuCM350 is available in a 120-lead, 8 mm × 8 mm CSP_BGA and operates from −40°C to +85°C.

To support extremely low dynamic and hibernate power management, the ADuCM350 provides a collection of power modes and features, such as dynamic and software controlled clock gating and power gating.

The AFE is connected to the ARM Cortex-M3 via an advanced high performance bus (AHB) slave interface on the advanced microcontroller bus architecture (AMBA) matrix, as well as direct memory access (DMA) and interrupt connections.

DAC/RCF/PGA Specifications

Table 3. DAC/PGA/RCF Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DAC					
Output Range	−600		+600	mV	As seen by sensor
Resolution			12	Bits	
Integral Nonlinearity (INL)		±0.85		LSB	Measured at an output of the excitation loop, using gain = 1 and default DAC clock (16 MHz ÷ 49 DAC clock speed)
Differential Nonlinearity (DNL)	−1		+1	LSB	Measured at an output of the excitation loop, using gain = 1 and default DAC clock (16 MHz ÷ 49 DAC clock speed)
Full-Scale Error					
Positive		±0.2		% FSR	PGA (gain = 1), measured at an output of the excitation loop, DAC code = 0xE00
		±1		% FSR	PGA (gain = 0.025), measured at an output of the excitation loop, DAC code = 0xE00
Negative		±0.2		% FSR	PGA (gain = 1), measured at an output of the excitation loop, DAC code = 0x200
		±1		% FSR	PGA (gain = 0.025), measured at an output of the excitation loop, DAC code = 0x200
Offset Error, Midscale		±1		mV	PGA (gain = 1 or gain = 0.025), measured at an output of the excitation loop across RCAL
Clocking Frequency	280.7	320	380.95	kHz	
PROGRAMMABLE GAIN AMPLIFIER (PGA)					
Gain from PGA in State 0		1			Covered by DAC full-scale error measured on an output of the excitation loop
Gain from PGA in State 1		0.025			Covered by DAC full-scale error measured on an output of the excitation loop
RECONSTRUCTION FILTER (RCF)					
3 dB Corner Frequency		50		kHz	

[1] There may be some system offsets and gain errors that can be calibrated at the system level to improve dc accuracy. Hence, the voltage swing at the output of the DAC is ±800 mV to guarantee ±600 mV swing on the sensor.

SWITCH MATRIX SPECIFICATIONS

Table 4. Switch Matrix Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
R_{ON}[1]					
Current Carrying Switches					
Dx, DR1, Tx, and TR2		40	50	Ω	
IVS		40	75	Ω	
Noncurrent Carrying Switches					
Px, Nx, and NR2	600		900	Ω	
PR1	600		950	Ω	
NL	260		350	Ω	
PL	210		260	Ω	
DC OFF LEAKAGE[2]					
T and N Switches		370		pA	Sum value of four T switches and four N switches
P Switches		340		pA	Sum value of four P switches
D Switches		350		pA	Sum value of four D switches

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ON LEAKAGE[2]					
T, N, and P Switches		530		pA	Sum value for 25 switches, including NL
D Switches		340		pA	Sum value for eight switches

[1] R_{ON} characterized with a voltage sweep from 0 V to VCCM. Production tested at 1.8 V.
[2] See Figure 38 as a reference. The AFE x pin is driven to 0.2 V.

TRANSIMPEDANCE AMPLIFIER SPECIFICATIONS

Table 5. Transimpedance Amplifier Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSIMPEDANCE AMPLIFIER					
Maximum Current Sink/Source		±5		mA	Ensure an R_{TIA} selection to generate ±750 mV swing for optimal linearity performance
Short-Circuit Protection Functionality		10		mA	

ADC SPECIFICATIONS

Table 6. ADC Specifications[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
Input Range	0.35		1.85	V	Internal reference
No Missing Codes		16		Bits	
DNL		±0.9		LSB	
INL		±0.7		LSB	@ 160 kSPS with respect to an optimal voltage range of ±750 mV, from 0°C to 50°C
		±1		LSB	@ 160 kSPS with respect to an optimal voltage range of ±750 mV, from −40°C to +85°C
Sample Rate After Decimation		160		kSPS	
3 dB Bandwidth		54		kHz	

[1] R_{TIA} = 7.5 kΩ, C_{TIA} = 220 pF; ±100 µA current measurement.

TEMPERATURE SENSOR SPECIFICATIONS

Table 7. Temperature Sensor Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					
Accuracy		±1		°C	0°C to 50°C, trimmed at 25°C
		±2		°C	−40°C to +85°C, trimmed at +25°C

CapTouch

Table 8. CapTouch Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CapTouch™ CHARACTERISTICS					
Core Resolution		14		Bits	
Core SNR	60			dB	1 kHz test tone, input range of ADC = 1.8 V
CAPT_x		±10		nA	GPIO leakage test
Update Rate	7.5		1E6	µs	Programmable, dependent on configuration
Update Rate per Sensor	7.5			µs	No filtering enabled, clock = 16 MHz
CAPT_x Input Range		±8		pF	ΔC_{IN} is register programmable from 0.5 pF to 9.3 pF
CAPT_x Offset (CapDAC) Range		75		pF	

Flash/General-Purpose Flash

Table 12. Flash/General-Purpose Flash Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FLASH/GP FLASH					
Endurance[1]	20,000			Cycles	
Erase Time		20		ms	@ 1.8 V
Program Time		20		µs	@ 1.8 V
Data Retention[2]		100		Years	Below room temperature

[1] Endurance is qualified to 10,000 cycles as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.

Digital Inputs/Outputs: Specified

Specified pin supply range from 2.5 V to 3.6 V.

Table 13. Digital Inputs and Outputs[1] Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PIN SUPPLY	2.5	3	3.6	V	
Impedance					
Pull-Down		20		kΩ	I_{SINK} < 10 µA
Pull-Up		15		kΩ	I_{SOURCE} < 10 µA
Internal Pull-Up/Pull-Down Enabled Leakage[2]		200		µA	
Digital I/O Leakage Current		.01	1	µA	
Input Capacitance		10		pF	
Input Voltage					
Low (V_{INL})			0.3 × pin supply	V	
High (V_{INH})	0.7 × pin supply			V	
Output Voltage					
Low (V_{OL})			0.4	V	I_{SINK} = 1.0 mA
V_{OL} High Drive		0.4		V	I_{SINK} = 1.6 mA
High (V_{OH})[3]	Pin supply − 0.4			V	I_{SOURCE} = 1.0 mA
V_{OH} High Drive		2.4		V	I_{SOURCE} = 1.6 mA

[1] Includes GPIO, debug, SPI, I²C, PDI, LCD, I²S, and beeper.
[2] See Table 35 for details regarding bumps/pins that have pull-up resistors.
[3] I²C does not drive out a high voltage; it uses external pull-up resistors.

Digital Inputs/Outputs: Functional

Functional pin supply range from 1.65 V to 2.5 V.

Table 14. Digital Inputs/Outputs: Functional Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PIN SUPPLY	1.65		2.5	V	
Input Voltage					
Low (V_{INL})		0.3 × pin supply		V	
High (V_{INH})		0.7 × pin supply		V	
Output Voltage					
Low (V_{OL})		0.45		V	I_{SINK} = 1.0 mA
High (V_{OH})[1]		Pin supply − 0.5		V	I_{SOURCE} = 1.0 mA

[1] I²C does not drive out a high voltage; it uses external pull-up resistors.

TIMING CHARACTERISTICS

LCD Segment/Common Timing Specifications

Table 26. LCD Segment/Common Timing Specifications[1, 2]

				Static Mux		4× Mux	
FRAMESEL[3]	FRAMESEL[2]	FRAMESEL[1]	FRAMESEL[0]	f_{LCD} (Hz)	Frame Rate (Hz)	f_{LCD} (Hz)	Frame Rate (Hz)
0	0	0	0	256	128	1024	128
0	0	0	1	204.8	102.4	819.2	102.4
0	0	1	0	170.7	85.3	682.7	85.3
0	0	1	1	146.3	73.1	585.1	73.1
0	1	0	0	128	64	512	64
0	1	0	1	113.8	56.9	455.1	56.9
0	1	1	0	102.4	51.2	409.6	51.2
0	1	1	1	93.1	46.5	372.4	46.5
1	0	0	0	85.3	42.7	341.3	42.7
1	0	0	1	78.8	39.4	315.1	39.4
1	0	1	0	73.1	36.6	292.6	36.6
1	0	1	1	68.3	34.1	273.1	34.1
1	1	0	0	64	32	256	32
1	1	0	1	60.2	30.1	240.9	30.1
1	1	1	0	56.9	28.4	227.6	28.4
1	1	1	1	53.9	26.9	215.6	26.9

[1] $f_{LCD} = f_{BCLK}/(FRAMESEL + 4)$. See the UG-587 hardware reference manual for details
[2] FRAMESEL[3], FRAMESEL[2], FRAMESEL[1], and FRAMESEL[0] indicate the bit numbers in the LCD_COM register.

I²C Timing

Capacitive load for each of the I²C bus lines (C_B) = 400 pF maximum as per I²C bus specifications; I²C timing is guaranteed by design and not production tested.

Table 27. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Min	Max	Unit
t_L	Clock low pulse width	1300		ns
t_H	Clock high pulse width	600		ns
t_{SHD}	Start condition hold time	600		ns
t_{DSU}	Data setup time	100		ns
t_{DHD}[1]	Data hold time	0		ns
t_{RSU}	Setup time for repeated start	600		ns
t_{PSU}	Stop condition setup time	600		ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3		µs
t_R	Rise time for both clock and data	20 + 0.1 Cb	300	ns
t_F	Fall time for both clock and data	20 + 0.1 Cb	300	ns
t_{SUP}	Pulse width of spike suppressed	0	50	ns

[1] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{INH} (minimum) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Table 28. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Min	Max	Unit
t_L	Clock low pulse width	4.7		µs
t_H	Clock high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.7		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}[1]	Data hold time	0		µs
t_{RSU}	Setup time for repeated start	4.0		µs

Parameter	Description	Min	Max	Unit
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both clock and data		1	µs
t_F	Fall time for both clock and data		300	ns

[1] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{INH} (minimum) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

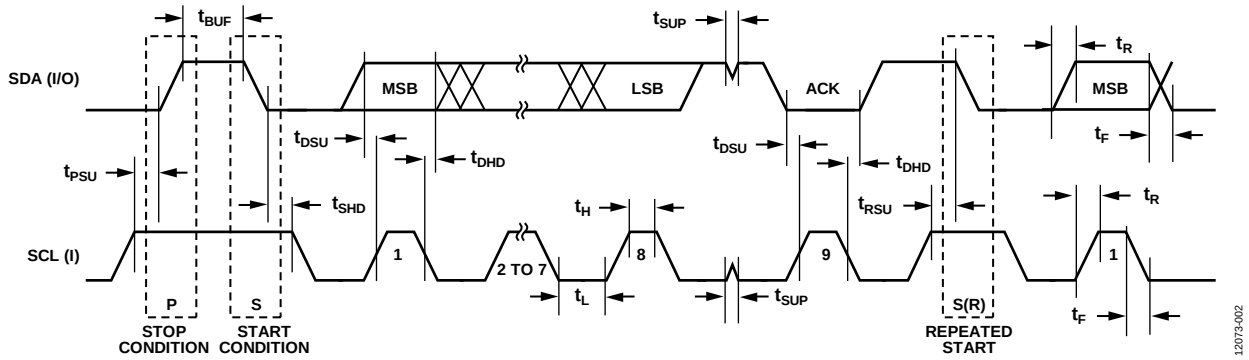

Figure 2. I²C-Compatible Interface Timing

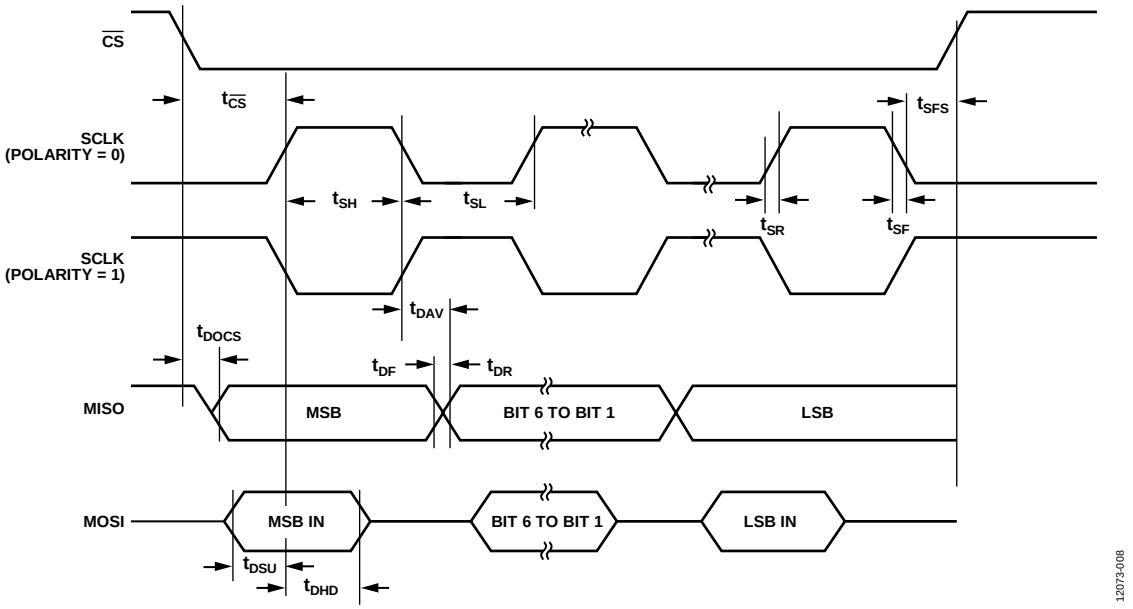

Figure 8. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 33.

Parameter	Rating
Supplies	
VCCM_ANA, VCCM_DIG, VLCDVDD, VDD_IO, VBACK to AGND_x/DGNDx	−0.3 V to +3.6 V
Decoupling	
DVDD, AVDD_RX/TX, VBIAS, VREF, VUSB	−0.3 V to +2.0 V
Digital Input/Output	
P0.x, P1.x, P2.x, P3.x, P4.x, BOOT, RESETX	−0.3 V to +3.6 V
TRACEx	−0.3 V to +3.6 V
Switch Matrix (RCAL 1, RCAL 2, AFE x)	−0.3 V to +3.6 V
TIA (TIA_I, TIA_O)	−0.3 V to +3.6 V
Analog Inputs (AN_x)	−0.3 V to +3.6 V
REF_EXCITE	−0.3 V to +1.98 V
VLCD FLY1, VLCD FLY2	−0.3 V to +3.6 V
V_LCD_13, V_LCD_23	−0.3 V to +3.6 V
VBUS to DGND	−0.3 V to +5.25 V
USB DM, USB DP to DGND	−0.3 V to +3.6 V
HF_XTALx, LF_XTALx	−0.3 V to +1.98 V
Analog Ground to Digital Ground	
AGND CTOUCH, AGND_RX/TX, AGND_REF to DGND, DGND1, DGND2, DGND USB	−0.3 V to +0.3 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages; assumes use of a JEDEC 4-layer board.

Table 34. Thermal Resistance

Package Type	θ_{JA}	Unit
CSP_BGA	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
SPI H					
R3	P0.12/SPIH_SCLK	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H Clock. This is a dual function pin.
P2	P0.13/SPIH_MISO	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H MISO. This is a dual function pin.
P3	P0.14/SPIH_MOSI	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H MOSI. This is a dual function pin.
M2	P0.15/SPIH_CS	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H Chip Select (Active Low). This is a dual function pin.
Other Serial Ports					
F14	P3.0/SPI0_SCLK	I/O	VDD_IO	Pull-up	GPIO/SPI 0 SCLK. This is a dual function pin.
G14	P3.1/SPI0_MISO	I/O	VDD_IO	Pull-up	GPIO/SPI 0 MISO. This is a dual function pin.
F15	P3.2/SPI0_MOSI	I/O	VDD_IO	Pull-up	GPIO/SPI 0 MOSI. This is a dual function pin.
F10	P3.3/SPI0_CS	I/O	VDD_IO	Pull-up	GPIO/SPI 0 Chip Select (Active Low). This is a dual function pin.
G10	P3.4/I2CSCL/SPI1_SCLK	I/O	VDD_IO	Pull-up	GPIO (External Interrupt 7)/I^2C Clock/SPI 1 SCLK. This is a multifunction pin.
H10	P3.5/I2CSD/SPI1_MISO	I/O	VDD_IO	Pull-up	GPIO/I2C Data/SPI 1 MISO. This is a multifunction pin.
G15	P3.6/UTX/TOUTB/SPI1_MOSI	I/O	VDD_IO	Pull-up	GPIO/UART Tx/Timer B Output/SPI 1 MOSI. This is a multifunction pin.
J10	P3.7/URX/TOUTC/SPI1_CS	I/O	VDD_IO	Pull-up	GPIO/UART Rx/Timer C Output/SPI 1 Chip Select (Active Low). This is a multifunction pin.
USB					
F1	USB DM	I/O	VCCM_DIG	N/A	USB Data −.
G1	USB DP	I/O	VCCM_DIG	N/A	USB Data +.
CapTouch Interface					
K15	P0.0/CAPT_A	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 1)/CapTouch A. This is a dual function pin.
J15	P0.1/CAPT_B	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 2)/CapTouch B. This is a dual function pin.
L15	P0.2/CAPT_C	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 3)/CapTouch C. This is a dual function pin.
K14	P0.3/CAPT_D	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 4)/CapTouch D. This is a dual function pin.
J14	P0.4/CAPT_E	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 5)/CapTouch E. This is a dual function pin.
L14	P0.5/CAPT_F	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 6)/CapTouch F. This is a dual function pin.
P14	AGND CTOUCH	G	N/A	N/A	Capacitance to Digital Converter AC Shield.
System Clocks					
P1	LF_XTAL1	A	RTC_VBACK	N/A	32 kHz XTAL Pin.
N1	LF_XTAL2	A	RTC_VBACK	N/A	32 kHz XTAL Pin.
D1	HF_XTAL1	A	DVDD	N/A	16 MHz XTAL Pin.
C1	HF_XTAL2	A	DVDD	N/A	16 MHz XTAL Pin.
Display					
E2	VLCD FLY1	A	VLCD VDD	N/A	LCD Flying Capacitor Top Plate.
F2	VLCD FLY2	A	VLCD VDD	N/A	LCD Flying Capacitor Bottom Plate.
D2	VLCDVDD	S	N/A	N/A	Full-Scale LCD Voltage Output or VLCD Supply.
C2	V_LCD_13	A	VLCD VDD	N/A	One-Third (1/3) LCD Voltage. Leave this pin as no connect.
B1	V_LCD_23	A	VLCD VDD	N/A	Two-Thirds (2/3) LCD Voltage. Leave this pin as no connect.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
Miscellaneous Digital Input/Output					
K8	RESETX	I	VCCM_DIG	Pull-up	Reset Pin (Active Low).
L1	P4.0/I2CSCL	I/O	VCCM_DIG	Pull-up	GPIO (External Interrupt 0)/I²C Clock. This is a dual function pin.
L2	P4.1/I2CSD	I/O	VCCM_DIG	Pull-up	GPIO/I²C Data. This is a dual function pin.
R1	P4.2/TOUTB	I/O	VCCM_DIG	Pull-up	GPIO/Timer B Output. This is a dual function pin.
R2	P0.10/TOUTC	I/O	VCCM_DIG	Pull-up	GPIO (External Interrupt 8)/Timer C Output. This is a dual function pin.
K2	P0.11	I/O	VCCM_DIG	Pull-up	GPIO (External Clock Input Pin).
N2	BOOT	I	VCCM_DIG	Pull-down	The device enters serial download mode if this pin is held high during, and for a short time after, a reset. It executes user code after any reset event or if the pin is low.
A1	DNC		N/A	N/A	Do Not Connect. Leave this pin floating.
Audio					
K6	P3.12/BEEP/BMCLK	I/O	VCCM_DIG	Pull-down	GPIO/Beeper Output Positive/I²S Bit Clock. This is a multifunction pin.
K7	P3.13/BEEPX/SDATA	I/O	VCCM_DIG	Pull-down	GPIO/Beeper Output Negative/I²S Serial Data Output. This is a multifunction pin.
J6	P3.14/LRCLK	I/O	VCCM_DIG	Pull-down	GPIO/I²S Frame Clock. This is a dual function pin.

[1] S is supply, A is analog input, I is digital input, O is digital output, I/O is digital input/output, and G is ground.
[2] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

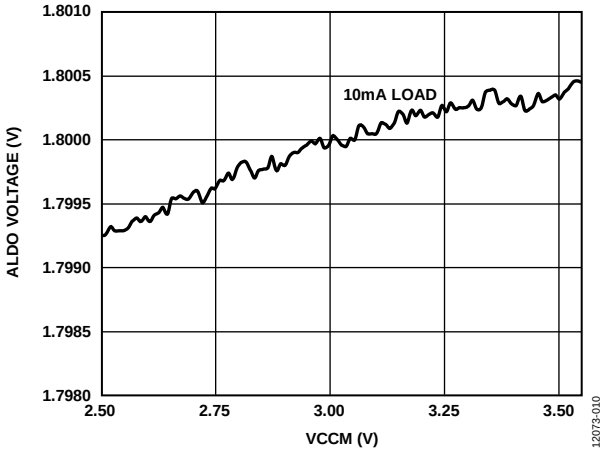

Figure 10. ALDO Line Regulation

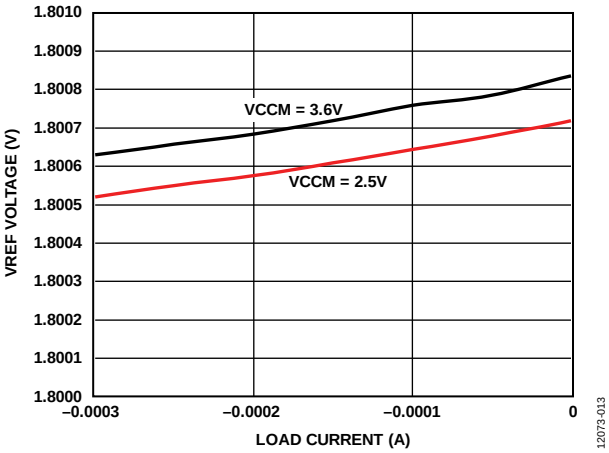

Figure 13. VREF Load Regulation

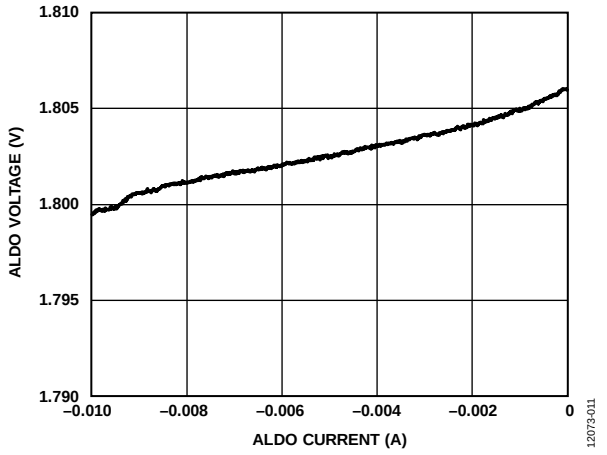

Figure 11. ALDO Load Regulation

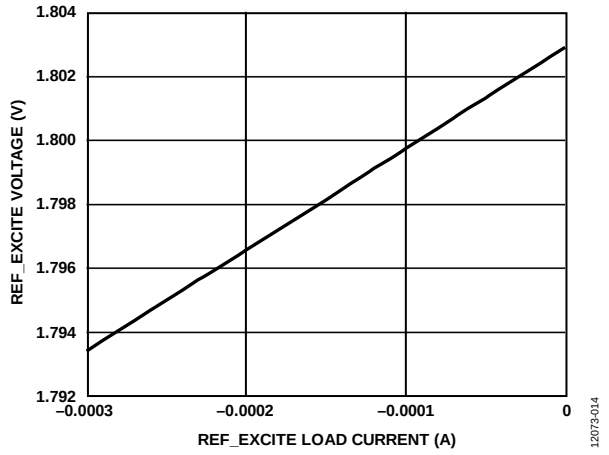

Figure 14. REF_EXCITE Load Regulation

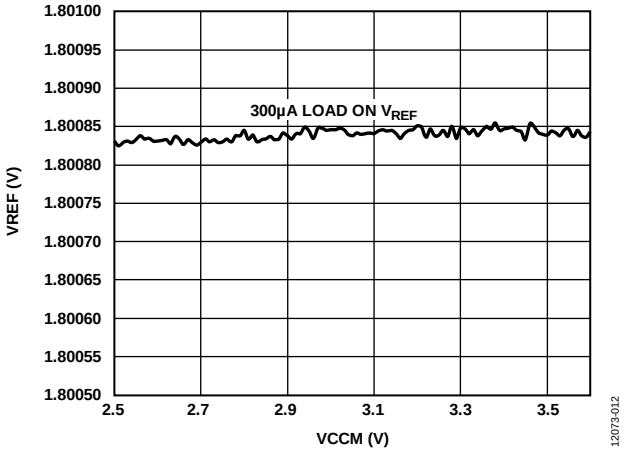

Figure 12. VREF Line Regulation

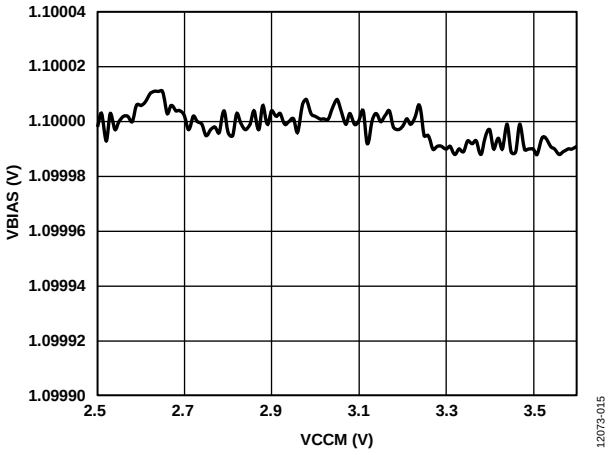

Figure 15. VBIAS Line Regulation

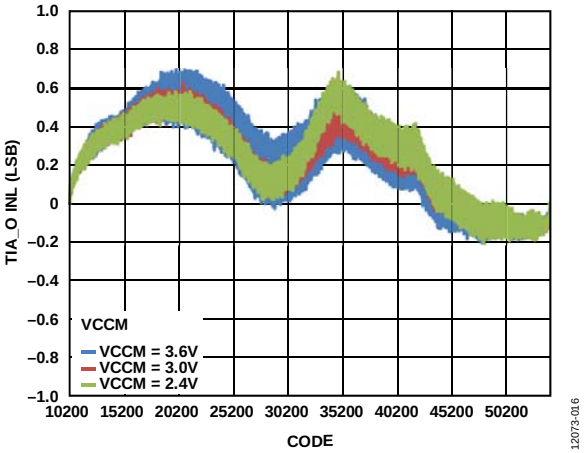

Figure 16. ADC TIA_O INL (16-Bit) vs. Code (±150 µA)

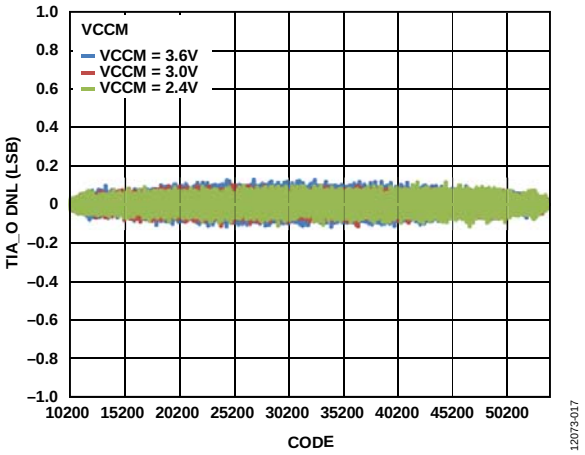

Figure 17. ADC ADC TIA_O DNL (16-Bit) vs. Code

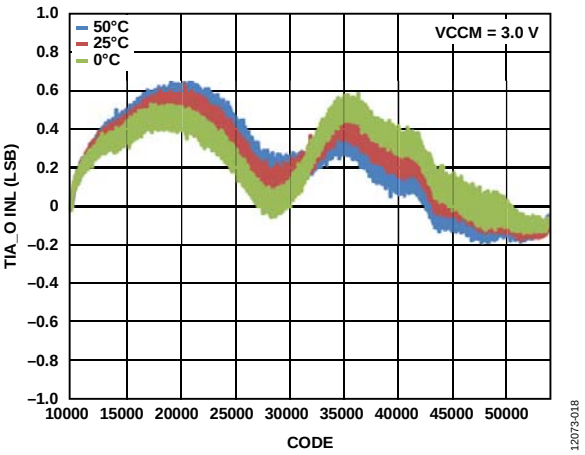

Figure 18. ADC ADC TIA_O INL (16-Bit) vs. Code (Temperature)

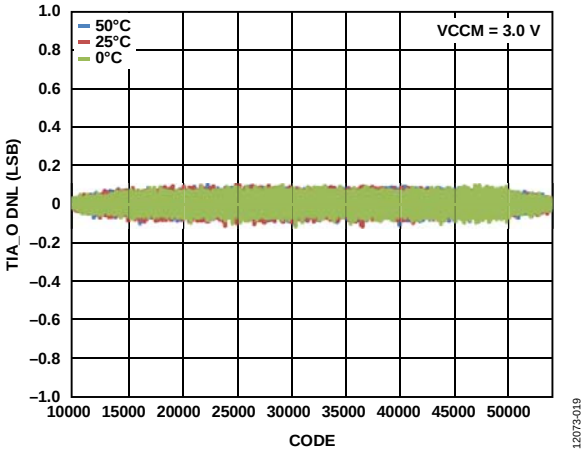

Figure 19. ADC TIA_O DNL (16-Bit) vs. Code (Temperature)

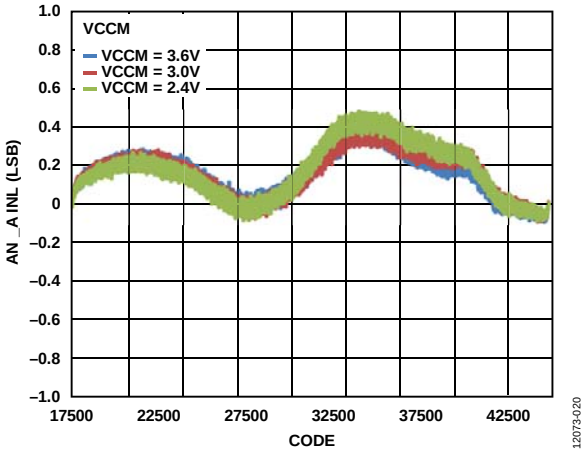

Figure 20. ADC AN_A INL (16-Bit) vs. Code

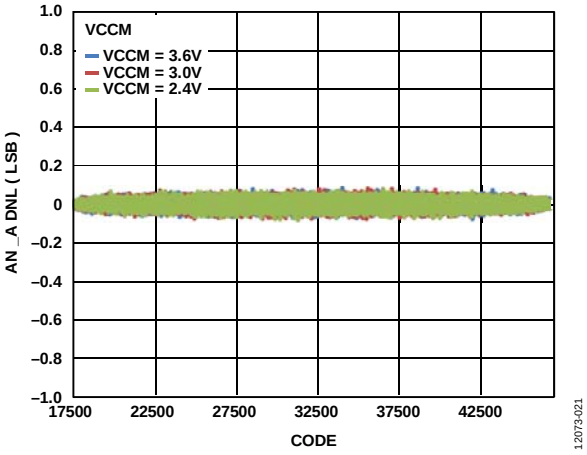

Figure 21. ADC AN_A DNL (16-Bit) vs. Code

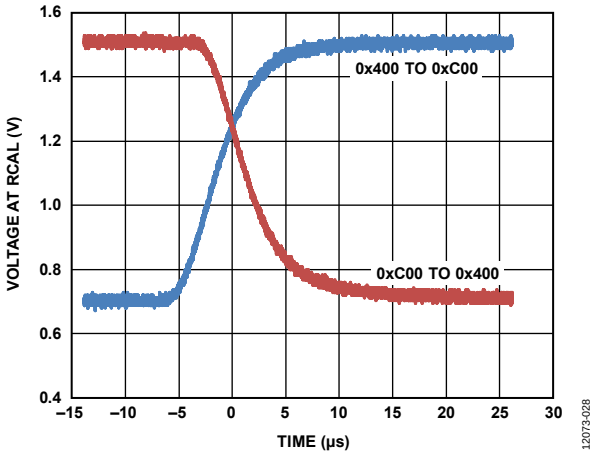

Figure 28. Settling Time of the DAC at RCAL

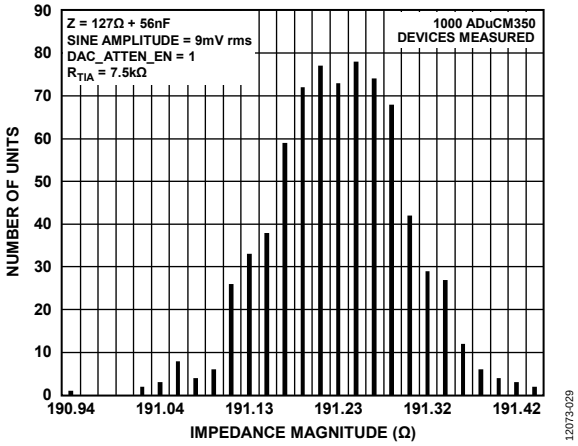

Figure 29. Impedance Measurement Magnitude Accuracy

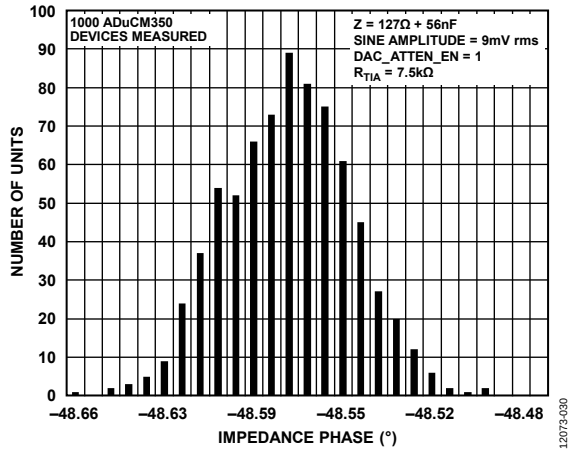

Figure 30. Impedance Measurement Phase Accuracy

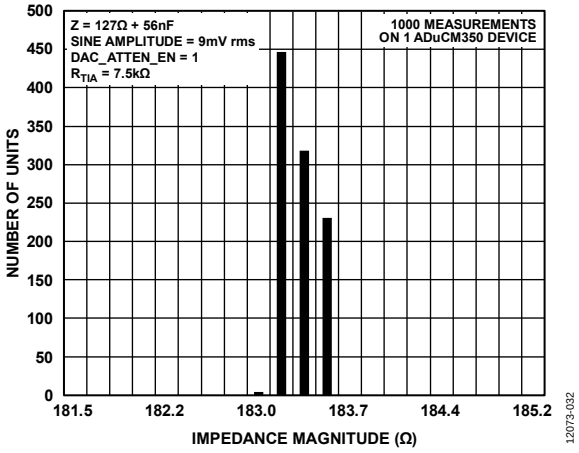

Figure 31. Impedance Measurement Magnitude Precision

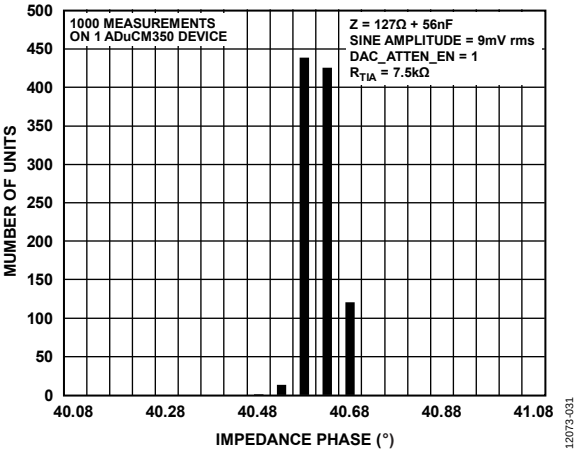

Figure 32. Impedance Measurement Phase Precision

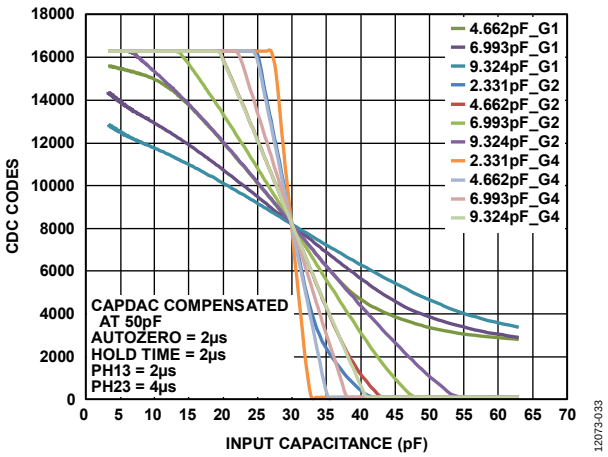

Figure 33. CapTouch Linearity

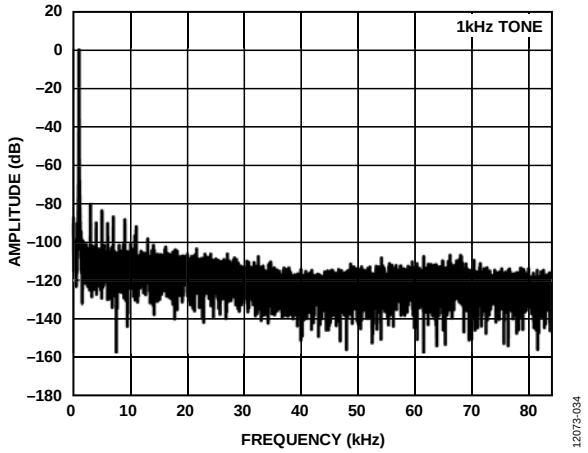

Figure 34. CapTouch SNR

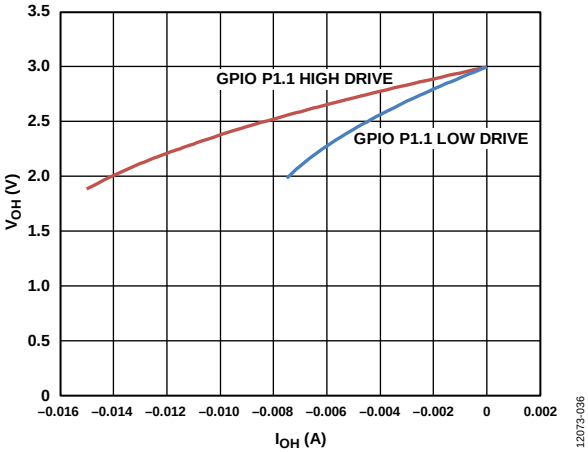

Figure 36. GPIO V_{OH} vs. I_{OH}

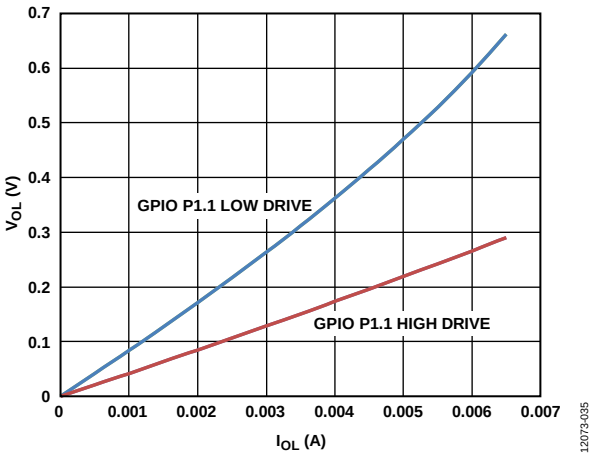

Figure 35. GPIO V_{OL} vs. I_{OL}

ANALOG FRONT END

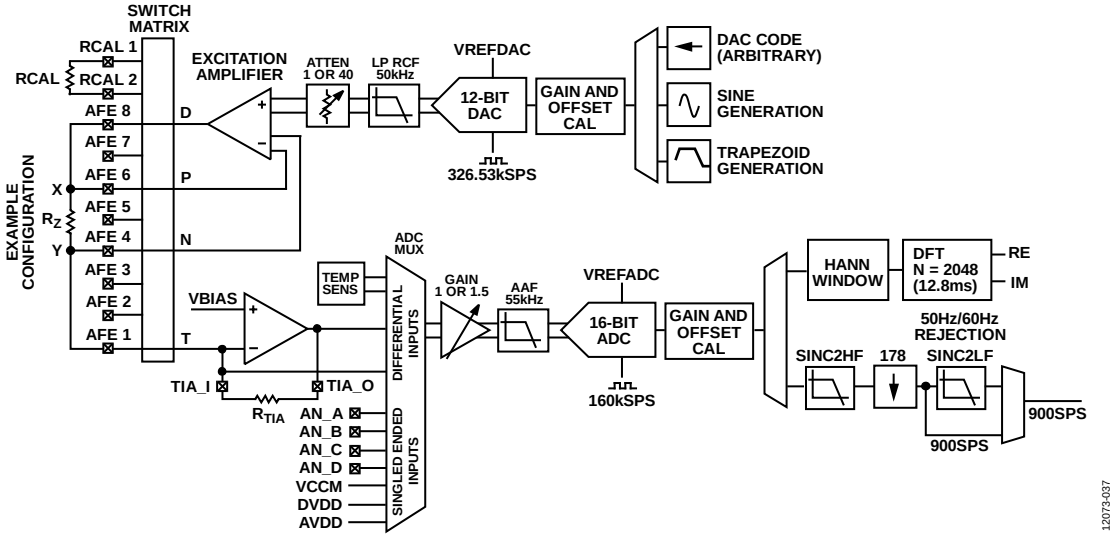

Figure 37. AFE System Block Diagram

For full details on the ADuCM350, refer to the UG-587 hardware reference manual.

The ADuCM350 is a high accuracy, configurable, AFE with a low power, peripheral rich, microcontroller subsystem.

EXCITATION STAGE

The excitation/transmit stage consists of a 12-bit DAC with an excitation buffer and an instrumentation amplifier in a feedback path to the DAC, which forces an accurate voltage across the impedance to be measured, thereby removing parasitics from the measurement system.

All measurements are referenced to a precision external resistor, which is used in the internal calibration loop to ensure no dc bias across an unknown impedance.

A large range of impedances can be measured, depending on the application. Users can optimize the calibration resistor (RCAL), ac amplitude of the excitation waveform, and the current-to-voltage (IV) resistor to tailor fit the system to the application demands. Impedances can be measured from 80 Hz to ~75 kHz.

The switch matrix offers the user full configurability with 34 user selectable switches. The current carrying switches on both excitation buffer output and the transimpedance input are optimally sized for current loads. The switch matrix allows the device to measure and store offset and gain results. The ADuCM350 can self calibrate Rx offset and gain, Tx offset and gain, and switch leakage. This off loads the requirement for an extensive factory calibration routine and removes temperature and aging induced errors from measurements.

MEASUREMENT STAGE

The AFE consists of a multiplexed input, 160 kSPS, 16-bit ADC with four dedicated voltage measurement channels and up to eight multiplexed current measurement channels using the on-chip transimpedance amplifier. The multiplexed channels are filtered and differentially buffered prior to data conversion.

The ADC data can be interrogated using three methods.

- By raw data at 160 kSPS.
- At the output of a 50 Hz/60 Hz filter at 900 SPS.
- Through a discrete Fourier transform (DFT) engine.

The power line filter is optimized for fast settling, just 36.6 ms settling. Data at 900 SPS can be further decimated by the user without requiring additional filtering.

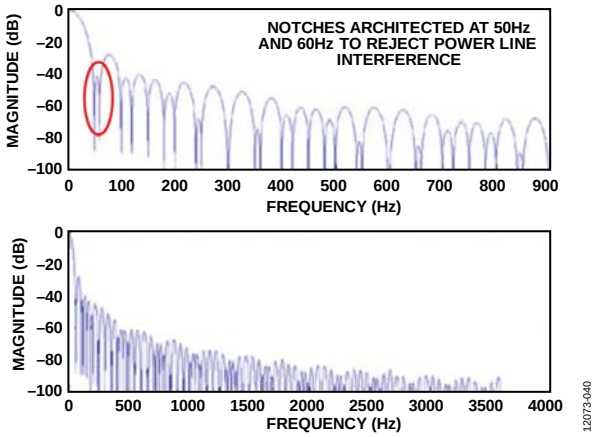

Figure 39. Power Line Rejection Modeling

The DFT engine performs a 2048-point single frequency discrete Fourier transform. It takes the 16-bit ADC output and converts it to complex impedance with real and imaginary components. As the ADC samples at 160 kSPS, this allows for a 79.5 Hz signal energy bandwidth, which gives excellent rejection of interferers.

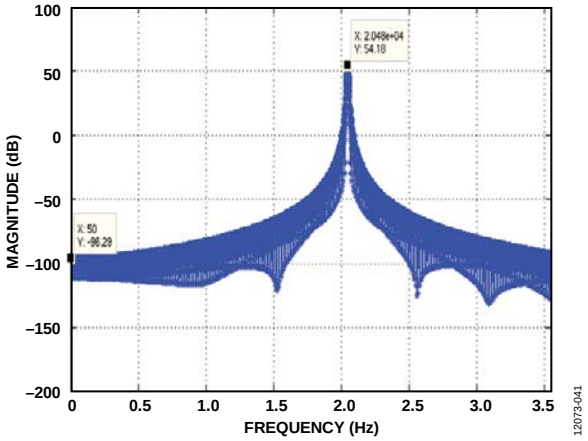

Figure 40. Frequency Response, 2048-Point DFT at 20 kHz

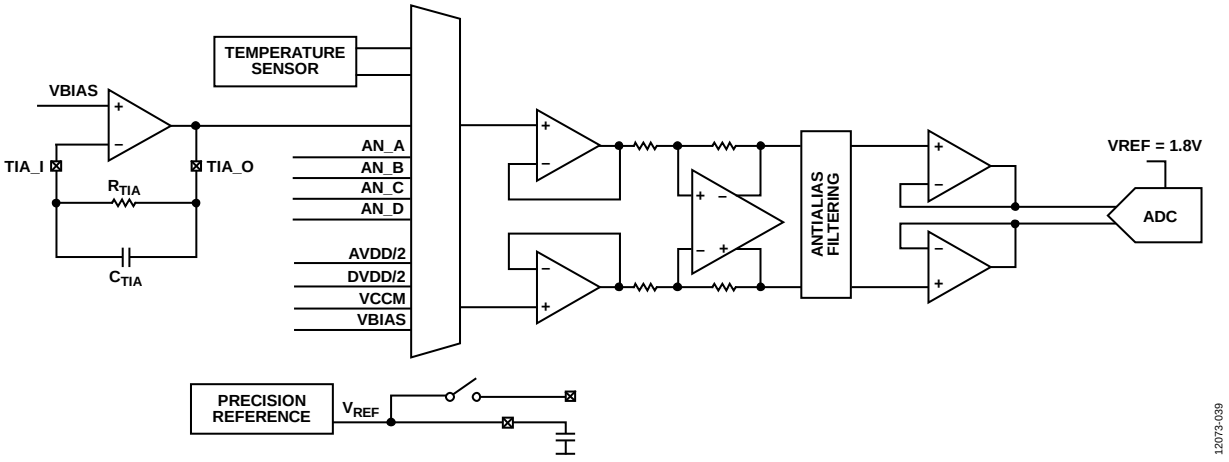

Figure 41. Rx Stage

MICROSUBSYSTEM

MEMORIES

The memory offerings for the ADuCM350 are as follows:

- 384 kB flash.
- 16 kB of flash configured for EEPROM emulation.
- 2 kB user information.
- 32 kB SRAM.
- 2 kB dedicated SRAM for USB endpoint.

Flash

The ADuCM350 includes 384 kB of embedded flash memory, accessed using the flash controller. The flash controller is connected to the bus matrix as a slave device for core and DMA access, as well as the 32-bit AHB for MMR access.

The flash controller supports 384 kB of user space and 2 kB of information space. Read and write to flash are executed via AHB only. The 384 kB flash memory comprises one 256 kB flash array and one 128 kB flash array. The 256 kB flash memory array and 128 kB flash array are controlled by two separate flash controllers with separate register controls.

With respect to flash integrity, the device supports

- Automatic signature check of information space at reset
- User signature for application code
- Parity checking on a per access basis
- 20,000 cycle endurance with 20 ms erase and 20 µs program
- 100-year data retention at room temperature

General-Purpose Flash

The device contains 16 kB of embedded flash memory for general purpose, such as EEPROM emulation.

SRAM

There is 32 kB of SRAM on chip of which 16 kB is retained during hibernate mode and an optional 16 kB can be retained during hibernate for reduced leakage current.

DEBUG CAPABILITY

The ADuCM350 supports two types of debug host interface: 4-wire JTAG debug (JTAG) interface and a serial 2-wire debug (SWD) interface.

The ADuCM350 incorporates the complete embedded trace of the ARM Cortex-M3 features to maximize code analysis, system profiling, and debugging capabilities.

PROGRAMMABLE GPIOS

The ADuCM350 has 66 GPIO pins, most of which have multiple, configurable functions defined by user code. They can be configured as an input/output and have programmable pull-up or pull-down resistors. All I/O pins are functional over the full supply range (VBAT = 1.8 V to 3.6 V).

In power saving mode, GPIO pins retain state; they tristate on reset to prevent any bus irritation. GPIOs of note are as follows:

- 32 pins multiplexed with LCD segment common pins
- Six pins multiplexed with CapTouch
- Nine pins on a dedicated VDDIO for ease of interfacing to peripherals

TIMERS

General-Purpose Timers

ADuCM350 has three identical general-purpose timers, each with a 16-bit count-up/count-down counter. The count-up/count-down counter can be clocked from one of four user selectable clock sources. Any selected clock source can be scaled down using a prescaler of 16, 256, or 32,768.

Watch Dog Timer (WDT)

The watchdog timer is a 16-bit count-down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, 256, or 4096. The watchdog timer is clocked either by the 32 kHz crystal oscillator (LFXTAL) or by the 32 kHz on-chip oscillator (LFOSC).The watchdog timer (WDT) is used to recover from an illegal software state. After the WUT is enabled by user code, it requires periodic servicing to prevent it from forcing a reset or interrupt of the processor. A WDT timeout can generate a reset or an interrupt.

Wake-Up Timer

The wake-up timer (WUT) consists of a 32-bit counter clocked from the 32 kHz external crystal (LFXTAL), 32 kHz internal oscillator (LFOSC), or peripheral clock (PCLK). The selected clock source can be scaled

USB

The USB port on the ADuCM350 is a USB 2.0 full speed compliant port. The module consists of the USB controller, USB PHY, USB RAM, and a 2-channel DMA. An integrated regulator powered by VBUS supplies the USB PHY. A dedicated PLL with 60 MHz clock capability is available for clock generation.

The USB supports bulk, isochronous, interrupt, and control modes. It has seven hardware endpoint and a dedicated 2-channel DMA. It supports suspend and wakeup.

The controller hardware is supplemented by a complete set of USB device class drivers to provide complete USB functionality using a defined Micrium stack. The USB stack has a requirement for an RTOS to be on the system. Analog Devices, Inc., has developed its system using the Micrium µC/OS-II.

Type A and Type B, and 9-bit (Option 1) and 8-bit (Option 3) serial interfaces for Type C.

By using the display controller, the depth on various interfaces is as follows:

- 8-bit interface is 8, 12, or 16 bits per pixel (not 18 or 24).
- 9-bit interface is 18 bits per pixel (not 8, 12, 16, or 24).
- 16-bit interface is 8, 12, or 16 bits per pixel (not 18 or 24).

AUDIO OPTIONS

The ADuCM350 has an integrated audio driver for beeper and an integrated I²S port.

Beeper

The beeper driver module in the ADuCM350 generates a differential square wave of programmable frequency. It drives an external piezoelectric sound component whose two terminals connect to the differential square wave output.

The beeper driver consists of a module that can deliver frequencies from 8 kHz to ~0.25 kHz. It operates on a fixed independent 32 kHz (32,768 Hz) clock source that is unaffected by changes in system clocks.

A timer allows for programmable tone durations from 4 ms to 1.02 sec in 4 ms increments. Single-tone (pulse) and multitone (sequence) modes provide versatile playback options.

In sequence mode, the beeper can be programmed to play any number of tone pairs from 1 to 254 (2 to 508 tones) or be programmed to play forever (until stopped by the user). Interrupts are available to indicate the start or end of any beep, the end of a sequence, or that the sequence is nearing completion.

I²S

The device supports I²S. The purpose of the I²S port is to provide audio data to an amplifier, which drives a small speaker. The I²S features available on the ADuCM350 include the following:

- Data samples of up to 24 bits.
- Frame clocks from 8 kHz to 192 kHz.
- Master/slave mode.
- 8-deep Tx FIFOs.
- DMA mode with address autoincrement.
- Interrupt mode.
- Downsampling transfers.

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

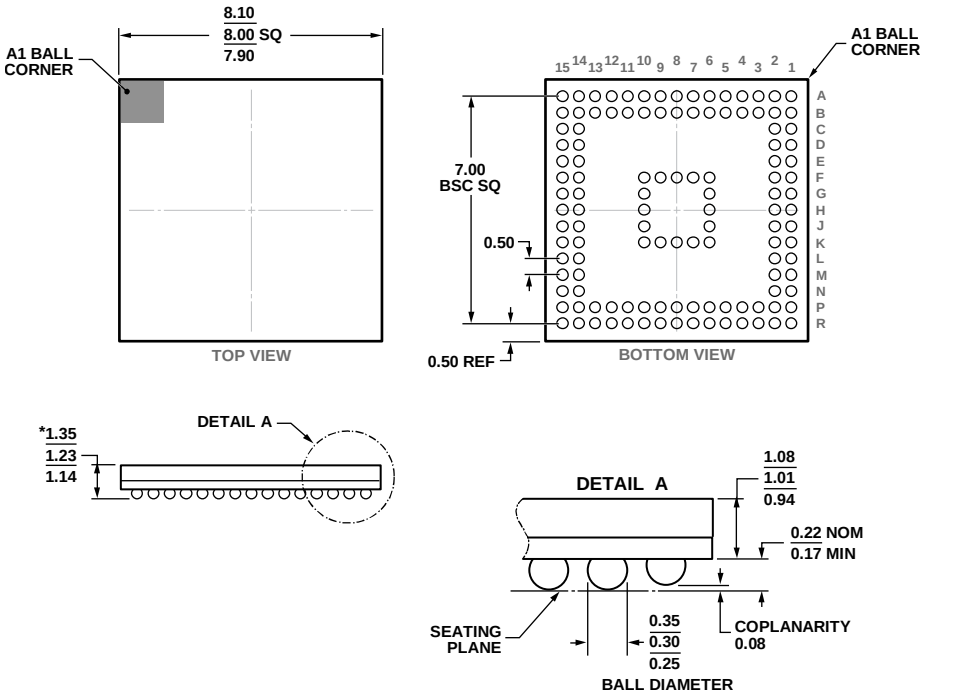

Figure 45. 120-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-120-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADuCM350BBCZ	−40°C to +85°C	120-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-120-3
ADuCM350BBCZ-RL	−40°C to +85°C	120-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-120-3

[1] Z = RoHS Compliant Part.

NOTES