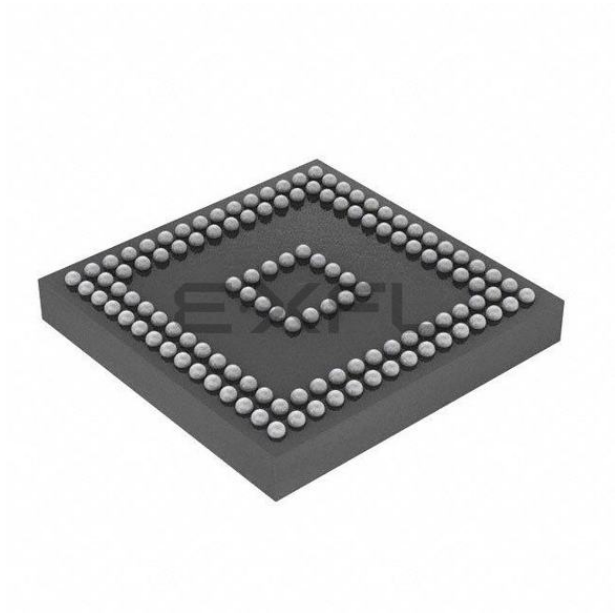

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	DMA, I²S, LCD, POR, WDT
Number of I/O	66
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 3.6V
Data Converters	A/D 12x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	120-LFBGA, CSPBGA
Supplier Device Package	120-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm350bbcz

ADUCM350* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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EVALUATION KITS

- ADuCM350 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1262: ADuCM350 Serial Download Protocol
- AN-1263: Security Integrity of the ADuCM350
- AN-1271: Optimizing the ADuCM350 for Impedance Conversion
- AN-1281: Amperometric/Potentiostat Measurements Using the ADuCM350
- AN-1282: Profiling the ADuCM350 Supply Current in an Example Application
- AN-1286: ADuCM350 Analog Front End Accuracy in a Noisy Digital Environment
- AN-1293: A Quick Guide to the ADuCM350 Sequencer
- AN-1302: Optimizing the ADuCM350 for 4-Wire, Bio-Isolated Impedance Measurement Applications

Data Sheet

- ADuCM350: 16-Bit Precision, Low Power Meter On A Chip with Cortex-M3 and Connectivity Data Sheet

User Guides

- UG-587: ADuCM350 Hardware Reference Manual
- UG-668: EVAL-ADuCM350EBZ User Guide
- UG-677: ADuCM350 Software Development Kit Quick Start Guide

REFERENCE MATERIALS

Technical Articles

- Home is Where the Heart Is

White Papers

- Operating the AD8233 with the ADuCM350

DESIGN RESOURCES

- ADUCM350 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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Visit the product page to see pricing options.

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REVISION HISTORY

5/14—Revision A: Initial Version

GENERAL DESCRIPTION

The ADuCM350 is a complete, coin cell powered, high precision, meter-on-chip for portable device applications for applications such as point-of-care diagnostics and body-worn devices for monitoring vital signs. The ADuCM350 is designed for high precision amperometric, voltametric, and impedometric measurement capabilities.

The ADuCM350 analog front end (AFE) features a 16-bit, precision, 160 kSPS analog-to-digital converter (ADC); 0.17% precision voltage reference; 12-bit, no missing codes digital-to-analog converter (DAC); and a reconfigurable ultralow leakage switch matrix. The ADuCM350 also includes an ARM® Cortex-M3-based processor, memory, and all I/O connectivity to support portable meters with display, USB communication, and active sensors. The ADuCM350 is available in a 120-lead, 8 mm × 8 mm CSP_BGA and operates from −40°C to +85°C.

To support extremely low dynamic and hibernate power management, the ADuCM350 provides a collection of power modes and features, such as dynamic and software controlled clock gating and power gating.

The AFE is connected to the ARM Cortex-M3 via an advanced high performance bus (AHB) slave interface on the advanced microcontroller bus architecture (AMBA) matrix, as well as direct memory access (DMA) and interrupt connections.

SPECIFICATIONS

All characterization is at VCCM = 2.5 V to 3.6 V, specifications below 2.5 V are for functionality only, all minimum and maximum specifications are specified for a temperature range of −40°C to +85°C, unless otherwise noted.

ANALOG FRONT-END SPECIFICATIONS

AFE LDO Specifications

Table 1. AFE LDO Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Output Voltage	1.71	1.8	1.89	V	Measured with a load capacitance (C_{LOAD}) = 0.47 µF; measured with 1 mA load current on AVDD_RX/TX; all AFE blocks powered down
Dropout		150	200	mV	10 mA load applied; no AFE blocks enabled
REGULATION					
Line		1080		µV/V	10 mA load applied
Load		0.65		mV/mA	10 mA load applied
POWER UP					
Power-Up Time		500		µs	Measured with a C_{LOAD} = 0.47 µF; current limit enabled

High Precision Internal Reference Specifications

Table 2. High Precision Internal Reference Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC V_{REF}					
Reference Voltage Initial Accuracy[1]	1.797	1.8	1.803	V	For a temperature range of 0°C to 50°C
	1.79	1.8	1.803	V	For a temperature range of −40°C to +85°C
Output Impedance			570	mΩ	LDO and reference enabled; all other AFE blocks disabled; reference loaded with 50 µA on VREF
Temperature Coefficient[2]	−52		+90	ppm/°C	For a temperature range of −40°C to +85°C, maximum value from −40°C to +25°C, and from +25°C to +85°C specified
	−45		+48	ppm/°C	For a temperature range of 0°C to 50°C, maximum value from −40°C to +25°C, and from 25°C to 85°C specified
VREF Thermal Hysteresis		50		ppm	
REF_EXCITE Switching Load	1.789	1.793	1.797	V	I_{LOAD} = 200 µA; internal ADC measurement
Line Regulation		50		µV/V	V_{CCM1} = 2.5 V, V_{CCM2} = 3.6 V; reference loaded with 300 µA
Short-Circuit Current to Ground		10		mA	Current limit off
DAC V_{REF}					
Reference Voltage	1.77	1.8	1.83	V	
VBIAS					
VBIAS Voltage	1.095	1.1	1.102	V	Measured with a C_{LOAD} = 0.47 µF; no current load

[1] Reference voltage is trimmed unloaded. Measured with C_{LOAD} = 4.7 µF. Measured at 25°C.
[2] Guaranteed by design and/or characterization.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ON LEAKAGE[2]					
T, N, and P Switches		530		pA	Sum value for 25 switches, including NL
D Switches		340		pA	Sum value for eight switches

[1] R_{ON} characterized with a voltage sweep from 0 V to VCCM. Production tested at 1.8 V.
[2] See Figure 38 as a reference. The AFE x pin is driven to 0.2 V.

TRANSIMPEDANCE AMPLIFIER SPECIFICATIONS

Table 5. Transimpedance Amplifier Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSIMPEDANCE AMPLIFIER					
Maximum Current Sink/Source		±5		mA	Ensure an R_{TIA} selection to generate ±750 mV swing for optimal linearity performance
Short-Circuit Protection Functionality		10		mA	

ADC SPECIFICATIONS

Table 6. ADC Specifications[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
Input Range	0.35		1.85	V	Internal reference
No Missing Codes		16		Bits	
DNL		±0.9		LSB	
INL		±0.7		LSB	@ 160 kSPS with respect to an optimal voltage range of ±750 mV, from 0°C to 50°C
		±1		LSB	@ 160 kSPS with respect to an optimal voltage range of ±750 mV, from −40°C to +85°C
Sample Rate After Decimation		160		kSPS	
3 dB Bandwidth		54		kHz	

[1] R_{TIA} = 7.5 kΩ, C_{TIA} = 220 pF; ±100 µA current measurement.

TEMPERATURE SENSOR SPECIFICATIONS

Table 7. Temperature Sensor Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					
Accuracy		±1		°C	0°C to 50°C, trimmed at 25°C
		±2		°C	−40°C to +85°C, trimmed at +25°C

CapTouch

Table 8. CapTouch Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CapTouch™ CHARACTERISTICS					
Core Resolution		14		Bits	
Core SNR	60			dB	1 kHz test tone, input range of ADC = 1.8 V
CAPT_x		±10		nA	GPIO leakage test
Update Rate	7.5		1E6	µs	Programmable, dependent on configuration
Update Rate per Sensor	7.5			µs	No filtering enabled, clock = 16 MHz
CAPT_x Input Range		±8		pF	ΔC_{IN} is register programmable from 0.5 pF to 9.3 pF
CAPT_x Offset (CapDAC) Range		75		pF	

Flash/General-Purpose Flash

Table 12. Flash/General-Purpose Flash Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FLASH/GP FLASH					
Endurance[1]	20,000			Cycles	
Erase Time		20		ms	@ 1.8 V
Program Time		20		µs	@ 1.8 V
Data Retention[2]		100		Years	Below room temperature

[1] Endurance is qualified to 10,000 cycles as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.

Digital Inputs/Outputs: Specified

Specified pin supply range from 2.5 V to 3.6 V.

Table 13. Digital Inputs and Outputs[1] Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PIN SUPPLY	2.5	3	3.6	V	
Impedance					
Pull-Down		20		kΩ	I_{SINK} < 10 µA
Pull-Up		15		kΩ	I_{SOURCE} < 10 µA
Internal Pull-Up/Pull-Down Enabled Leakage[2]		200		µA	
Digital I/O Leakage Current		.01	1	µA	
Input Capacitance		10		pF	
Input Voltage					
Low (V_{INL})			0.3 × pin supply	V	
High (V_{INH})	0.7 × pin supply			V	
Output Voltage					
Low (V_{OL})			0.4	V	I_{SINK} = 1.0 mA
V_{OL} High Drive		0.4		V	I_{SINK} = 1.6 mA
High (V_{OH})[3]	Pin supply − 0.4			V	I_{SOURCE} = 1.0 mA
V_{OH} High Drive		2.4		V	I_{SOURCE} = 1.6 mA

[1] Includes GPIO, debug, SPI, I²C, PDI, LCD, I²S, and beeper.
[2] See Table 35 for details regarding bumps/pins that have pull-up resistors.
[3] I²C does not drive out a high voltage; it uses external pull-up resistors.

Digital Inputs/Outputs: Functional

Functional pin supply range from 1.65 V to 2.5 V.

Table 14. Digital Inputs/Outputs: Functional Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PIN SUPPLY	1.65		2.5	V	
Input Voltage					
Low (V_{INL})		0.3 × pin supply		V	
High (V_{INH})		0.7 × pin supply		V	
Output Voltage					
Low (V_{OL})		0.45		V	I_{SINK} = 1.0 mA
High (V_{OH})[1]		Pin supply − 0.5		V	I_{SOURCE} = 1.0 mA

[1] I²C does not drive out a high voltage; it uses external pull-up resistors.

Universal Serial Bus Regulator Specifications

Table 15. Universal Serial Bus Regulator Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS REGULATOR					
Input Voltage Range	3.6		5.25	V	
Regulated Output Voltage	3.2		3.4	V	
Dropout		440		mV	40 mA continuous current
Regulation					
Line		0.0043		%/V	4.5 V to 5.5 V
Load		0.0093		%/mA	@ 5 V, 220 nF ceramic decoupling capacitor
Power-Up Time		37		µs	

Universal Serial Bus DC Specifications

Table 16. Universal Serial Bus DC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER					
Single-Ended Input Voltage (Driven)					
High	2.0			V	
Low			0.8	V	
Differential Receiver Input					
Common Mode	0.8		2.5	V	
Sensitivity	0.2			V	V(USB DP) – V(USB DM)
TRANSMITTER					
Output Voltage					
Low (V_{OL})	0		0.3	V	Pull-up resistor asserted on the USB pin, USB DP, R_{PU} to AVDD
High (V_{OH})	2.8		3.6	V	Pull-down resistor asserted on USB DP and USB DM (15 kΩ to GND)
Driver Output Impedance	28		44	Ω	R_{DRIVER} + R_{SERIES}
Term Series Resistor		40		Ω	
Pull-Up Resistor (D+ High)	1.425	1.5	3.095	kΩ	Termination voltage = USB regulator voltage
Pull-Up Resistor (D+ Low)	0.9		1.575	kΩ	Termination voltage = USB regulator voltage
Pull-Down Resistors	14.25	15	24.8	kΩ	

Universal Serial Bus AC Specifications

Meeting USB 2.0 compliance electrical tests.

Table 17. Universal Serial Bus AC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FULL SPEED DRIVER TIMING					C_{LOAD} = 50 pF
Signaling Rate	11.988	12		MHz	
Output Time					
Rise	4		20	ns	V_{OH} – V_{OL} (10% to 90%), C_{LOAD} = 50 pF
Fall	4		20	ns	V_{OH} – V_{OL} (10% to 90%), C_{LOAD} = 50 pF
Rise and Fall Matching	90		111.1	%	Exclude transition from idle
Output Voltage Crossover	1.3		2.0	V	Exclude transition from idle
FULL SPEED JITTER					C_{LOAD} = 50 pF
Driver Jitter Generated	−2		+2	ns	Next transitions
	−1		+1	ns	Paired transitions
Load Capacitance			50	pF	Testing slew rate

LCD, Charge Pump

Table 18. LCD, Charge Pump Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCE					
Reservoir Capacitance Between VLCDVDD and VLCD_GND	0.47	1		µF	
Flying Capacitance	2.2		4.7	nF	Between VLCD FLY1 and VLCD FLY2
VLCD					
Switching Voltage					
VLCD FLY1	−0.7		VLCD + 0.2	V	Top of flying capacitor
VLCD FLY2	0		VCCM	V	Bottom of flying capacitor
VLCD Charge Pump Switching Frequency		32		kHz	
Minimum VLCD with Respect to VCCM_ANA and VCCM_DIG	2.1			V	When <2.1 V after 62.5 ms elapses indicates fault condition
VLCDVDD					
VLCDVDD Voltage Range	2.4		3.65	V	5-bit programmable in steps of 40 mV
VLCDVDD Pin Leakage		3		nA	To VCCM
		0.2		nA	To GND
VLCDVDD Start-Up Time		5		ms	VLCDVDD = 0 V to 3.6 V, reservoir = 1 µF, flying capacitor = 2.2 nF (minimum) and 4.7 nF (maximum)
VLCDVDD Line Regulation		0.32		%	
V_LCD_xx VOLTAGE RANGE					
V_LCD_13 Voltage Range	VLCD ÷ 3 − 10		VLCD ÷ 3 + 10	mV	
V_LCD_23 Voltage Range	2/3 VLCD − 13		2/3 VLCD + 13	mV	
COMx PINS					
DC Voltage Across Segment and COMx Pins			50	mV	
PIN OUTPUT IMPEDANCE					
Segment		2000		Ω	
Common		130		Ω	

SYSTEM CLOCKS/TIMERS

The following tables document the system clock specifications in the ADuCM350.

Platform External Crystal Oscillator

Table 19. Platform External Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOW FREQUENCY					
$C_{EXT}1 = C_{EXT}2$	12	15	18	pF	External capacitor, C1 = C2 (symmetrical load)
Frequency		32,768		Hz	
HIGH FREQUENCY					
$C_{EXT}1 = C_{EXT}2$	10	12	15	pF	External capacitor
Frequency		8 or 16		MHz	

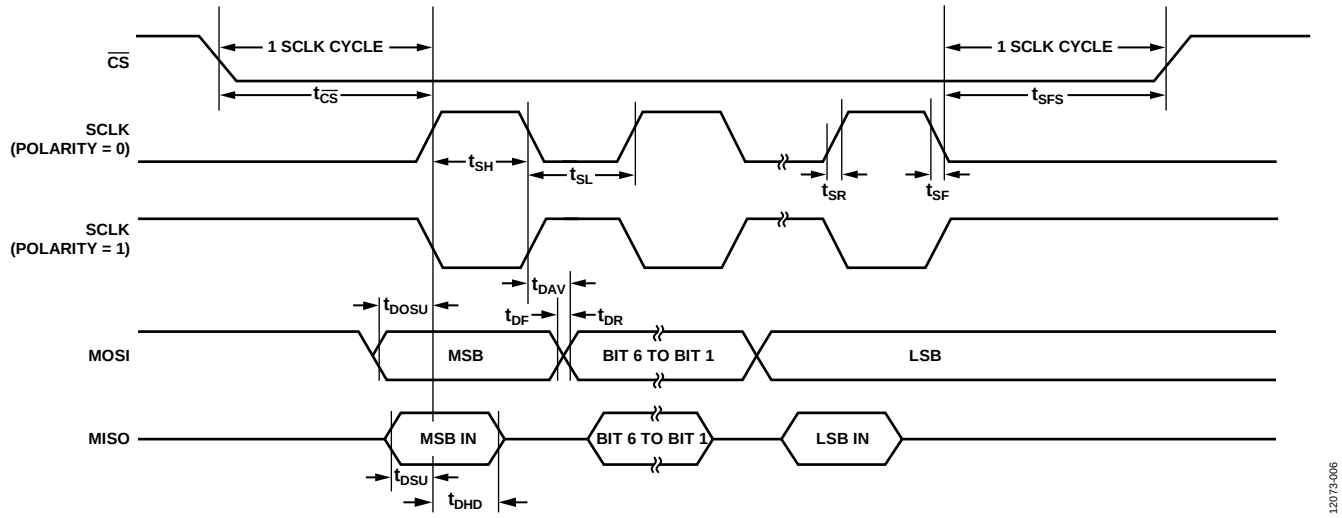

Figure 6. SPI Master Mode Timing (Phase Mode = 0)

Table 32. SPI Slave Mode Timing

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	38			ns
t_{SL}	SCLK low pulse width[1]		(SPIXDIV[5:0] + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]	62.5	(SPIDIV[5:0] + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			49.1	ns
t_{DSU}	Data input setup time before SCLK edge	20.2			ns
t_{DHD}	Data input hold time after SCLK edge	10.1			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK rise time		12	35.5	ns
t_{SF}	SCLK fall time		12	35.5	ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			25	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 62.5 ns. It corresponds to the maximum internal clock frequency before clock dividers.

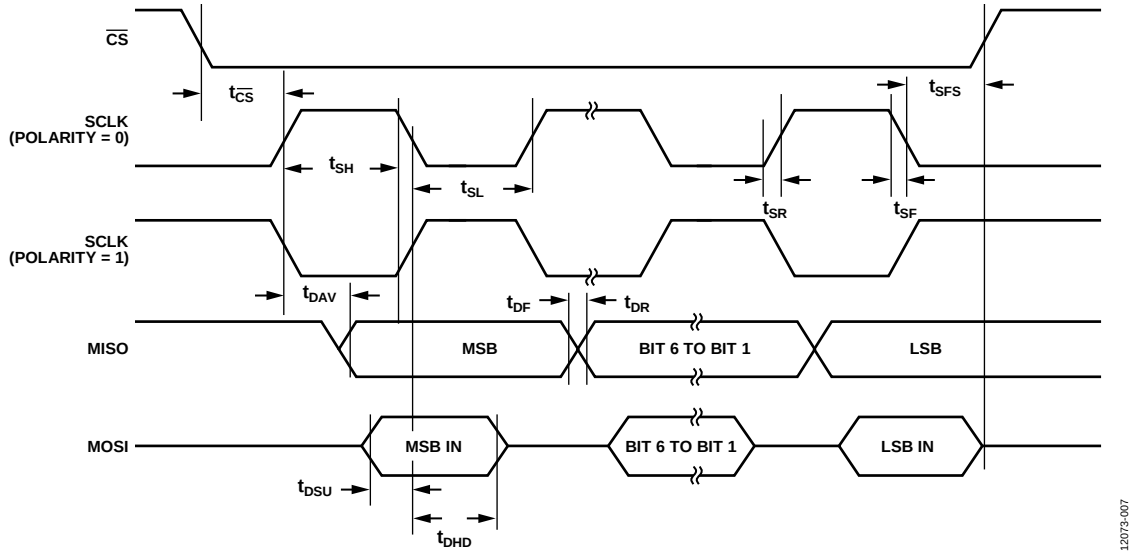

Figure 7. SPI Slave Mode Timing (Phase Mode = 1)

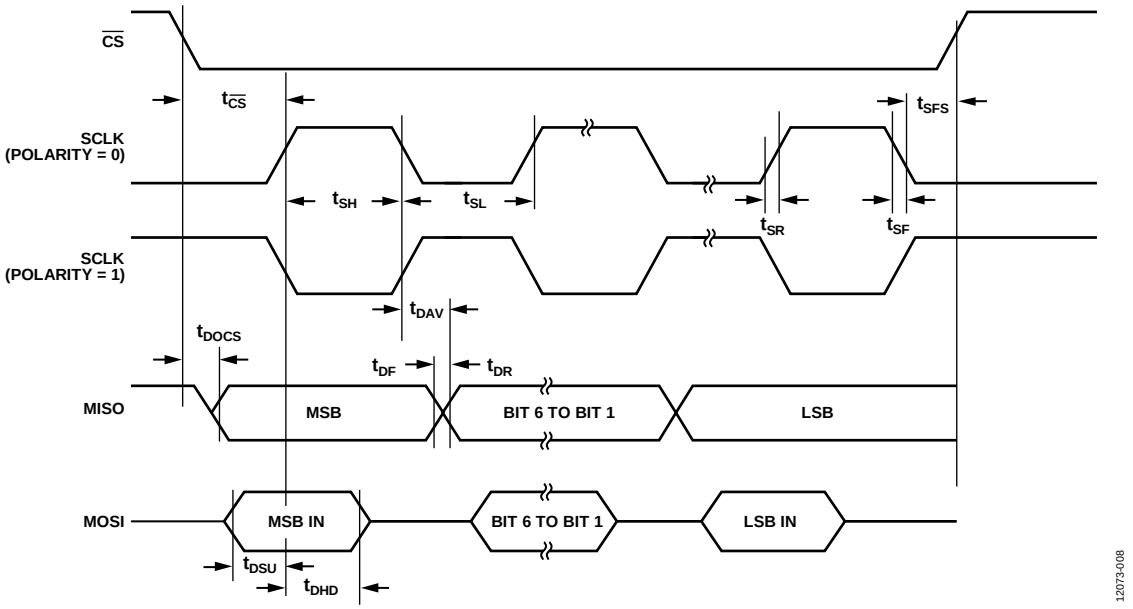

Figure 8. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 33.

Parameter	Rating
Supplies	
VCCM_ANA, VCCM_DIG, VLCDVDD, VDD_IO, VBACK to AGND_x/DGNDx	−0.3 V to +3.6 V
Decoupling	
DVDD, AVDD_RX/TX, VBIAS, VREF, VUSB	−0.3 V to +2.0 V
Digital Input/Output	
P0.x, P1.x, P2.x, P3.x, P4.x, BOOT, RESETX	−0.3 V to +3.6 V
TRACEx	−0.3 V to +3.6 V
Switch Matrix (RCAL 1, RCAL 2, AFE x)	−0.3 V to +3.6 V
TIA (TIA_I, TIA_O)	−0.3 V to +3.6 V
Analog Inputs (AN_x)	−0.3 V to +3.6 V
REF_EXCITE	−0.3 V to +1.98 V
VLCD FLY1, VLCD FLY2	−0.3 V to +3.6 V
V_LCD_13, V_LCD_23	−0.3 V to +3.6 V
VBUS to DGND	−0.3 V to +5.25 V
USB DM, USB DP to DGND	−0.3 V to +3.6 V
HF_XTALx, LF_XTALx	−0.3 V to +1.98 V
Analog Ground to Digital Ground	
AGND CTOUCH, AGND_RX/TX, AGND_REF to DGND, DGND1, DGND2, DGND USB	−0.3 V to +0.3 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages; assumes use of a JEDEC 4-layer board.

Table 34. Thermal Resistance

Package Type	θ_{JA}	Unit
CSP_BGA	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
B2	P2.0/COM0	I/O	VLCD VDD	Pull-up	GPIO/Common Output 0 for LCD Back Plane (COM 0). This is a dual function pin.
A2	P2.1/COM1/RESX	I/O	VLCD VDD	Pull-up	GPIO/COM 1/Parallel Display Interface (PDI) Reset. This is a multifunction pin.
B3	P2.2/COM2/CSX	I/O	VLCD VDD	Pull-up	GPIO/COM 2/PDI Chip Select. This is a multifunction pin.
A3	P2.3/COM3/DCX	I/O	VLCD VDD	Pull-up	GPIO/COM 3/PDI Data Select. This is a multifunction pin.
B4	P2.4/S1/RWX-RDX	I/O	VLCD VDD	Pull-up	GPIO/Segment Driver 1 (SEG 1)/PDI R/WX or RDX. This is a multifunction pin.
A4	P2.5/S2/ECLOCK-WRX	I/O	VLCD VDD	Pull-up	GPIO/SEG 2/PDI E Clock Output (Motorola Bus Mode) or PD Write Select (Intel® Bus Mode). This is a multifunction pin.
A5	P1.0/S3/D0/SCL	I/O	VLCD VDD	Pull-down	GPIO/SEG 3/PDI D0/PDI Serial Port Clock. This is a multifunction pin.
B5	P1.1/S4/D1/DOUT	I/O	VLCD VDD	Pull-down	GPIO/SEG 4/PDI D1/PDI Serial Port Data Output. This is a multifunction pin.
A6	P1.2/S5/D2/DIN	I/O	VLCD VDD	Pull-down	GPIO/SEG 5/PDI D2/PDI Serial Port Data Input. This is a multifunction pin.
B6	P1.3/S6/D3	I/O	VLCD VDD	Pull-down	GPIO/SEG 6/PDI D3. This is a multifunction pin.
A7	P1.4/S7/D4	I/O	VLCD VDD	Pull-down	GPIO/SEG 7/PDI D4. This is a multifunction pin.
B7	P1.5/S8/D5	I/O	VLCD VDD	Pull-down	GPIO/SEG 8/PDI D5. This is a multifunction pin.
A8	P1.6/S9/D6	I/O	VLCD VDD	Pull-down	GPIO/SEG 9/PDI D6. This is a multifunction pin.
B8	P1.7/S10/D7	I/O	VLCD VDD	Pull-down	GPIO/SEG 10/PDI D7/System Clock Output. This is a multifunction pin.
A9	P1.8/S11/D8	I/O	VLCD VDD	Pull-down	GPIO/SEG 11/PDI D8. This is a multifunction pin.
B9	P1.9/S12/D9	I/O	VLCD VDD	Pull-down	GPIO/SEG 12/ PDI D9. This is a multifunction pin.
A10	P1.10/S13/D10	I/O	VLCD VDD	Pull-down	GPIO/SEG 13/PDI D10. This is a multifunction pin.
B10	P1.11/S14/D11	I/O	VLCD VDD	Pull-down	GPIO/SEG 14/PDI D11. This is a multifunction pin.
A11	P1.12/S15/D12	I/O	VLCD VDD	Pull-down	GPIO/SEG 15/PDI D12. This is a multifunction pin.
B11	P1.13/S16/D13	I/O	VLCD VDD	Pull-down	GPIO/SEG 16/PDI D13. This is a multifunction pin.
A12	P1.14/S17/D14	I/O	VLCD VDD	Pull-down	GPIO/SEG 17/PDI D14. This is a multifunction pin.
B12	P1.15/S18/D15	I/O	VLCD VDD	Pull-down	GPIO/SEG 18/PDI D15. This is a multifunction pin.
D15	P2.6/S19/TE	I/O	VLCD VDD	Pull-down	GPIO/SEG 19/TE. This is a multifunction pin.
C15	P2.7/S20/TOUTA	I/O	VLCD VDD	Pull-down	GPIO/SEG 20/Timer A Output. This is a multi-function pin.
B15	P2.8/S21	I/O	VLCD VDD	Pull-down	GPIO/SEG 21. This is a dual function pin.
A14	P2.9/S22	I/O	VLCD VDD	Pull-down	GPIO/SEG 22. This is a dual function pin.
A13	P2.10/S23	I/O	VLCD VDD	Pull-down	GPIO/SEG 23. This is a dual function pin.
B13	P2.11/S24	I/O	VLCD VDD	Pull-down	GPIO/SEG 24. This is a dual function pin.
B14	P2.12/S25	I/O	VLCD VDD	Pull-up	GPIO/SEG 25. This is a dual function pin.
D14	P2.13/S26	I/O	VLCD VDD	Pull-up	GPIO/SEG 26. This is a dual function pin.
E15	P2.14/S27	I/O	VLCD VDD	Pull-up	GPIO/SEG 27. This is a dual function pin.
A15	P2.15/S28	I/O	VLCD VDD	Pull-up	GPIO/SEG 28. This is a dual function pin.
F8	P3.8/S29	I/O	VLCD VDD	Pull-up	GPIO/SEG 29. This is a dual function pin.
F9	P3.9/S30	I/O	VLCD VDD	Pull-up	GPIO/SEG 30. This is a dual function pin.
C14	P3.10/S31	I/O	VLCD VDD	Pull-up	GPIO/SEG 31. This is a dual function pin.
E14	P3.11/S32	I/O	VLCD VDD	Pull-up	GPIO/SEG 32. This is a dual function pin.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
Miscellaneous Digital Input/Output					
K8	RESETX	I	VCCM_DIG	Pull-up	Reset Pin (Active Low).
L1	P4.0/I2CSCL	I/O	VCCM_DIG	Pull-up	GPIO (External Interrupt 0)/I²C Clock. This is a dual function pin.
L2	P4.1/I2CSD	I/O	VCCM_DIG	Pull-up	GPIO/I²C Data. This is a dual function pin.
R1	P4.2/TOUTB	I/O	VCCM_DIG	Pull-up	GPIO/Timer B Output. This is a dual function pin.
R2	P0.10/TOUTC	I/O	VCCM_DIG	Pull-up	GPIO (External Interrupt 8)/Timer C Output. This is a dual function pin.
K2	P0.11	I/O	VCCM_DIG	Pull-up	GPIO (External Clock Input Pin).
N2	BOOT	I	VCCM_DIG	Pull-down	The device enters serial download mode if this pin is held high during, and for a short time after, a reset. It executes user code after any reset event or if the pin is low.
A1	DNC		N/A	N/A	Do Not Connect. Leave this pin floating.
Audio					
K6	P3.12/BEEP/BMCLK	I/O	VCCM_DIG	Pull-down	GPIO/Beeper Output Positive/I²S Bit Clock. This is a multifunction pin.
K7	P3.13/BEEPX/SDATA	I/O	VCCM_DIG	Pull-down	GPIO/Beeper Output Negative/I²S Serial Data Output. This is a multifunction pin.
J6	P3.14/LRCLK	I/O	VCCM_DIG	Pull-down	GPIO/I²S Frame Clock. This is a dual function pin.

[1] S is supply, A is analog input, I is digital input, O is digital output, I/O is digital input/output, and G is ground.
[2] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

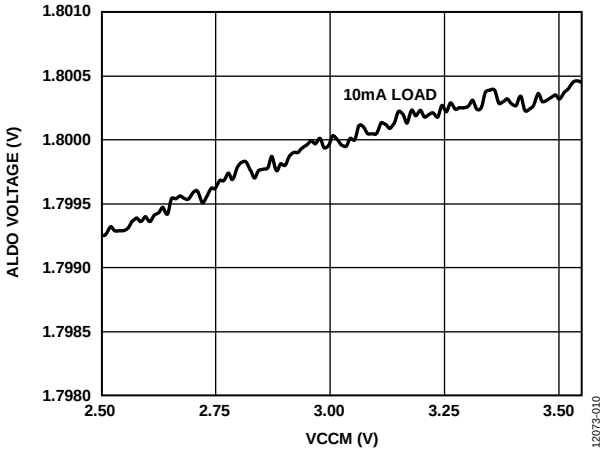

Figure 10. ALDO Line Regulation

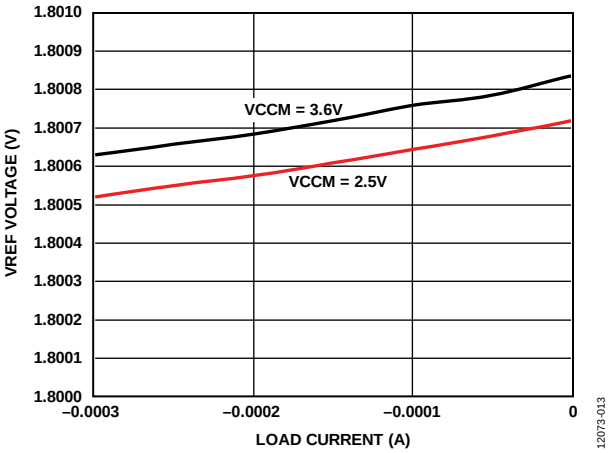

Figure 13. VREF Load Regulation

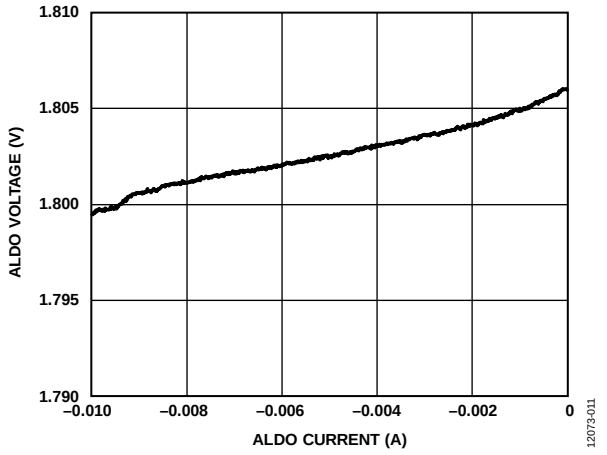

Figure 11. ALDO Load Regulation

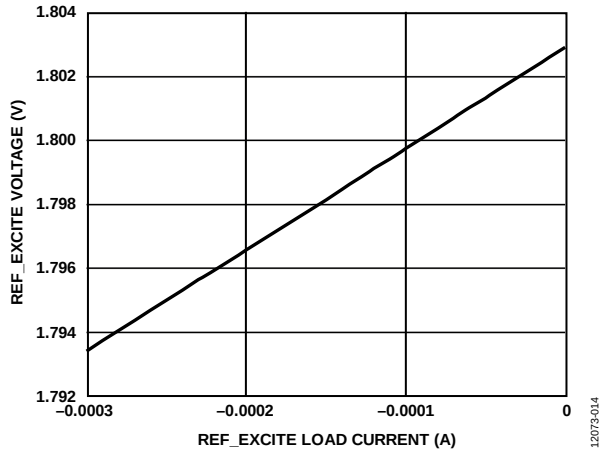

Figure 14. REF_EXCITE Load Regulation

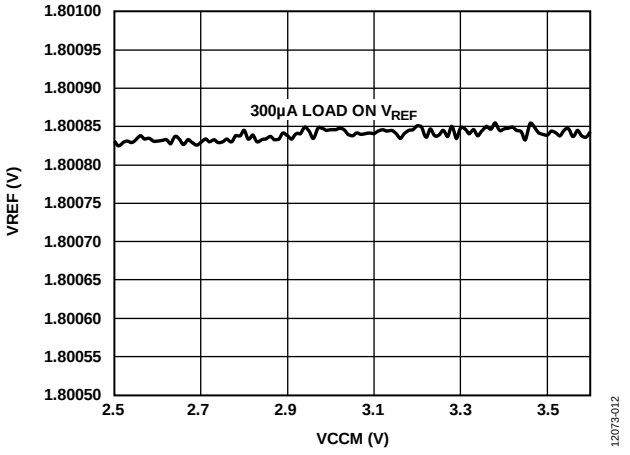

Figure 12. VREF Line Regulation

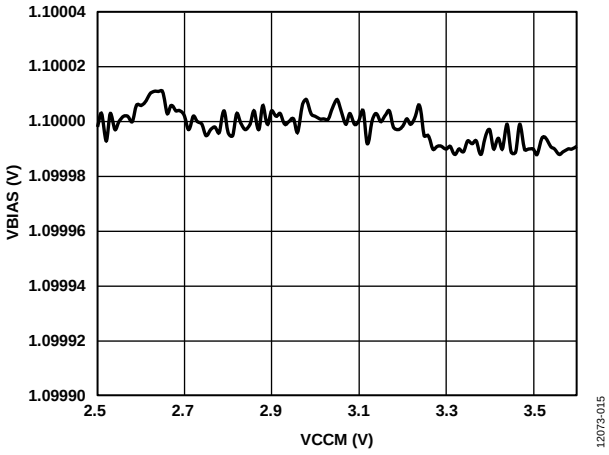

Figure 15. VBIAS Line Regulation

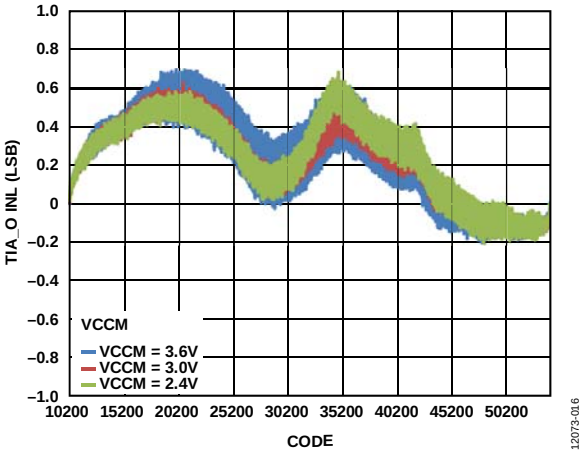

Figure 16. ADC TIA_O INL (16-Bit) vs. Code (±150 µA)

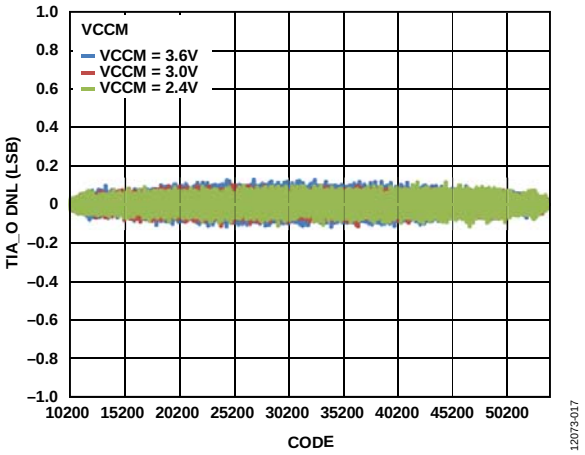

Figure 17. ADC ADC TIA_O DNL (16-Bit) vs. Code

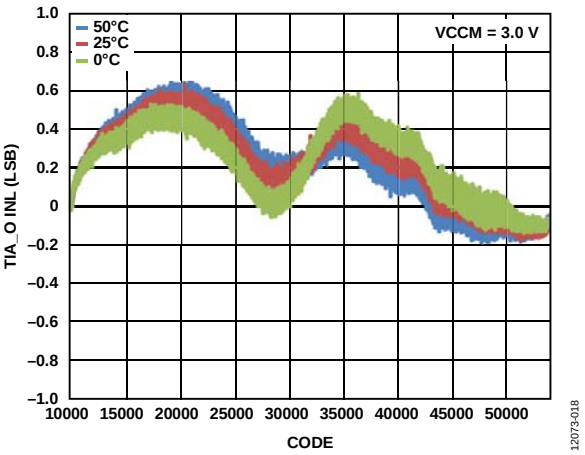

Figure 18. ADC ADC TIA_O INL (16-Bit) vs. Code (Temperature)

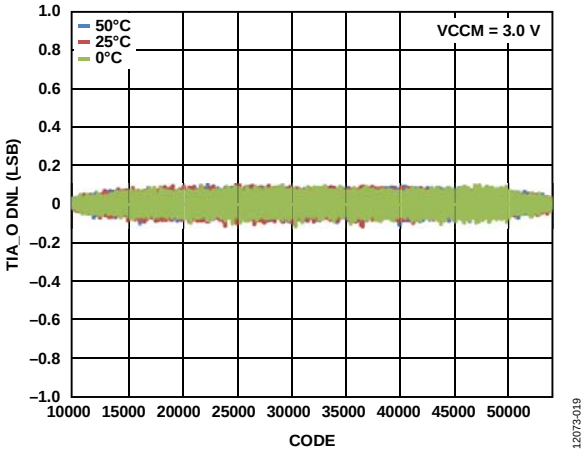

Figure 19. ADC TIA_O DNL (16-Bit) vs. Code (Temperature)

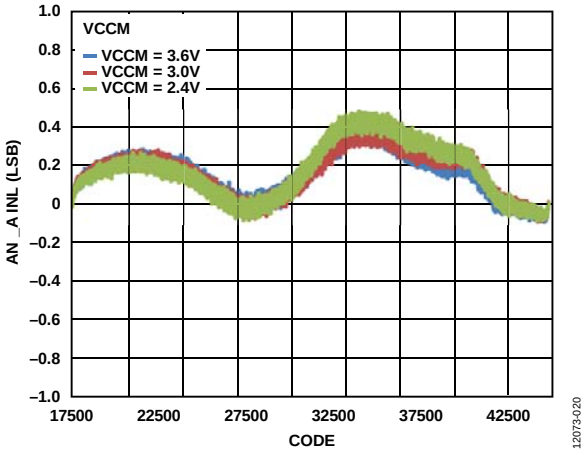

Figure 20. ADC AN_A INL (16-Bit) vs. Code

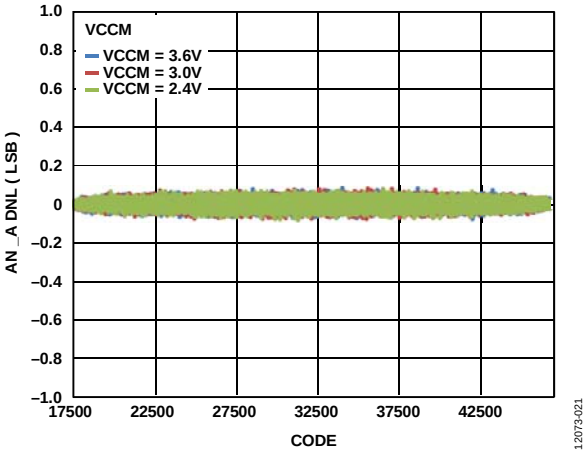

Figure 21. ADC AN_A DNL (16-Bit) vs. Code

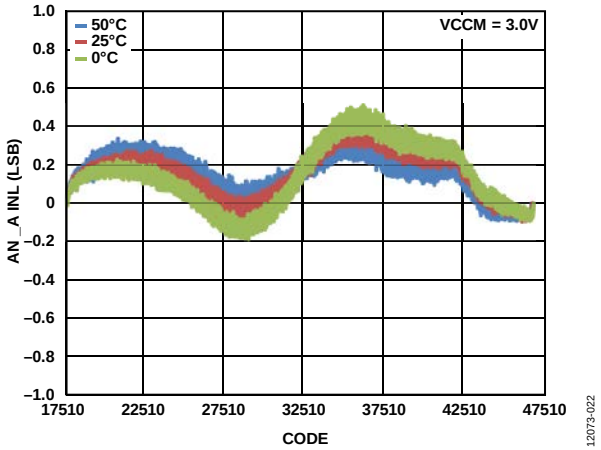

Figure 22. ADC AN_A INL (16-Bit) vs. Code (Temperature)

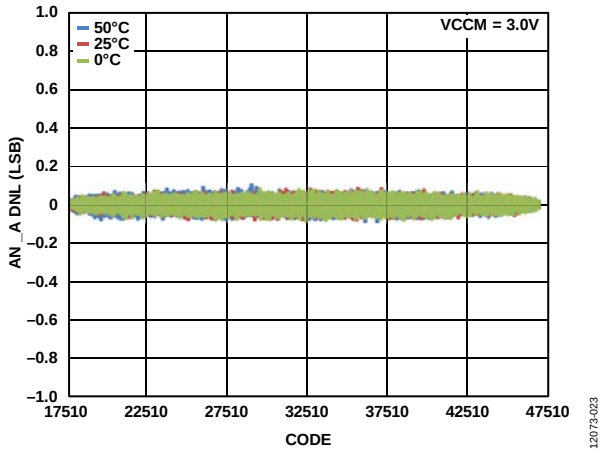

Figure 23. ADC AN_A DNL (16-Bit) vs. Code (Temperature)

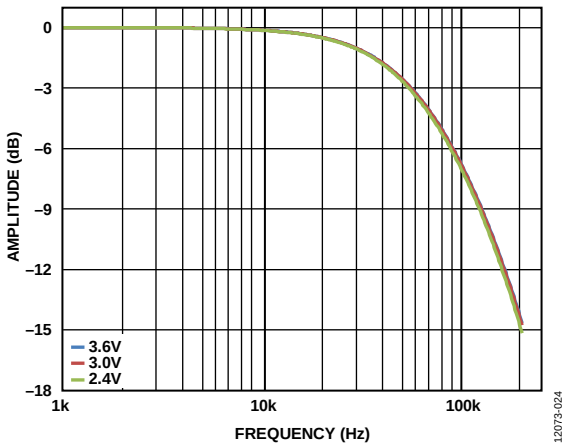

Figure 24. Receive Channel Antialias Filter Roll-Off

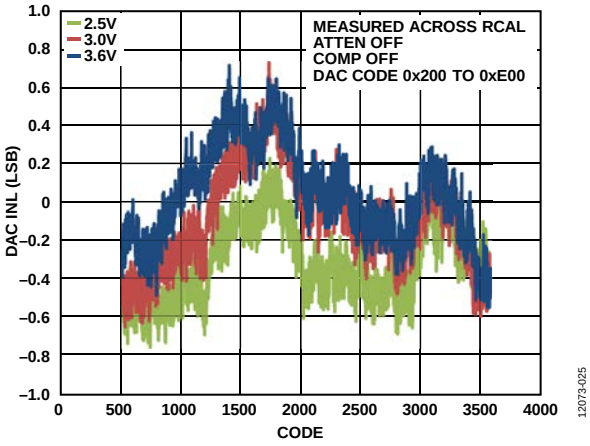

Figure 25. DAC INL (12-Bit) vs. Code

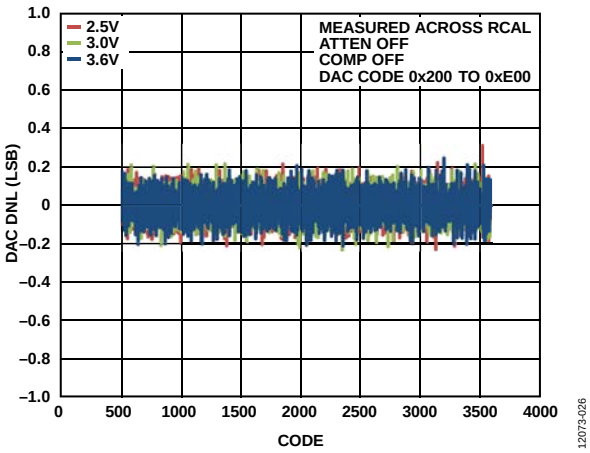

Figure 26. DAC DNL (12-Bit) vs. Code

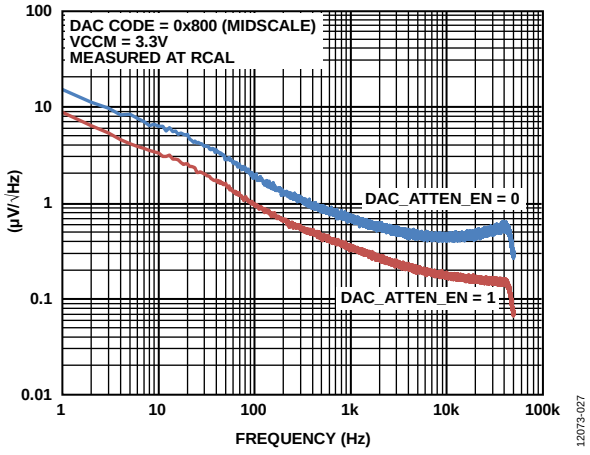

Figure 27. Noise Spectral Density

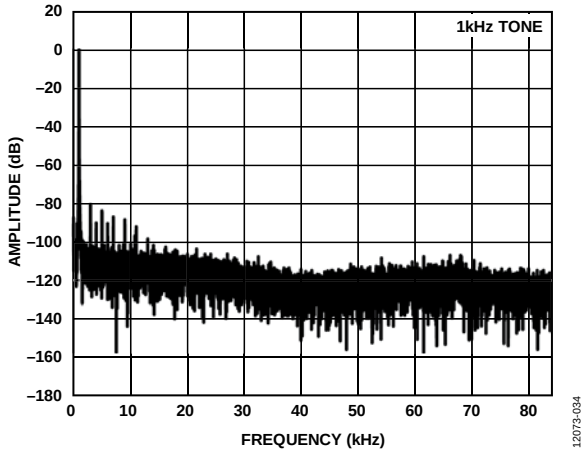

Figure 34. CapTouch SNR

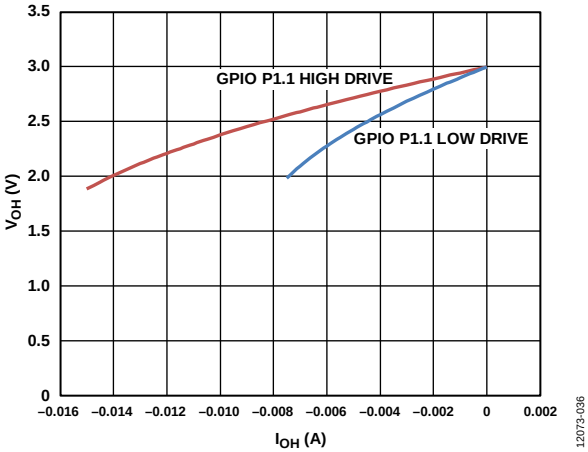

Figure 36. GPIO V_{OH} vs. I_{OH}

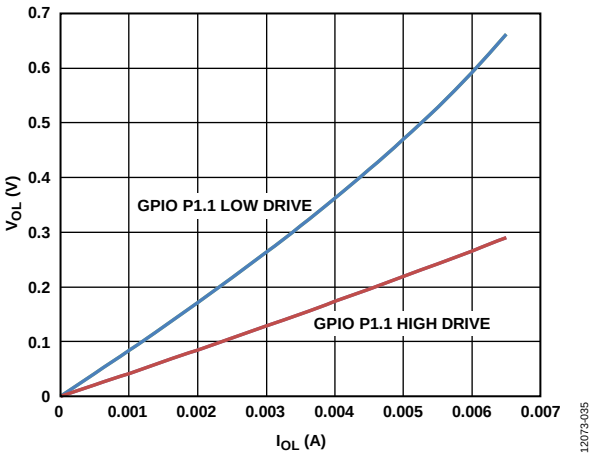

Figure 35. GPIO V_{OL} vs. I_{OL}

MEASUREMENT STAGE

The AFE consists of a multiplexed input, 160 kSPS, 16-bit ADC with four dedicated voltage measurement channels and up to eight multiplexed current measurement channels using the on-chip transimpedance amplifier. The multiplexed channels are filtered and differentially buffered prior to data conversion.

The ADC data can be interrogated using three methods.

- By raw data at 160 kSPS.
- At the output of a 50 Hz/60 Hz filter at 900 SPS.
- Through a discrete Fourier transform (DFT) engine.

The power line filter is optimized for fast settling, just 36.6 ms settling. Data at 900 SPS can be further decimated by the user without requiring additional filtering.

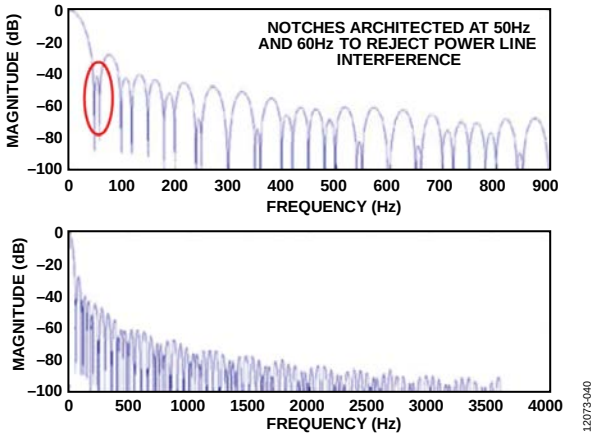

Figure 39. Power Line Rejection Modeling

The DFT engine performs a 2048-point single frequency discrete Fourier transform. It takes the 16-bit ADC output and converts it to complex impedance with real and imaginary components. As the ADC samples at 160 kSPS, this allows for a 79.5 Hz signal energy bandwidth, which gives excellent rejection of interferers.

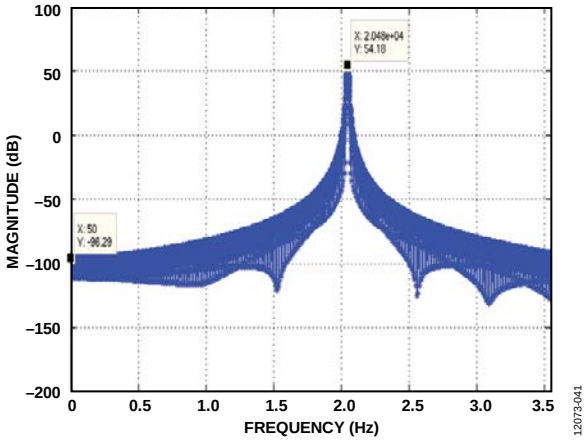

Figure 40. Frequency Response, 2048-Point DFT at 20 kHz

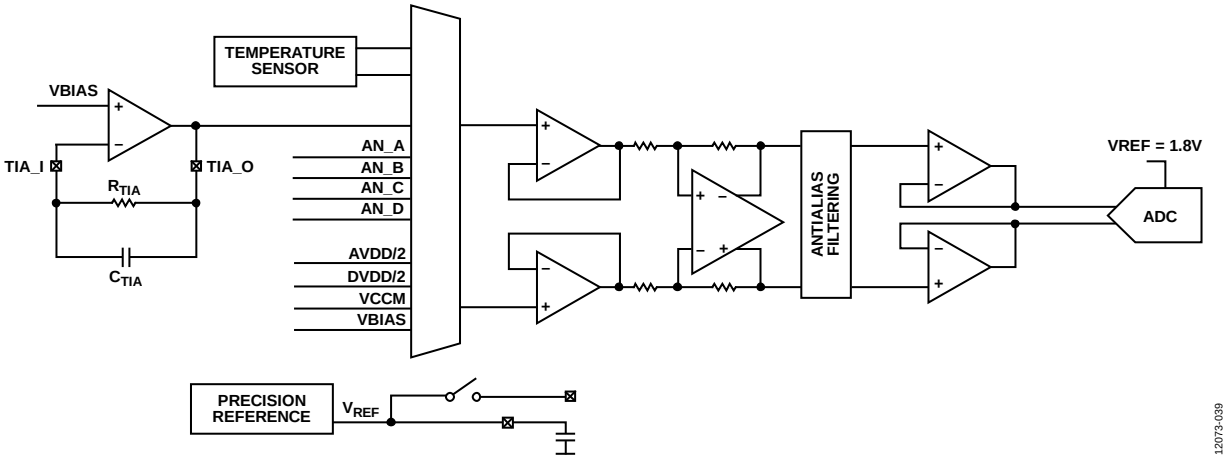

Figure 41. Rx Stage

MICROSUBSYSTEM

MEMORIES

The memory offerings for the ADuCM350 are as follows:

- 384 kB flash.
- 16 kB of flash configured for EEPROM emulation.
- 2 kB user information.
- 32 kB SRAM.
- 2 kB dedicated SRAM for USB endpoint.

Flash

The ADuCM350 includes 384 kB of embedded flash memory, accessed using the flash controller. The flash controller is connected to the bus matrix as a slave device for core and DMA access, as well as the 32-bit AHB for MMR access.

The flash controller supports 384 kB of user space and 2 kB of information space. Read and write to flash are executed via AHB only. The 384 kB flash memory comprises one 256 kB flash array and one 128 kB flash array. The 256 kB flash memory array and 128 kB flash array are controlled by two separate flash controllers with separate register controls.

With respect to flash integrity, the device supports

- Automatic signature check of information space at reset
- User signature for application code
- Parity checking on a per access basis
- 20,000 cycle endurance with 20 ms erase and 20 µs program
- 100-year data retention at room temperature

General-Purpose Flash

The device contains 16 kB of embedded flash memory for general purpose, such as EEPROM emulation.

SRAM

There is 32 kB of SRAM on chip of which 16 kB is retained during hibernate mode and an optional 16 kB can be retained during hibernate for reduced leakage current.

DEBUG CAPABILITY

The ADuCM350 supports two types of debug host interface: 4-wire JTAG debug (JTAG) interface and a serial 2-wire debug (SWD) interface.

The ADuCM350 incorporates the complete embedded trace of the ARM Cortex-M3 features to maximize code analysis, system profiling, and debugging capabilities.

PROGRAMMABLE GPIOS

The ADuCM350 has 66 GPIO pins, most of which have multiple, configurable functions defined by user code. They can be configured as an input/output and have programmable pull-up or pull-down resistors. All I/O pins are functional over the full supply range (VBAT = 1.8 V to 3.6 V).

In power saving mode, GPIO pins retain state; they tristate on reset to prevent any bus irritation. GPIOs of note are as follows:

- 32 pins multiplexed with LCD segment common pins
- Six pins multiplexed with CapTouch
- Nine pins on a dedicated VDDIO for ease of interfacing to peripherals

TIMERS

General-Purpose Timers

ADuCM350 has three identical general-purpose timers, each with a 16-bit count-up/count-down counter. The count-up/count-down counter can be clocked from one of four user selectable clock sources. Any selected clock source can be scaled down using a prescaler of 16, 256, or 32,768.

Watch Dog Timer (WDT)

The watchdog timer is a 16-bit count-down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, 256, or 4096. The watchdog timer is clocked either by the 32 kHz crystal oscillator (LFXTAL) or by the 32 kHz on-chip oscillator (LFOSC).The watchdog timer (WDT) is used to recover from an illegal software state. After the WUT is enabled by user code, it requires periodic servicing to prevent it from forcing a reset or interrupt of the processor. A WDT timeout can generate a reset or an interrupt.

Wake-Up Timer

The wake-up timer (WUT) consists of a 32-bit counter clocked from the 32 kHz external crystal (LFXTAL), 32 kHz internal oscillator (LFOSC), or peripheral clock (PCLK). The selected clock source can be scaled

USB

The USB port on the ADuCM350 is a USB 2.0 full speed compliant port. The module consists of the USB controller, USB PHY, USB RAM, and a 2-channel DMA. An integrated regulator powered by VBUS supplies the USB PHY. A dedicated PLL with 60 MHz clock capability is available for clock generation.

The USB supports bulk, isochronous, interrupt, and control modes. It has seven hardware endpoint and a dedicated 2-channel DMA. It supports suspend and wakeup.

The controller hardware is supplemented by a complete set of USB device class drivers to provide complete USB functionality using a defined Micrium stack. The USB stack has a requirement for an RTOS to be on the system. Analog Devices, Inc., has developed its system using the Micrium µC/OS-II.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D12073-0-5/14(A)