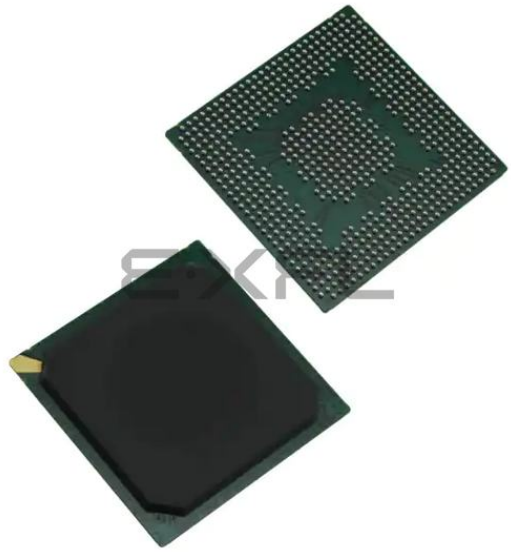

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8315cvragda

CAUTION

When the device is in D3 warm (standby) mode, all external voltage supplies applied to any I/O pins, with the exception of wake-up pins, must be turned off. Applying supplied external voltage to any I/O pins, except the wake up pins, while the device is in D3 warm standby mode may cause permanent damage to the device.

An example of the power-up sequence is shown in Figure 4 when implemented along with low power D3 warm mode.

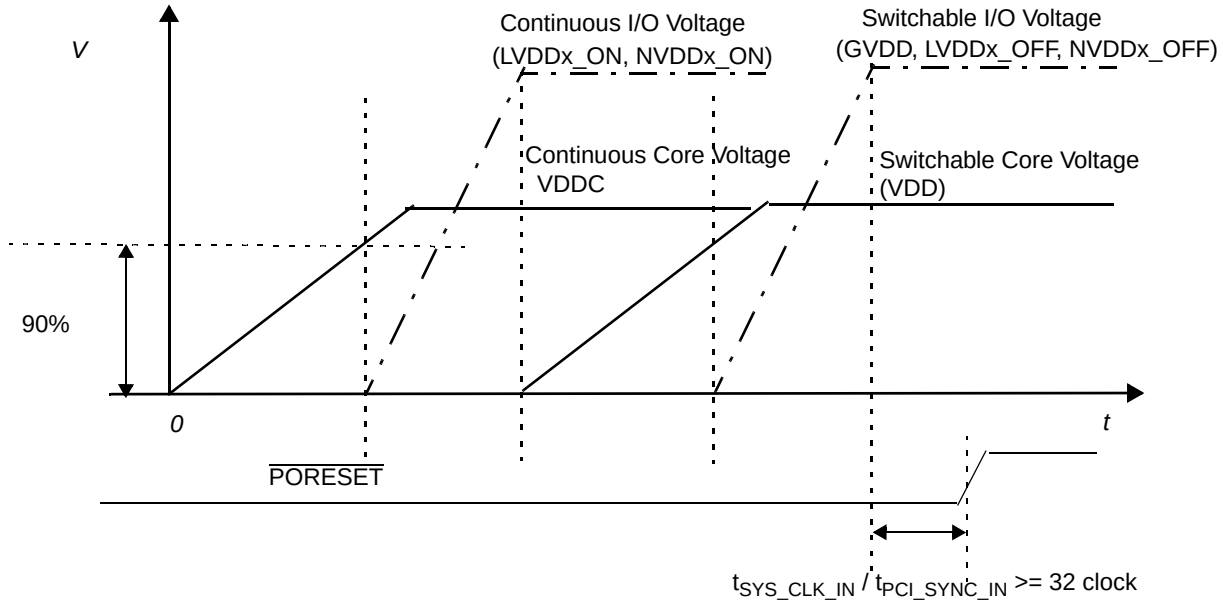

Figure 4. Power Up Sequencing Example with Low power D3 Warm Mode

The switchable and continuous supplies can be combined when the D3 warm mode is not used.

The SATA power supplies VDD33PLL and VDD33ANA should go high after NVDD3_OFF supply and go low before NVDD3_OFF supply. The NVDD3_OFF voltage levels should not drop below the VDD33PLL, VDD33ANA voltages at any time.

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

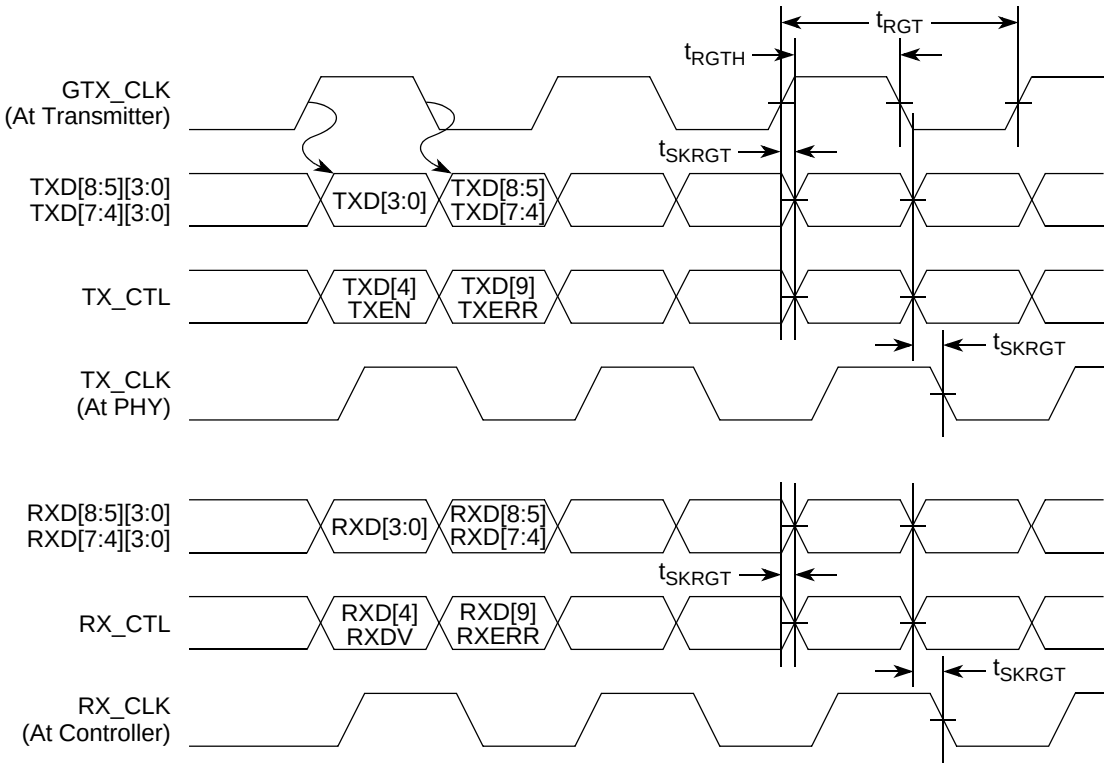

Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

9.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for MII, RMII, RGMII, and RTBI are specified in Section 9.1, "eTSEC (10/100/1000 Mbps)—MII/RMII/RGMII/RTBI Electrical Characteristics."

9.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NVDD	—	—	3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NVDD = Min	2.10	NVDD + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NVDD = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.00	—	V
Input low voltage	V_{IL}	—	—	—	0.80	V
Input high current	I_{IH}	NVDD = Max	V_{IN} [1] = 2.1 V	—	40	μA

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V (continued)

Parameter	Symbol	Conditions		Min	Max	Unit
Input low current	I_{IL}	NVDD = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

9.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 31. MII Management AC Timing Specifications

At recommended operating conditions with NVDD is 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the maximum frequency is 4.16 MHz and the minimum frequency is 0.593 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 133 MHz, the delay is 60 ns).

Table 33. 1588 Timer AC Specifications (continued)

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9.5 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of MPC8315E as shown in Figure 18, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 49.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 26.4, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ pins.

9.5.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, "High-Speed Serial Interfaces (HSSI)."

9.5.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 34. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Unit	Note
t_{REF}	REFCLK cycle time	—	8	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

9.5.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 35 and Table 36 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX[n]}}$) as depicted in Figure 17.

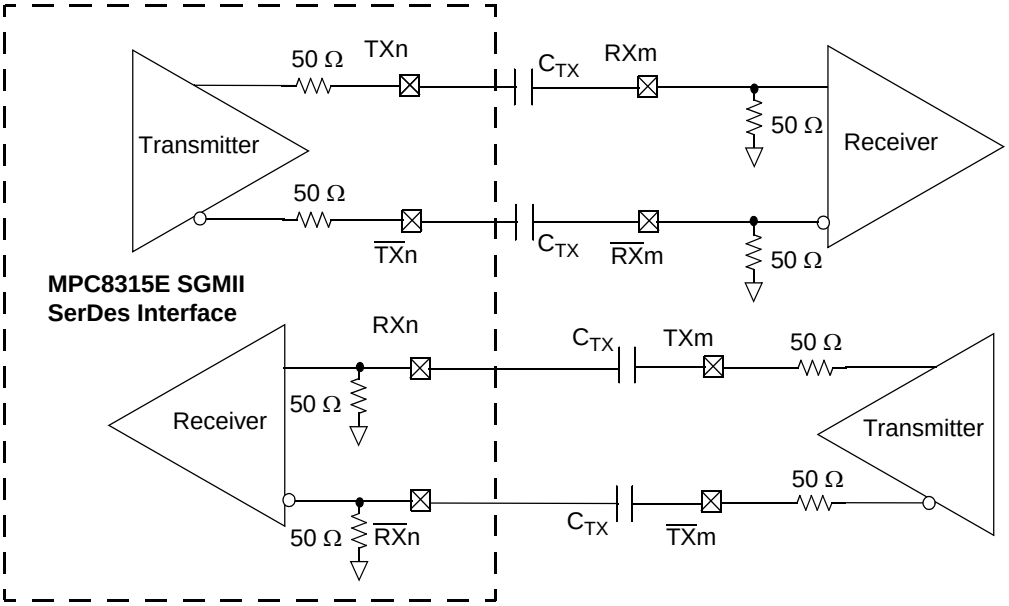

Figure 18. 4-Wire AC-Coupled SGMII Serial Link Connection Example

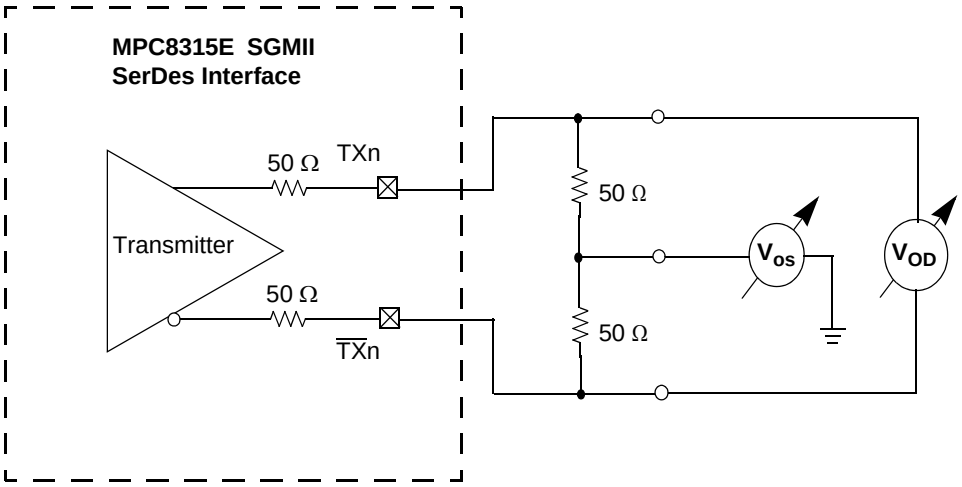

Figure 19. SGMII Transmitter DC Measurement Circuit

Table 36. SGMII DC Receiver Electrical Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		XCOREVDD	0.95	1.0	1.05	V	—
DC Input voltage range		—	N/A			—	1
Input differential voltage	EQ = 0	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	EQ = 1		175	—			
Loss of signal threshold	EQ = 0	VLOS	30	—	100	mV	3, 4
	EQ = 1		65	—	175		

Table 41. USB_CLK_IN DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.4	V

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 42. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typical	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	—	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/Time interval error	Peak to peak value measured with a second order high-pass filter of 500 KHz bandwidth	t_{CLK_PJ}	—	—	200	ps

11 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8315E.

11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 43. DC Electrical Characteristics (when Operating at 3.3 V)

Parameter	Symbol	Min	Max	Unit
Output high voltage (NVDD = min, I_{OH} = –2 mA)	V_{OH}	NVDD – 0.2	—	V
Output low voltage (NVDD = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V
Input high voltage	V_{IH}	2	NVDD + 0.3	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input high current (V_{IN} = 0 V or V_{IN} = NVDD)	I_{IN}	—	±5	μA

11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the MPC8315E.

Table 44. Local Bus General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 48. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 47)

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs
Fall time of both SDA and SCL signals	t_{I2CF} [4]	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × NVDD	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × NVDD	—	V

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8315E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. MPC8315E does not follow the *I2C-BUS Specifications* version 2.1 regarding the tI2CF AC parameter.

This figure provides the AC test load for the I²C.

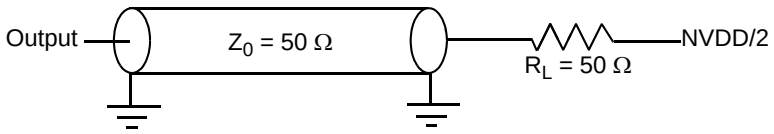

Figure 33. I²C AC Test Load

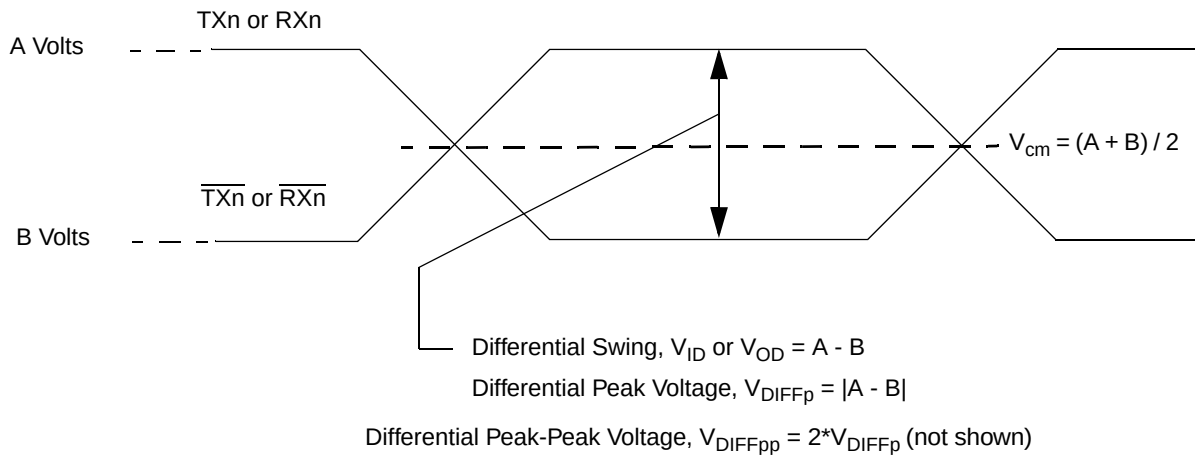

Figure 38. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ for PCI Express and SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

15.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XCOREVDD are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

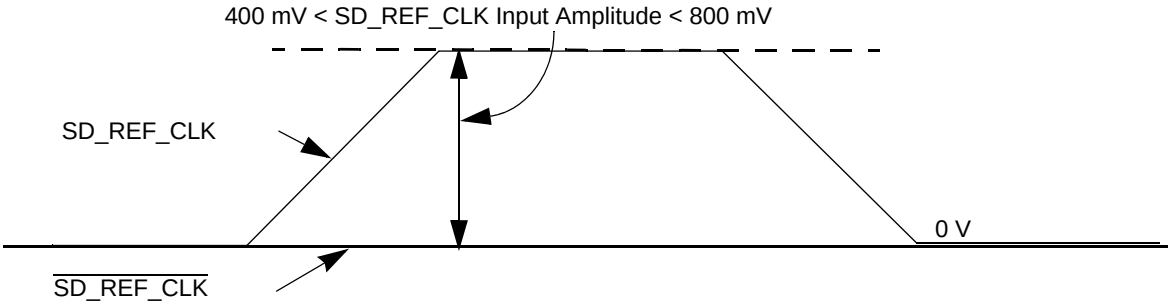

Figure 42. Single-Ended Reference Clock Input DC Requirements

15.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to XCOREVSS, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43–Figure 46 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it’s very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8315E SerDes reference clock receiver requirement provided in this document.

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 52. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Note:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 47.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 48.

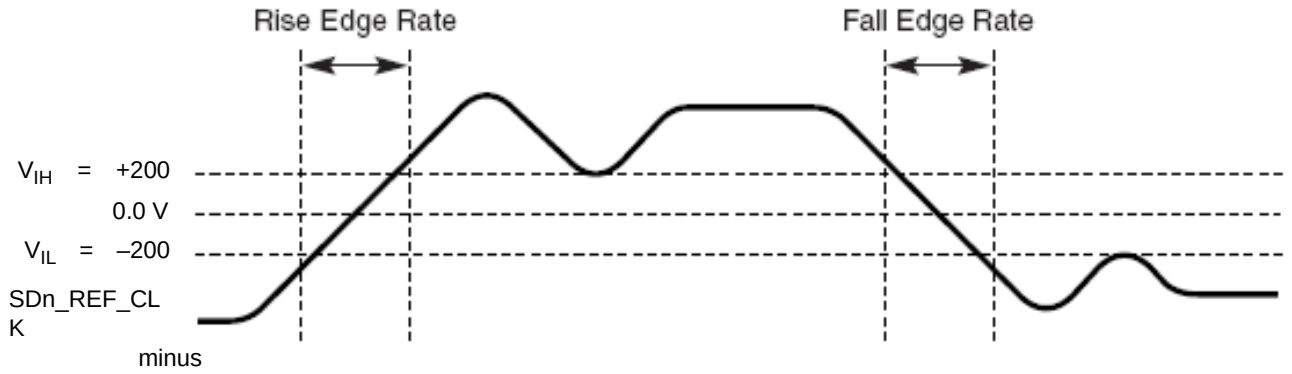

Figure 47. Differential Measurement Points for Rise and Fall Time

Table 54. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
De-Emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.	–3.0	–3.5	-4.0	dB	2
Minimum TX eye width	$T_{TX\text{-}EYE}$	The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER}$ = 1 - $U_{TX\text{-}EYE}$= 0.3 UI.	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median	$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.	—	—	0.15	UI	2, 3
D+/D- TX output rise/fall time	$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	—	0.125	—	—	UI	2, 5
RMS AC peak common mode output voltage	$V_{TX\text{-}CM\text{-}ACp}$	$V_{TX\text{-}CM\text{-}ACp}$ = RMS(|V_{TXD+} + $V_{TXD\text{-}}$|/2 - $V_{TX\text{-}CM\text{-}DC}$) $V_{TX\text{-}CM\text{-}DC}$ = $DC_{(avg)}$ of |$V_{TX\text{-}D+}$ + $V_{TX\text{-}D\text{-}}$|/2	—	—	20	mV	2
Absolute delta of DC common mode voltage during L0 and electrical idle	$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	|$V_{TX\text{-}CM\text{-}DC\ (during\ L0)}$ - $V_{TX\text{-}CM\text{-}Idle\text{-}DC\ (During\ Electrical\ Idle)}$|<=100 mV $V_{TX\text{-}CM\text{-}DC}$ = $DC_{(avg)}$ of |$V_{TX\text{-}D+}$ + $V_{TX\text{-}D\text{-}}$|/2 [L0] $V_{TX\text{-}CM\text{-}Idle\text{-}DC}$ = $DC_{(avg)}$ of |$V_{TX\text{-}D+}$ + $V_{TX\text{-}D\text{-}}$|/2 [Electrical Idle]	0	—	100	mV	2
Absolute delta of DC common mode between D+ and D–	$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	|$V_{TX\text{-}CM\text{-}DC\text{-}D+}$ - $V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}}$| <= 25 mV $V_{TX\text{-}CM\text{-}DC\text{-}D+}$ = $DC_{(avg)}$ of |$V_{TX\text{-}D+}$| $V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}}$ = $DC_{(avg)}$ of |$V_{TX\text{-}D\text{-}}$|	0	—	25	mV	2
Electrical idle differential peak output voltage	$V_{TX\text{-}IDLE\text{-}DIFFp}$	$V_{TX\text{-}IDLE\text{-}DIFFp}$ = |$V_{TX\text{-}IDLE\text{-}D+}$ -$V_{TX\text{-}IDLE\text{-}D\text{-}}$| <= 20 mV	0	—	20	mV	2
Amount of voltage change allowed during receiver detection	$V_{TX\text{-}RCV\text{-}DETECT}$	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present.	—	—	600	mV	6
TX DC common mode voltage	$V_{TX\text{-}DC\text{-}CM}$	The allowed DC Common Mode voltage under any conditions.	—	—	3.6	V	6
TX short circuit current limit	$I_{TX\text{-}SHORT}$	The total current the Transmitter can provide when shorted to its ground	—	—	90	mA	—
Minimum time spent in electrical idle	$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set	50	—	—	UI	—

Table 54. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX-IDLE-SET-TO-IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX-DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	RL_{TX-CM}	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX-DIFF-DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	Z_{TX-DC}	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX-SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—
AC coupling capacitor	C_{TX}	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	75	—	200	nF	8
Crosslink random timeout	$T_{crosslink}$	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.	0	—	1	ms	7

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.
8. MPC8315E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required

17.3 Out-of-Band (OOB) Electrical Characteristics

This table provides the out-of-band (OOB) electrical characteristics for the SATA interface of the MPC8315.

Table 59. Out-of-Band (OOB) Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
OOB Signal Detection Threshold 1.5G 3.0G	$V_{SATA\_OOBDETE}$	 50 75	 100 125	 200 200	mVp-p	—
UI During OOB Signaling	T_{SATA_UIOOB}	—	666.67	—	ps	—
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	$T_{SATA\_UIOOBTXB}$	—	160	—	UI	—
COMINIT/ COMRESET Transmit Gap Length	$T_{SATA\_UIOOBTXGap}$	—	480	—	UI	—
COMWAKE Transmit Gap Length	$T_{SATA\_UIOOBTX WakeGap}$	—	160	—	UI	—

18 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8315E.

18.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 60. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

18.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 61. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Table 70. MPC8315E TEPBGA II Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	AF16	I/O	GVDD	—
MEMC_MDQ[1]	AE17	I/O	GVDD	—
MEMC_MDQ[2]	AH17	I/O	GVDD	—
MEMC_MDQ[3]	AG17	I/O	GVDD	—
MEMC_MDQ[4]	AG18	I/O	GVDD	—
MEMC_MDQ[5]	AH18	I/O	GVDD	—
MEMC_MDQ[6]	AD18	I/O	GVDD	—
MEMC_MDQ[7]	AF19	I/O	GVDD	—
MEMC_MDQ[8]	AH19	I/O	GVDD	—
MEMC_MDQ[9]	AD19	I/O	GVDD	—
MEMC_MDQ[10]	AG20	I/O	GVDD	—
MEMC_MDQ[11]	AH20	I/O	GVDD	—
MEMC_MDQ[12]	AH21	I/O	GVDD	—
MEMC_MDQ[13]	AE21	I/O	GVDD	—
MEMC_MDQ[14]	AH22	I/O	GVDD	—
MEMC_MDQ[15]	AD21	I/O	GVDD	—
MEMC_MDQ[16]	AG10	I/O	GVDD	—
MEMC_MDQ[17]	AH9	I/O	GVDD	—
MEMC_MDQ[18]	AH8	I/O	GVDD	—
MEMC_MDQ[19]	AD11	I/O	GVDD	—
MEMC_MDQ[20]	AH7	I/O	GVDD	—
MEMC_MDQ[21]	AG7	I/O	GVDD	—
MEMC_MDQ[22]	AF8	I/O	GVDD	—
MEMC_MDQ[23]	AD10	I/O	GVDD	—
MEMC_MDQ[24]	AE9	I/O	GVDD	—
MEMC_MDQ[25]	AH6	I/O	GVDD	—
MEMC_MDQ[26]	AH5	I/O	GVDD	—
MEMC_MDQ[27]	AG6	I/O	GVDD	—
MEMC_MDQ[28]	AH4	I/O	GVDD	—
MEMC_MDQ[29]	AE6	I/O	GVDD	—
MEMC_MDQ[30]	AD8	I/O	GVDD	—
MEMC_MDQ[31]	AF5	I/O	GVDD	—
MEMC_MDM0	AE18	O	GVDD	—
MEMC_MDM1	AE20	O	GVDD	—
MEMC_MDM2	AE10	O	GVDD	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{QUIESCE}}$	B5	O	$NVDD1_{ON}$	—
System Control				
$\overline{\text{HRESET}}$	B6	I/O	$NVDD1_{ON}$	1
$\overline{\text{PORESET}}$	A6	I	$NVDD1_{ON}$	—
Clocks				
SYS_XTAL_IN	L27	I	$NVDD2_{ON}$	—
SYS_XTAL_OUT	J28	O	$NVDD2_{ON}$	—
SYS_CLK_IN	K28	I	$NVDD2_{ON}$	—
USB_XTAL_IN	A15	I	$NVDD2_{OFF}$	—
USB_XTAL_OUT	B14	O	$NVDD2_{OFF}$	—
USB_CLK_IN	B15	I	$NVDD2_{OFF}$	—
PCI_SYNC_OUT	J27	O	$NVDD2_{ON}$	3
RTC_CLK	K26	I	$NVDD2_{ON}$	—
PCI_SYNC_IN	K27	I	$NVDD2_{ON}$	—
MISC				
AVDD1	AC15	I	—	—
AVDD2	M23	I	—	—
THERM0	L25	I	$NVDD2_{ON}$	7
$\overline{\text{DMA\_DACK0}}$/GPIO_13	AC4	I/O	$NVDD1_{OFF}$	—
$\overline{\text{DMA\_DREQ0}}$/GPIO_12	AD1	I/O	$NVDD1_{OFF}$	—
DMA_DONE0/GPIO_14	AD2	I/O	$NVDD1_{OFF}$	—
NC, No Connect	A2	—	—	—
NC, No Connect	U25	—	—	—
PCI				
$\overline{\text{PCI\_INTA}}$	B18	O	$NVDD2_{OFF}$	—
$\overline{\text{PCI\_RESET\_OUT}}$	A20	O	$NVDD2_{OFF}$	—
PCI_AD[0]	J25	I/O	$NVDD2_{OFF}$	—
PCI_AD[1]	J24	I/O	$NVDD2_{OFF}$	—
PCI_AD[2]	K24	I/O	$NVDD2_{OFF}$	—
PCI_AD[3]	H27	I/O	$NVDD2_{OFF}$	—
PCI_AD[4]	H28	I/O	$NVDD2_{OFF}$	—
PCI_AD[5]	H26	I/O	$NVDD2_{OFF}$	—
PCI_AD[6]	G27	I/O	$NVDD2_{OFF}$	—
PCI_AD[7]	G28	I/O	$NVDD2_{OFF}$	—
PCI_AD[8]	F26	I/O	$NVDD2_{OFF}$	—

Table 70. MPC8315E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
ETSEC2				
GPIO_26/TSEC2_COL	A8	I/O	$LVDD2_{ON}$	—
GPIO_27/TSEC2_CRS	E9	I/O	$LVDD2_{ON}$	—
TSEC2_GTX_CLK	B10	O	$LVDD2_{ON}$	—
TSEC2_RX_CLK	B8	I	$LVDD2_{ON}$	—
TSCE2_RX_DV	C9	I	$LVDD2_{ON}$	—
TSEC2_RXD[3]	C10	I	$LVDD2_{ON}$	—
TSEC2_RXD[2]	D10	I	$LVDD2_{ON}$	—
TSEC2_RXD[1]	A9	I	$LVDD2_{ON}$	—
TSEC2_RXD[0]	B9	I	$LVDD2_{ON}$	—
TSEC2_RX_ER	A10	I	$LVDD2_{ON}$	—
TSEC2_TX_CLK	D8	I	$LVDD2_{ON}$	—
TSEC2_TXD[3]/CFG_RESET_SOURCE[0]	D11	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[2]/CFG_RESET_SOURCE[1]	C7	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[1]/CFG_RESET_SOURCE[2]	E8	I/O	$LVDD2_{ON}$	—
TSEC2_TXD[0]/CFG_RESET_SOURCE[3]	B7	I/O	$LVDD2_{ON}$	—
TSEC2_TX_EN	D12	O	$LVDD2_{ON}$	—
TSEC2_TX_ER	B11	O	$LVDD2_{ON}$	—
SGMII / PCI Express PHY				
TXA	P4	O	XPADVDD	—
$\overline{\text{TXA}}$	N4	O	XPADVDD	—
RXA	R1	I	XCOREVDD	—
$\overline{\text{RXA}}$	P1	I	XCOREVDD	—
TXB	U4	O	XPADVDD	—
$\overline{\text{TXB}}$	V4	O	XPADVDD	—
RXB	U1	I	XCOREVDD	—
$\overline{\text{RXB}}$	V1	I	XCOREVDD	—
SD_IMP_CAL_RX	N3	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	R4	I	XCOREVDD	—
SD_REF_CLK	R5	I	XCOREVDD	—
SD_PLL_TPD	T2	O	—	—
SD_IMP_CAL_TX	V5	I	XPADVDD	—
SDAVDD	T3	I	—	—
SD_PLL_TPA_ANA	T4	O	—	—
SDAVSS	T5	I	—	—
USB Phy				

Table 79. Heat Sinks and Junction-to-Case Thermal Resistance of MPC8315E TEPBGA II

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm TEBGA II
		Junction-to-Ambient Thermal Resistance
AAVID 30 x 30 x 9.4 mm Pin Fin	Natural Convection	14.4
AAVID 30 x 30 x 9.4 mm Pin Fin	0.5 m/s	11.4
AAVID 30 x 30 x 9.4 mm Pin Fin	1 m/s	10.1
AAVID 30 x 30 x 9.4 mm Pin Fin	2 m/s	8.9
AAVID 35 x 31 x 23 mm Pin Fin	Natural Convection	12.3
AAVID 35 x 31 x 23 mm Pin Fin	0.5 m/s	9.3
AAVID 35 x 31 x 23 mm Pin Fin	1 m/s	8.5
AAVID 35 x 31 x 23 mm Pin Fin	2 m/s	7.9
AAVID 43 x 41 x 16.5 mm Pin Fin	Natural Convection	12.5
AAVID 43 x 41 x 16.5 mm Pin Fin	0.5 m/s	9.7
AAVID 43 x 41 x 16.5 mm Pin Fin	1 m/s	8.5
AAVID 43 x 41 x 16.5 mm Pin Fin	2 m/s	7.7
Wakefield, 53 x 53 x 25 mm Pin Fin	Natural Convection	10.9
Wakefield, 53 x 53 x 25 mm Pin Fin	0.5 m/s	8.5
Wakefield, 53 x 53 x 25 mm Pin Fin	1 m/s	7.5
Wakefield, 53 x 53 x 25 mm Pin Fin	2 m/s	7.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias. Note that the RC filter results in lower voltage level on AVDD. This does not imply that the DC specification can be relaxed.

This figure shows the PLL power supply filter circuit.

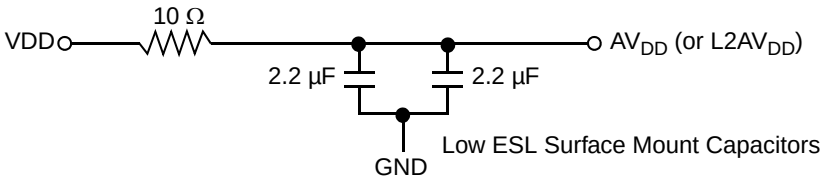

Figure 63. PLL Power Supply Filter Circuit

26.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8315E system, and the MPC8315E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, NVDD, GVDD, and LVDD pins of the device. These decoupling capacitors should receive their power from separate VDD, NVDD, GVDD, LVDD, and GND power planes in the PCB, utilizing thick and short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, NVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

26.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external VDD, GVDD, LVDD, NVDD, and GND pins of the device.

26.5 Output Buffer DC Impedance

The MPC8315E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NVDD or GND. Then, the value of each resistor is varied until the pad voltage is NVDD/2 (see Figure 64). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals NVDD/2. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

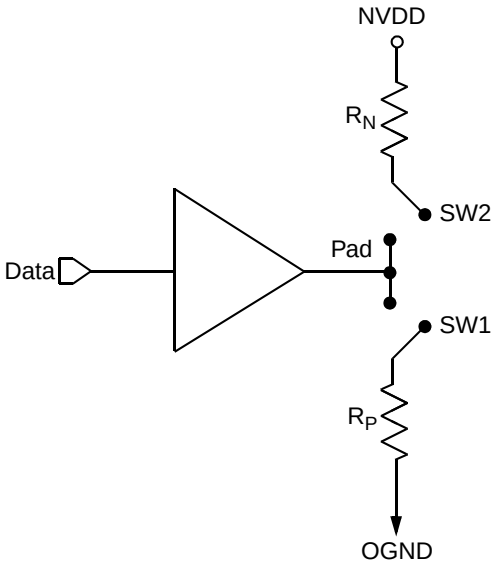

Figure 64. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 81. Part Numbering Nomenclature

MPC	8315	E	C	VR	AG	D	A
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1]**	**e300 Core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8315	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	VR= Pb Free TEPBGA II	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz	Contact local Freescale sales office

Note:
1. See Section 23, “Package and Pin Listings,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by electric may support other maximum core frequencies.
3. Contact your local Freescale field applications engineer (FAE).

This table shows the SVR settings by device and package type.

Table 82. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)	SVR (Rev 1.2)
MPC8315E	TEPBGA II	0x80B4_0010	0x80B4_0011	0x80B4_0012
MPC8315	TEPBGA II	0x80B5_0010	0x80B5_0011	0x80B5_0012

Note:
1. PVR = 8085_0020 for all devices and revisions in this table.